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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	50MHz
Connectivity	EBI/EMI, I²C, LINbus, SPI, UART/USART, USB
Peripherals	CapSense, DMA, LCD, POR, PWM, WDT
Number of I/O	25
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 16x12b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-BSSOP (0.295", 7.50mm Width)
Supplier Device Package	48-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c3446pva-076

Figure 2-4. 100-pin TQFP Part Pinout

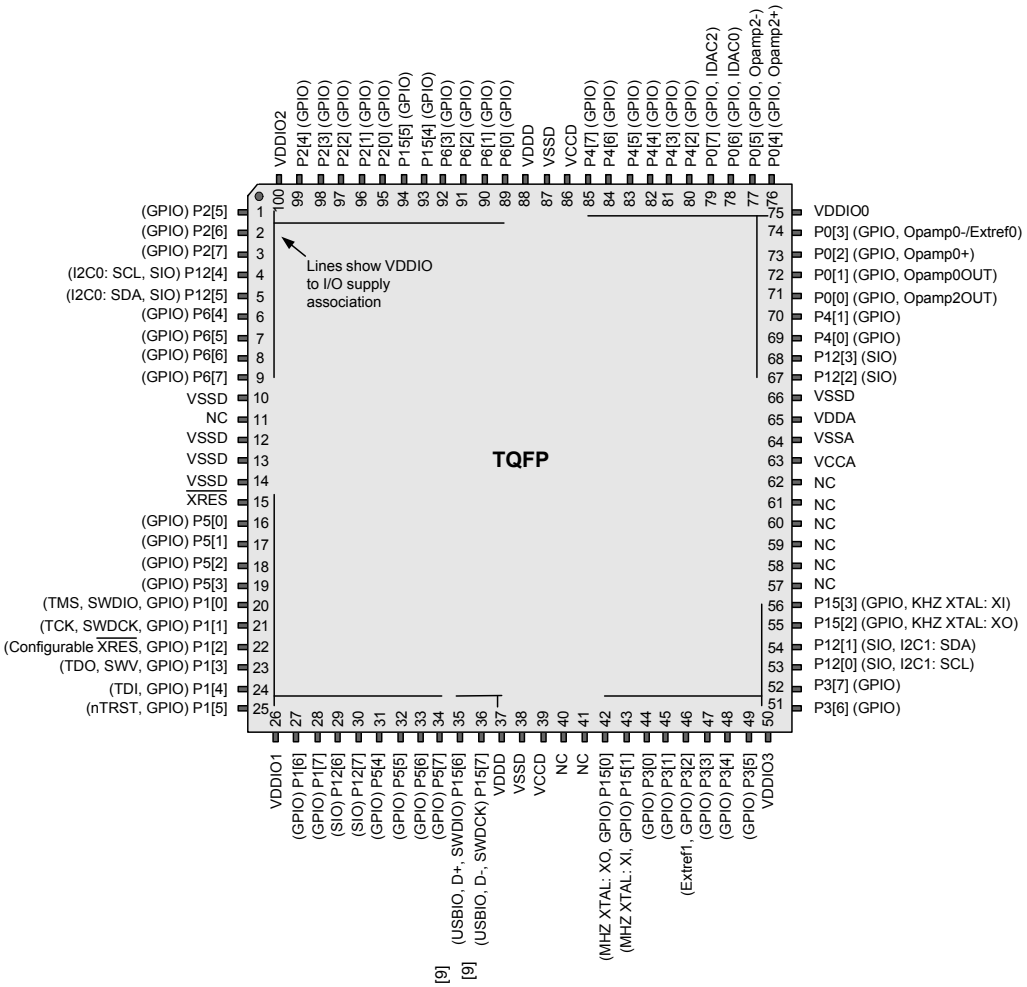


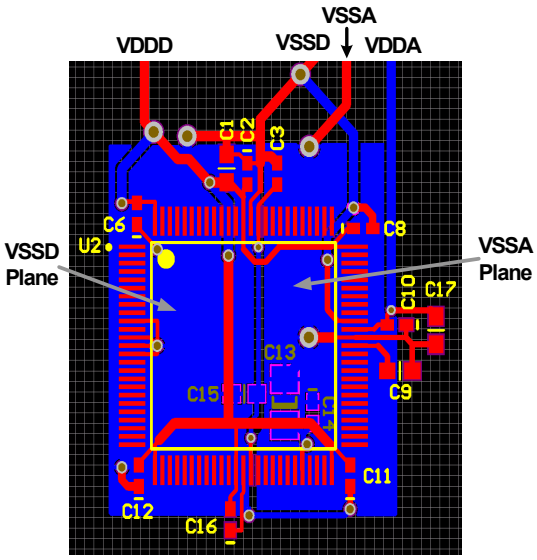
Figure 2-5 and Figure 2-6 show an example schematic and an example PCB layout, for the 100-pin TQFP part, for optimal analog performance on a two-layer board.

- The two pins labeled VDDD must be connected together.
- The two pins labeled VCCD must be connected together, with capacitance added, as shown in Figure 2-5 and Power System on page 29. The trace between the two VCCD pins should be as short as possible.
- The two pins labeled Vssd must be connected together.

For information on circuit board layout issues for mixed signals, refer to the application note, AN57821 - Mixed Signal Circuit Board Layout Considerations for PSoC® 3 and PSoC 5.

Note
9. Pins are Do Not Use (DNU) on devices without USB. The pin must be left floating.

Figure 2-6. Example PCB Layout for 100-pin TQFP Part for Optimal Analog Performance



3. Pin Descriptions

IDAC0, IDAC2

Low resistance output pin for high current DACs (IDAC).

Opamp0OUT, Opamp2OUT

High current output of uncommitted opamp[10].

Extref0, Extref1

External reference input to the analog system.

Opamp0–, Opamp2–

Inverting input to uncommitted opamp.

Opamp0+, Opamp2+

Noninverting input to uncommitted opamp.

GPIO

General purpose I/O pin provides interfaces to the CPU, digital peripherals, analog peripherals, interrupts, LCD segment drive, and CapSense[10].

I2C0: SCL, I2C1: SCL

I^2C SCL line providing wake from sleep on an address match. Any I/O pin can be used for I^2C SCL if wake from sleep is not required.

I2C0: SDA, I2C1: SDA

I^2C SDA line providing wake from sleep on an address match. Any I/O pin can be used for I^2C SDA if wake from sleep is not required.

kHz XTAL: Xo, kHz XTAL: Xi

32.768-kHz crystal oscillator pin.

MHz XTAL: Xo, MHz XTAL: Xi

4- to 25-MHz crystal oscillator pin.

nTRST

Optional JTAG test reset programming and debug port connection to reset the JTAG connection.

SIO

Special I/O provides interfaces to the CPU, digital peripherals and interrupts with a programmable high threshold voltage, analog comparator, high sink current, and high impedance state when the device is unpowered.

SWDCK

Serial wire debug clock programming and debug port connection.

SWDIO

Serial wire debug input and output programming and debug port connection.

SWV

Single wire viewer debug output.

TCK

JTAG test clock programming and debug port connection.

TDI

JTAG test data in programming and debug port connection.

TDO

JTAG test data out programming and debug port connection.

TMS

JTAG test mode select programming and debug port connection.

Note
10. GPIOs with opamp outputs are not recommended for use with CapSense.

Table 4-4. Boolean Instructions *(continued)*

Mnemonic	Description	Bytes	Cycles
ANL C, /bit	AND complement of direct bit to carry	2	2
ORL C, bit	OR direct bit to carry	2	2
ORL C, /bit	OR complement of direct bit to carry	2	2
MOV C, bit	Move direct bit to carry	2	2
MOV bit, C	Move carry to direct bit	2	3
JC rel	Jump if carry is set	2	3
JNC rel	Jump if no carry is set	2	3
JB bit, rel	Jump if direct bit is set	3	5
JNB bit, rel	Jump if direct bit is not set	3	5
JBC bit, rel	Jump if direct bit is set and clear bit	3	5

Table 4-8. Interrupt Vector Table

#	Fixed Function	DMA	UDB
0	LVD	phub_termout0[0]	udb_intr[0]
1	Cache/ECC	phub_termout0[1]	udb_intr[1]
2	Reserved	phub_termout0[2]	udb_intr[2]
3	Sleep (Pwr Mgr)	phub_termout0[3]	udb_intr[3]
4	PICU[0]	phub_termout0[4]	udb_intr[4]
5	PICU[1]	phub_termout0[5]	udb_intr[5]
6	PICU[2]	phub_termout0[6]	udb_intr[6]
7	PICU[3]	phub_termout0[7]	udb_intr[7]
8	PICU[4]	phub_termout0[8]	udb_intr[8]
9	PICU[5]	phub_termout0[9]	udb_intr[9]
10	PICU[6]	phub_termout0[10]	udb_intr[10]
11	PICU[12]	phub_termout0[11]	udb_intr[11]
12	PICU[15]	phub_termout0[12]	udb_intr[12]
13	Comparators Combined	phub_termout0[13]	udb_intr[13]
14	Switched Caps Combined	phub_termout0[14]	udb_intr[14]
15	I^2C	phub_termout0[15]	udb_intr[15]
16	CAN	phub_termout1[0]	udb_intr[16]
17	Timer/Counter0	phub_termout1[1]	udb_intr[17]
18	Timer/Counter1	phub_termout1[2]	udb_intr[18]
19	Timer/Counter2	phub_termout1[3]	udb_intr[19]
20	Timer/Counter3	phub_termout1[4]	udb_intr[20]
21	USB SOF Int	phub_termout1[5]	udb_intr[21]
22	USB Arb Int	phub_termout1[6]	udb_intr[22]
23	USB Bus Int	phub_termout1[7]	udb_intr[23]
24	USB Endpoint[0]	phub_termout1[8]	udb_intr[24]
25	USB Endpoint Data	phub_termout1[9]	udb_intr[25]
26	Reserved	phub_termout1[10]	udb_intr[26]
27	LCD	phub_termout1[11]	udb_intr[27]
28	Reserved	phub_termout1[12]	udb_intr[28]
29	Decimator Int	phub_termout1[13]	udb_intr[29]
30	PHUB Error Int	phub_termout1[14]	udb_intr[30]
31	EEPROM Fault Int	phub_termout1[15]	udb_intr[31]

Figure 6-8. SIO Input/Output Block Diagram

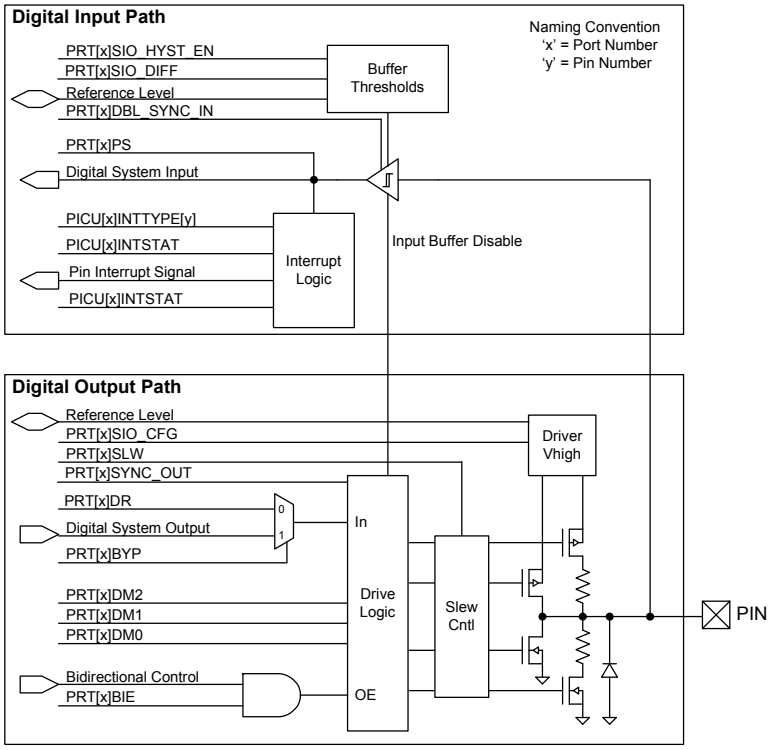
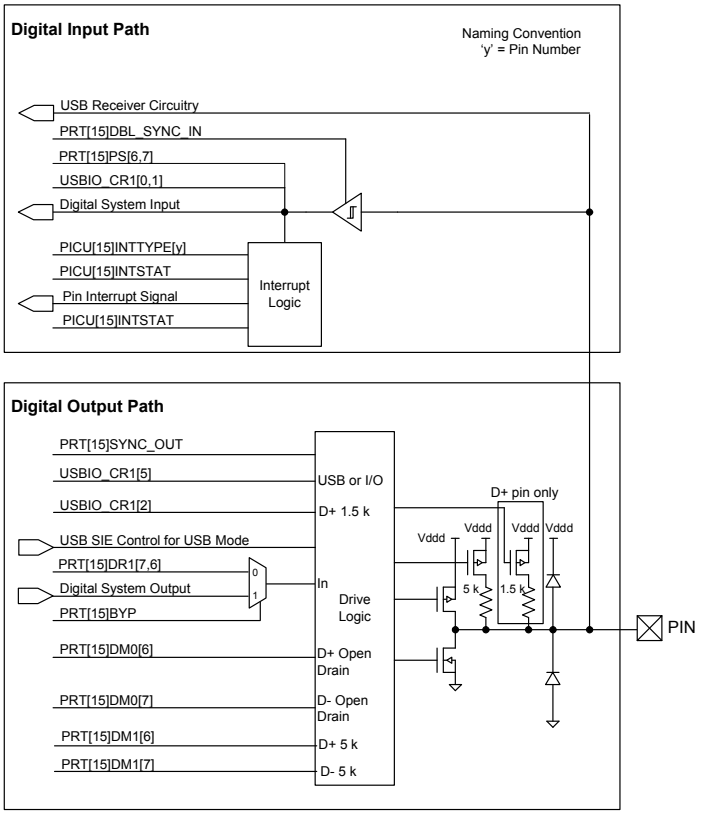


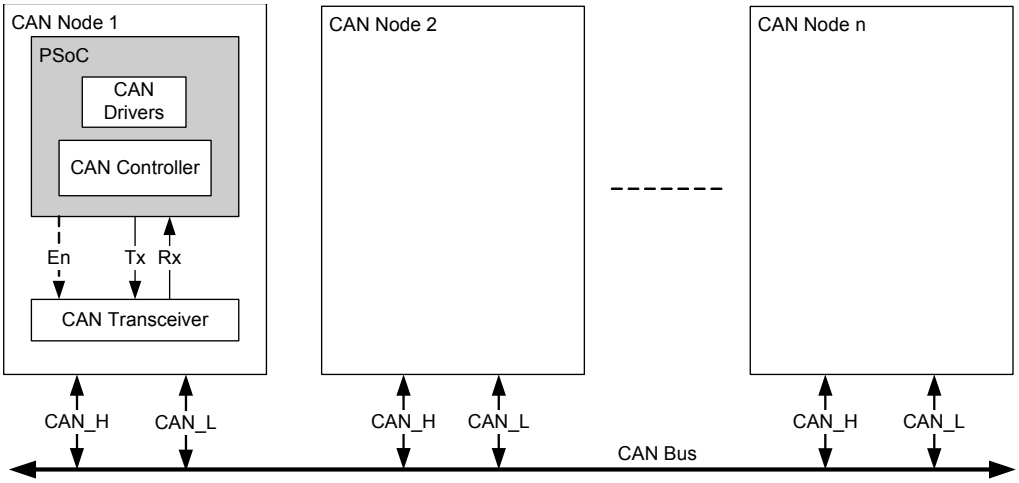
Figure 6-9. USBIO Block Diagram



7.5 CAN

The CAN peripheral is a fully functional controller area network (CAN) supporting communication baud rates up to 1 Mbps. The CAN controller implements the CAN2.0A and CAN2.0B specifications as defined in the Bosch specification and conforms to the ISO-11898-1 standard. The CAN protocol was originally designed for automotive applications with a focus on a high level of fault detection. This ensures high communication reliability at a low cost. Because of its success in automotive applications, CAN is used as a standard communication protocol for motion oriented machine control networks (CANOpen) and factory automation applications (DeviceNet). The CAN controller features allow the efficient implementation of higher level protocols without affecting the performance of the microcontroller CPU. Full configuration support is provided in PSoC Creator.

Figure 7-14. CAN Bus System Implementation



7.5.1 CAN Features

- CAN2.0A/B protocol implementation – ISO 11898 compliant
  - Standard and extended frames with up to 8 bytes of data per frame
  - Message filter capabilities
  - Remote Transmission Request (RTR) support
  - Programmable bit rate up to 1 Mbps
- Listen Only mode
- SW readable error counter and indicator
- Sleep mode: Wake the device from sleep with activity on the Rx pin
- Supports two or three wire interface to external transceiver (Tx, Rx, and Enable). The three-wire interface is compatible with the Philips PHY; the PHY is not included on-chip. The three wires can be routed to any I/O
- Enhanced interrupt controller
  - CAN receive and transmit buffers status
  - CAN controller error status including BusOff
- Receive path
  - 16 receive buffers each with its own message filter
  - Enhanced hardware message filter implementation that covers the ID, IDE, and RTR
  - DeviceNet addressing support
  - Multiple receive buffers linkable to build a larger receive message array
  - Automatic transmission request (RTR) response handler
  - Lost received message notification
- Transmit path
  - Eight transmit buffers
  - Programmable transmit priority
  - Round robin
  - Fixed priority
  - Message transmissions abort capability

7.5.2 Software Tools Support

CAN Controller configuration integrated into PSoC Creator:

- CAN Configuration walkthrough with bit timing analyzer
- Receive filter setup

8. Analog Subsystem

The analog programmable system creates application specific combinations of both standard and advanced analog signal processing blocks. These blocks are then interconnected to each other and also to any pin on the device, providing a high level of design flexibility and IP security. The features of the analog subsystem are outlined here to provide an overview of capabilities and architecture.

- Flexible, configurable analog routing architecture provided by analog globals, analog mux bus, and analog local buses.
- High resolution delta-sigma ADC.
- Two 8-bit DACs that provide either voltage or current output.
- Four comparators with optional connection to configurable LUT outputs.
- Two configurable switched capacitor/continuous time (SC/CT) blocks for functions that include opamp, unity gain buffer, programmable gain amplifier, transimpedance amplifier, and mixer.
- Two opamps for internal use and connection to GPIO that can be used as high current output buffers.
- CapSense subsystem to enable capacitive touch sensing.
- Precision reference for generating an accurate analog voltage for internal analog blocks.

Figure 8-1. Analog Subsystem Block Diagram

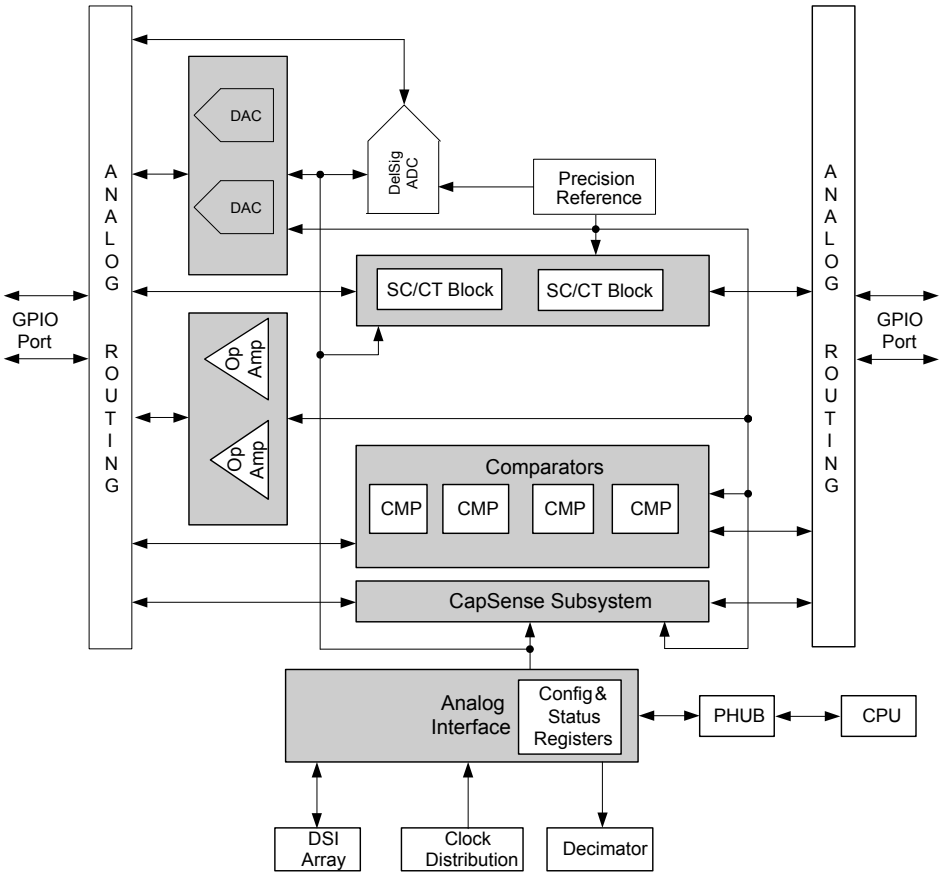
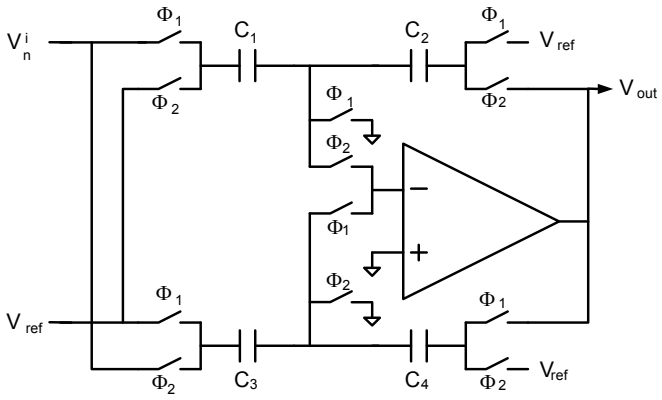


Figure 8-13. Sample and Hold Topology (Φ1 and Φ2 are opposite phases of a clock)



8.11.1 Down Mixer

The SC/CT block can be used as a mixer to down convert an input signal. This circuit is a high bandwidth passive sample network that can sample input signals up to 14 MHz. This sampled value is then held using the opamp with a maximum clock rate of 4 MHz. The output frequency is at the difference between the input frequency and the highest integer multiple of the Local Oscillator that is less than the input.

8.11.2 First Order Modulator – SC Mode

A first order modulator is constructed by placing the SC/CT block in an integrator mode and using a comparator to provide a 1-bit feedback to the input. Depending on this bit, a reference voltage is either subtracted or added to the input signal. The block output is the output of the comparator and not the integrator in the modulator case. The signal is downshifted and buffered and then processed by a decimator to make a delta-sigma converter or a counter to make an incremental converter. The accuracy of the sampled data from the first-order modulator is determined from several factors.

The main application for this modulator is for a low-frequency ADC with high accuracy. Applications include strain gauges, thermocouples, precision voltage, and current measurement.

9. Programming, Debug Interfaces, Resources

PSoC devices include extensive support for programming, testing, debugging, and tracing both hardware and firmware. Three interfaces are available: JTAG, SWD, and SWV. JTAG and SWD support all programming and debug features of the device. JTAG also supports standard JTAG scan chains for board level test and chaining multiple JTAG devices to a single JTAG connection.

For more information on PSoC 3 Programming, refer to the PSoC® 3 Device Programming Specifications.

Complete Debug on Chip (DoC) functionality enables full device debugging in the final system using the standard production device. It does not require special interfaces, debugging pods, simulators, or emulators. Only the standard programming connections are required to fully support debug.

The PSoC Creator IDE software provides fully integrated programming and debug support for PSoC devices. The low cost MiniProg3 programmer and debugger is designed to provide full programming and debug support of PSoC devices in conjunction with the PSoC Creator IDE. PSoC JTAG, SWD, and SWV interfaces are fully compatible with industry standard third party tools.

All DOC circuits are disabled by default and can only be enabled in firmware. If not enabled, the only way to reenable them is to erase the entire device, clear flash protection, and reprogram the device with new firmware that enables DOC. Disabling DOC features, robust flash protection, and hiding custom analog and digital functionality inside the PSoC device provide a level of security not possible with multichip application solutions. Additionally, all device interfaces can be permanently disabled (Device Security) for applications concerned about phishing attacks due to a maliciously reprogrammed device. Permanently disabling interfaces is not recommended in most applications because you cannot access the device later. Because all programming, debug, and test interfaces are disabled when device security is enabled, PSoCs with Device Security enabled may not be returned for failure analysis.

Table 9-1. Debug Configurations

Debug and Trace Configuration	GPIO Pins Used
All debug and trace disabled	0
JTAG	4 or 5
SWD	2
SWV	1
SWD + SWV	3

9.1 JTAG Interface

The IEEE 1149.1 compliant JTAG interface exists on four or five pins (the nTRST pin is optional). The JTAG interface is used for programming the flash memory, debugging, I/O scan chains, and JTAG device chaining.

PSoC 3 has certain timing requirements to be met for entering programming mode through the JTAG interface. Due to these timing requirements, not all standard JTAG programmers, or standard JTAG file formats such as SVF or STAPL, can support PSoC 3 programming. The list of programmers that support PSoC 3 programming is available at http://www.cypress.com/go/programming.

The JTAG clock frequency can be up to 14 MHz, or 1/3 of the CPU clock frequency for 8 and 16-bit transfers, or 1/5 of the CPU clock frequency for 32-bit transfers. By default, the JTAG pins are enabled on new devices but the JTAG interface can be disabled, allowing these pins to be used as GPIO instead.

9.2 Serial Wire Debug Interface

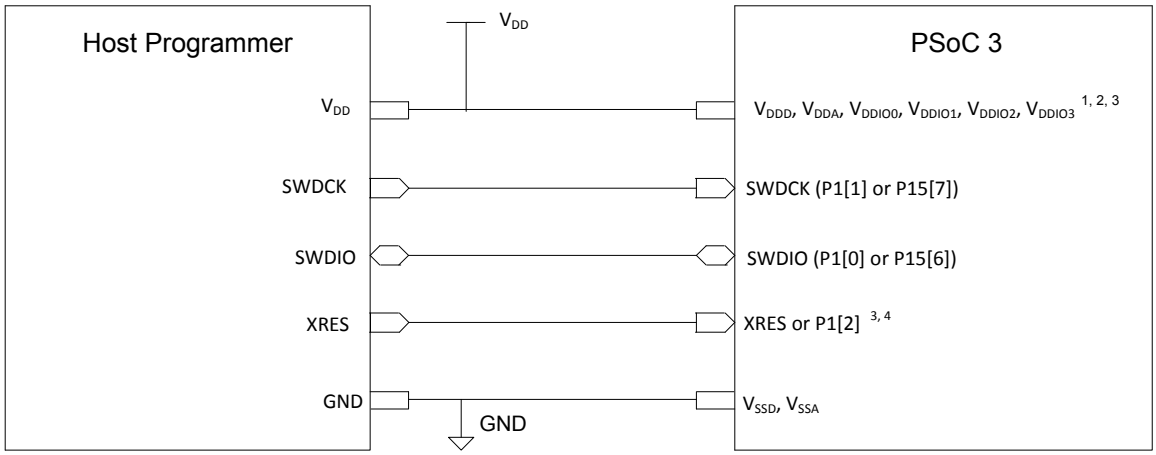
The SWD interface is the preferred alternative to the JTAG interface. It requires only two pins instead of the four or five needed by JTAG. SWD provides all of the programming and debugging features of JTAG at the same speed. SWD does not provide access to scan chains or device chaining. The SWD clock frequency can be up to 1/3 of the CPU clock frequency.

SWD uses two pins, either two of the JTAG pins (TMS and TCK) or the USBIO D+ and D– pins. The USBIO pins are useful for in system programming of USB solutions that would otherwise require a separate programming connector. One pin is used for the data clock and the other is used for data input and output.

SWD can be enabled on only one of the pin pairs at a time. This only happens if, within 8 µs (key window) after reset, that pin pair (JTAG or USB) receives a predetermined sequence of 1s and 0s. SWD is used for debugging or for programming the flash memory.

The SWD interface can be enabled from the JTAG interface or disabled, allowing its pins to be used as GPIO. Unlike JTAG, the SWD interface can always be reacquired on any device during the key window. It can then be used to reenable the JTAG interface, if desired. When using SWD or JTAG pins as standard GPIO, make sure that the GPIO functionality and PCB circuits do not interfere with SWD or JTAG use.

Figure 9-2. SWD Interface Connections between PSoC 3 and Programmer



[1] The voltage levels of the Host Programmer and the PSoC 3 voltage domains involved in Programming should be the same. XRES pin (XRES_N or P1[2]) is powered by V_{DDIO1}. The USB SWD pins are powered by V_{DDD}. So for Programming using the USB SWD pins with XRES pin, the V_{DDD}, V_{DDIO1} of PSoC 3 should be at the same voltage level as Host V_{DD}. Rest of PSoC 3 voltage domains (V_{DDA}, V_{DDIO0}, V_{DDIO2}, V_{DDIO3}) need not be at the same voltage level as host Programmer. The Port 1 SWD pins are powered by V_{DDIO1}. So V_{DDIO1} of PSoC 3 should be at same voltage level as host V_{DD} for Port 1 SWD programming. Rest of PSoC 3 voltage domains (V_{DDD}, V_{DDA}, V_{DDIO0}, V_{DDIO2}, V_{DDIO3}) need not be at the same voltage level as host Programmer.

[2] Vdda must be greater than or equal to all other power supplies (Vddd, Vddio's) in PSoC 3.

[3] For Power cycle mode Programming, XRES pin is not required. But the Host programmer must have the capability to toggle power (Vddd, Vdda, All Vddio's) to PSoC 3. This may typically require external interface circuitry to toggle power which will depend on the programming setup. The power supplies can be brought up in any sequence, however, once stable, VDDA must be greater than or equal to all other supplies.

[4] P1[2] will be configured as XRES by default only for 48-pin devices (without dedicated XRES pin). For devices with dedicated XRES pin, P1[2] is GPIO pin by default. So use P1[2] as Reset pin only for 48-pin devices, but use dedicated XRES pin for rest of devices.

9.3 Debug Features

Using the JTAG or SWD interface, the CY8C34 supports the following debug features:

- Halt and single-step the CPU
- View and change CPU and peripheral registers, and RAM addresses
- Eight program address breakpoints
- One memory access breakpoint—break on reading or writing any memory address and data value
- Break on a sequence of breakpoints (non recursive)
- Debugging at the full speed of the CPU
- Compatible with PSoC Creator and MiniProg3 programmer and debugger
- Standard JTAG programming and debugging interfaces make CY8C34 compatible with other popular third-party tools (for example, ARM / Keil)

9.4 Trace Features

The CY8C34 supports the following trace features when using JTAG or SWD:

- Trace the 8051 program counter (PC), accumulator register (ACC), and one SFR / 8051 core RAM register
- Trace depth up to 1000 instructions if all registers are traced, or 2000 instructions if only the PC is traced (on devices that include trace memory)
- Program address trigger to start tracing
- Trace windowing, that is, only trace when the PC is within a given range
- Two modes for handling trace buffer full: continuous (overwriting the oldest trace data) or break when trace buffer is full

9.5 Single Wire Viewer Interface

The SWV interface is closely associated with SWD but can also be used independently. SWV data is output on the JTAG interface's TDO pin. If using SWV, you must configure the device for SWD, not JTAG. SWV is not supported with the JTAG interface.

SWV is ideal for application debug where it is helpful for the firmware to output data similar to 'printf' debugging on PCs. The SWV is ideal for data monitoring, because it requires only a single pin and can output data in standard UART format or Manchester encoded format. For example, it can be used to tune a PID control loop in which the output and graphing of the three error terms greatly simplifies coefficient tuning.

The following features are supported in SWV:

- 32 virtual channels, each 32 bits long
- Simple, efficient packing and serializing protocol
- Supports standard UART format (N81)

9.6 Programming Features

The JTAG and SWD interfaces provide full programming support. The entire device can be erased, programmed, and verified. You can increase flash protection levels to protect firmware IP. Flash protection can only be reset after a full device erase. Individual flash blocks can be erased, programmed, and verified, if block security settings permit.

9.7 Device Security

PSoC 3 offers an advanced security feature called device security, which permanently disables all test, programming, and debug ports, protecting your application from external access. The device security is activated by programming a 32-bit key (0×50536F43) to a Write Once Latch (WOL).

The Write Once Latch is a type of nonvolatile latch (NVL). The cell itself is an NVL with additional logic wrapped around it. Each WOL device contains four bytes (32 bits) of data. The wrapper outputs a '1' if a super-majority (28 of 32) of its bits match a pre-determined pattern (0×50536F43); it outputs a '0' if this majority is not reached. When the output is 1, the Write Once NV latch locks the part out of Debug and Test modes; it also permanently gates off the ability to erase or alter the contents of the latch. Matching all bits is intentionally not required, so that single (or few) bit failures do not deassert the WOL output. The state of the NVL bits after wafer processing is truly random with no tendency toward 1 or 0.

The WOL only locks the part after the correct 32-bit key (0×50536F43) is loaded into the NVL's volatile memory, programmed into the NVL's nonvolatile cells, and the part is reset. The output of the WOL is only sampled on reset and used to disable the access. This precaution prevents anyone from reading, erasing, or altering the contents of the internal memory.

The user can write the key into the WOL to lock out external access only if no flash protection is set (see "Flash Security" on page 21). However, after setting the values in the WOL, a user still has access to the part until it is reset. Therefore, a user can write the key into the WOL, program the flash protection data, and then reset the part to lock it.

If the device is protected with a WOL setting, Cypress cannot perform failure analysis and, therefore, cannot accept RMAs from customers. The WOL can be read out through the SWD port to electrically identify protected parts. The user can write the key in WOL to lock out external access only if no flash protection is set. For more information on how to take full advantage of the security features in PSoC see the PSoC 3 TRM.

Disclaimer

Note the following details of the flash code protection features on Cypress devices.

Cypress products meet the specifications contained in their particular Cypress data sheets. Cypress believes that its family of products is one of the most secure families of its kind on the market today, regardless of how they are used. There may be methods, unknown to Cypress, that can breach the code protection features. Any of these methods, to our knowledge, would be dishonest and possibly illegal. Neither Cypress nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Cypress is willing to work with the customer who is concerned about the integrity of their code. Code protection is constantly evolving. We at Cypress are committed to continuously improving the code protection features of our products.

10. Development Support

The CY8C34 family has a rich set of documentation, development tools, and online resources to assist you during your development process. Visit psoc.cypress.com/getting-started to find out more.

10.1 Documentation

A suite of documentation, supports the CY8C34 family to ensure that you can find answers to your questions quickly. This section contains a list of some of the key documents.

Software User Guide: A step-by-step guide for using PSoC Creator. The software user guide shows you how the PSoC Creator build process works in detail, how to use source control with PSoC Creator, and much more.

Component data sheets: The flexibility of PSoC allows the creation of new peripherals (components) long after the device has gone into production. Component data sheets provide all of the information needed to select and use a particular component, including a functional description, API documentation, example code, and AC/DC specifications.

Application Notes: PSoC application notes discuss a particular application of PSoC in depth; examples include brushless DC motor control and on-chip filtering. Application notes often include example projects in addition to the application note document.

Technical Reference Manual: The Technical Reference Manual (TRM) contains all the technical detail you need to use a PSoC device, including a complete description of all PSoC registers.

10.2 Online

In addition to print documentation, the Cypress PSoC forums connect you with fellow PSoC users and experts in PSoC from around the world, 24 hours a day, 7 days a week.

10.3 Tools

With industry standard cores, programming, and debugging interfaces, the CY8C34 family is part of a development tool ecosystem. Visit us at www.cypress.com/go/psoccreator for the latest information on the revolutionary, easy to use PSoC Creator IDE, supported third party compilers, programmers, debuggers, and development kits.

11. Electrical Specifications

Specifications are valid for -40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted. The unique flexibility of the PSoC UDBs and analog blocks enable many functions to be implemented in PSoC Creator components, see the component data sheets for full AC/DC specifications of individual functions. See the Example Peripherals on page 40 for further explanation of PSoC Creator components.

11.1 Absolute Maximum Ratings

Table 11-1. Absolute Maximum Ratings DC Specifications [17]

Parameter	Description	Conditions	Min	Typ	Max	Units
Tstorag	Storage temperature	Recommended storage temperature is 0 °C–50 °C. Exposure to storage temperatures above 125 °C for extended periods may affect device reliability	–55	25	125	°C
Vdda	Analog supply voltage relative to Vssd		–0.5	–	6	V
Vddd	Digital supply voltage relative to Vssd		–0.5	–	6	V
Vddio	I/O supply voltage relative to Vssd		–0.5	–	6	V
Vcca	Direct analog core voltage input		–0.5	–	1.95	V
Vccd	Direct digital core voltage input		–0.5	–	1.95	V
Vssa	Analog ground voltage		Vssd – 0.5	–	Vssd + 0.5	V
Vgpio[18]	DC input voltage on GPIO	Includes signals sourced by Vdda and routed internal to the pin	Vssd – 0.5	–	Vddio + 0.5	V
Vsio	DC input voltage on SIO	Output disabled	Vssd – 0.5	–	7	V
		Output enabled	Vssd – 0.5	–	6	V
Ivddio [19]	Current per Vddio supply pin	–40 °C to +85 °C	–	–	100	mA
		–40 °C to +125 °C	–	–	40	
I_{GPIO}	GPIO current		–30	–	41	mA
I_{SIO}	SIO current		–49	–	28	mA
I_{USBIO}	USBIO current		–56	–	59	mA
V_{EXTREF}	ADC external reference inputs	Pins P0[3], P3[2]	–	–	2	V
LU	Latch up current [20]		–140	–	140	mA
ESD_{HBM}	Electrostatic discharge voltage, Human body model	V_{SSA} tied to V_{SSD}	2200	–	–	V
		V_{SSA} not tied to V_{SSD}	750	–	–	V
ESD_{CDM}	Electro-static discharge voltage	Charge Device Model	500	–	–	V

Note Usage above the absolute maximum conditions listed in Table 11-1 may cause permanent damage to the device. Exposure to maximum conditions for extended periods of time may affect device reliability. When used below maximum conditions but above normal operating conditions the device may not operate to specification.

Notes
17. Usage above the absolute maximum conditions listed in Table 11-1 may cause permanent damage to the device. Exposure to Absolute Maximum conditions for extended periods of time may affect device reliability. The Maximum Storage Temperature is 150 °C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below Absolute Maximum conditions but above normal operating conditions, the device may not operate to specification.
18. The Vddio supply voltage must be greater than the maximum analog voltage on the associated GPIO pins. Maximum analog voltage on GPIO pin ≤ Vddio ≤ Vdda.
19. Maximum value 100 mA of Iddio applies only to –40 °C to +85 °C range and the limit of Iddio parameter for the –40 °C to +125 °C range is 40 mA.
20. Meets or exceeds JEDEC Spec EIA/JESD78 IC Latch-up Test.

Figure 11-6. GPIO Output High Voltage and Current

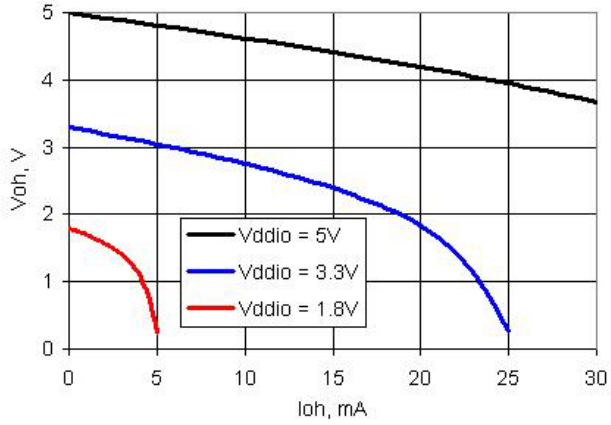


Figure 11-7. GPIO Output Low Voltage and Current

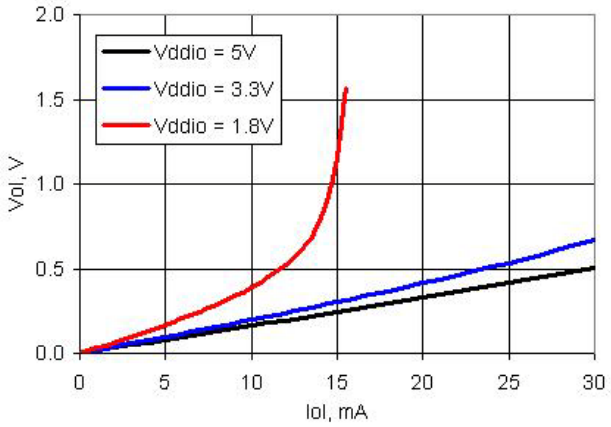


Table 11-7. GPIO AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
TriseF	Rise time in Fast Strong Mode[29]	3 V Vddio Cload = 25 pF	–	–	12	ns
TfallF	Fall time in Fast Strong Mode[29]	3 V Vddio Cload = 25 pF	–	–	12	ns
TriseS	Rise time in Slow Strong Mode[29]	3 V Vddio Cload = 25 pF	–	–	60	ns
TfallS	Fall time in Slow Strong Mode[29]	3 V Vddio Cload = 25 pF	–	–	60	ns
Fgpioout	GPIO output operating frequency					
	3 V ≤ Vddio ≤ 5.5 V, fast strong drive mode	90/10% Vddio into 25 pF, -40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C	-	-	33	MHz
		90/10% Vddio into 25 pF, -40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C	-	-	24	MHz
	1.71 V ≤ Vddio < 3 V, fast strong drive mode	90/10% Vddio into 25 pF, -40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C	-	-	20	MHz
		90/10% Vddio into 25 pF, -40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C	-	-	16	MHz
	3 V ≤ Vddio ≤ 5.5 V, slow strong drive mode	90/10% Vddio into 25 pF, -40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C	-	-	7	MHz
		90/10% Vddio into 25 pF, -40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C	-	-	7	MHz
	1.71 V ≤ Vddio < 3 V, slow strong drive mode	90/10% Vddio into 25 pF, -40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C	-	-	3.5	MHz
		90/10% Vddio into 25 pF, -40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C	-	-	3.5	MHz
Fgpioin	GPIO input operating frequency					
	1.71 V ≤ Vddio ≤ 5.5 V	90/10% better than 60/40 duty cycle, -40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C	-	-	66	MHz
		90/10% better than 60/40 duty cycle, -40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C	-	-	50	MHz

11.5.3 Voltage Reference

Table 11-20. Voltage Reference Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Vref	Precision reference	-40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C	1.021 (-0.3%)	1.024	1.027 (+0.3%)	V
		-40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C	1.018 (–0.6%)	1.024	1.030 (+0.6%)	V
	After typical PCB assembly, post reflow	Typical (non-optimized) board layout and 250 °C solder reflow. Device may be calibrated after assembly to improve performance.				
		–40 °C		±0.5		%
		25 °C		±0.2		%
		85 °C		±0.2		%
	Temperature drift[38]	Box method	–	–	30	ppm/°C
	Long term drift		–	100	–	ppm/khr
	Thermal cycling drift (stability)[38, 39]		–	100	–	ppm

Figure 11-25. Voltage Reference vs. Temperature and V_{CCA}

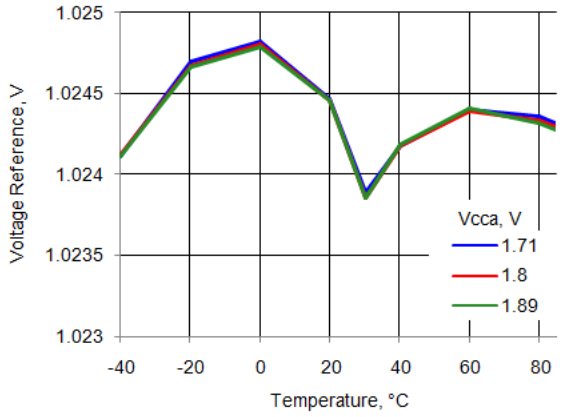
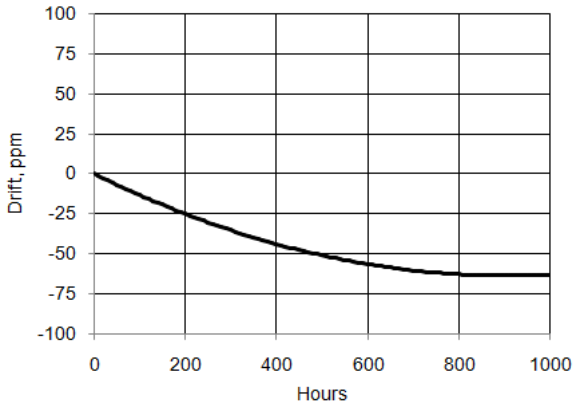
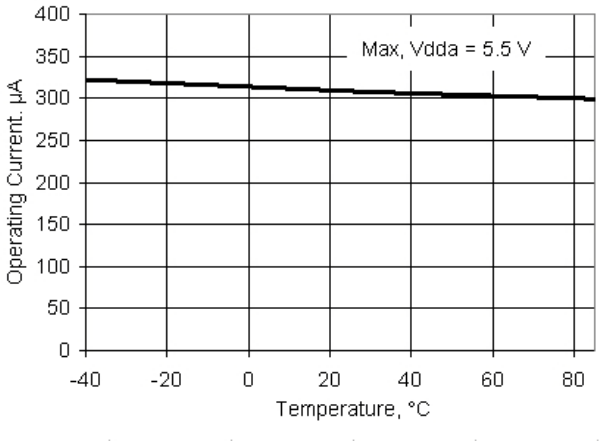


Figure 11-26. Voltage Reference Long-Term Drift



Notes
38. Based on device characterization (Not production tested).
39. After eight full cycles between –40 °C and 100 °C.

Figure 11-48. VDAC Operating Current vs Temperature, 1 V Mode, High speed mode



11.5.12 LCD Direct Drive

Table 11-35. LCD Direct Drive DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
I_{CC}	LCD system operating current	Device sleep mode with wakeup at 400-Hz rate to refresh LCDs, bus clock = 3 Mhz, Vddio = Vdda = 3 V, 4 commons, 16 segments, 1/4 duty cycle, 50 Hz frame rate, no glass connected	–	38	–	µA
I_{CC_SEG}	Current per segment driver	Strong drive mode	–	260	–	µA
V_{BIAS}	LCD bias range (V_{BIAS} refers to the main output voltage(V0) of LCD DAC)	$V_{DDA} \geq 3$ V and $V_{DDA} \geq V_{BIAS}$	2	–	5	V
	LCD bias step size	$V_{DDA} \geq 3$ V and $V_{DDA} \geq V_{BIAS}$	–	9.1 × V_{DDA}	–	mV
	LCD capacitance per segment/common driver	Drivers may be combined	–	500	5000	pF
	Long term segment offset		–	–	20	mV
I_{OUT}	Output drive current per segment driver)	Vddio = 5.5V, strong drive mode	355	–	710	µA

Table 11-36. LCD Direct Drive AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
f_{LCD}	LCD frame rate		10	50	150	Hz

11.8.3 Interrupt Controller

Table 11-65. Interrupt Controller AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Delay from Interrupt signal input to ISR code execution from ISR code	Includes worse case completion of longest instruction DIV with 6 cycles	-	-	25	Tcy CPU

11.8.4 JTAG Interface

Table 11-66. JTAG Interface AC Specifications[29]

Parameter	Description	Conditions	Min	Typ	Max	Units
f_TCK	TCK frequency	3.3 V ≤ V_{DDD} ≤ 5 V	–	–	14[58]	MHz
		1.71 V ≤ V_{DDD} < 3.3 V	–	–	7[58]	MHz
T_TDI_setup	TDI setup before TCK high		(T/10) – 5	–	–	ns
T_TMS_setup	TMS setup before TCK high		T/4	–	–	
T_TDI_hold	TDI, TMS hold after TCK high	T = 1/f_TCK max	T/4	–	–	
T_TDO_valid	TCK low to TDO valid	T = 1/f_TCK max	–	–	2T/5	
T_TDO_hold	TDO hold after TCK high	T = 1/f_TCK max	T/4	–	–	

Figure 11-60. JTAG Interface Timing

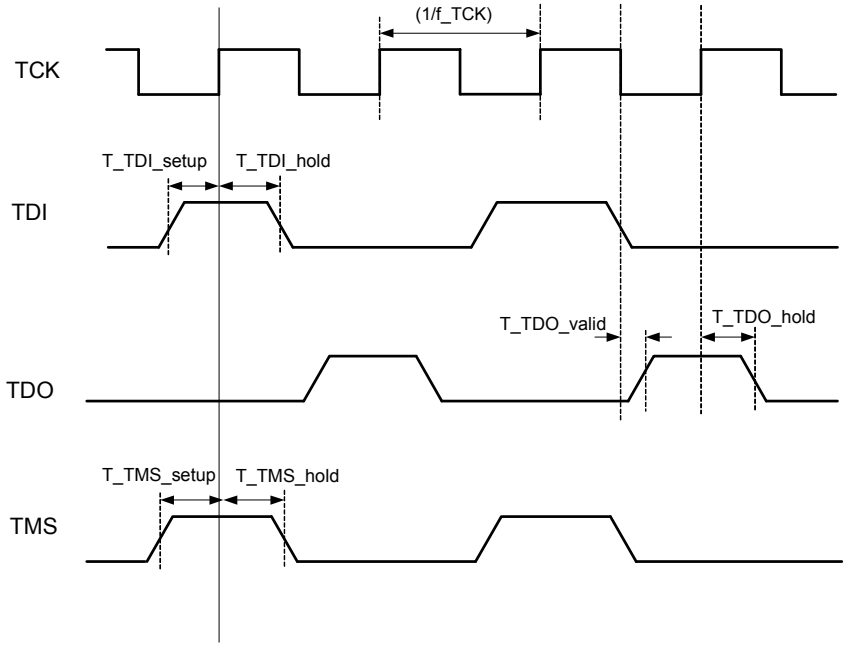


Table 14-1. Acronyms Used in this Document *(continued)*

Acronym	Description
PHUB	peripheral hub
PHY	physical layer
PICU	port interrupt control unit
PLA	programmable logic array
PLD	programmable logic device, see also PAL
PLL	phase-locked loop
PMDD	package material declaration data sheet
POR	power-on reset
PRES	precise low-voltage reset
PRS	pseudo random sequence
PS	port read data register
PSoC®	Programmable System-on-Chip™
PSRR	power supply rejection ratio
PWM	pulse-width modulator
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RTC	real-time clock
RTL	register transfer language
RTR	remote transmission request
RX	receive
SAR	successive approximation register
SC/CT	switched capacitor/continuous time
SCL	I^2C serial clock
SDA	I^2C serial data
S/H	sample and hold
SINAD	signal to noise and distortion ratio
SIO	special input/output, GPIO with advanced features. See GPIO.
SOC	start of conversion

Table 14-1. Acronyms Used in this Document *(continued)*

Acronym	Description
SOF	start of frame
SPI	Serial Peripheral Interface, a communications protocol
SR	slew rate
SRAM	static random access memory
SRES	software reset
SWD	serial wire debug, a test protocol
SWV	single-wire viewer
TD	transaction descriptor, see also DMA
THD	total harmonic distortion
TIA	transimpedance amplifier
TRM	technical reference manual
TTL	transistor-transistor logic
TX	transmit
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
UDB	universal digital block
USB	Universal Serial Bus
USBIO	USB input/output, PSoC pins used to connect to a USB port
VDAC	voltage DAC, see also DAC, IDAC
WDT	watchdog timer
WOL	write once latch, see also NVL
WRES	watchdog timer reset
XRES	external reset I/O pin
XTAL	crystal

15. Reference Documents

PSoC® 3, PSoC® 5 Architecture TRM

PSoC® 3 Registers TRM

17. Revision History *(continued)*

Description Title: PSoC® 3: CY8C34 Automotive Family Datasheet, Programmable System-on-Chip (PSoC®) Document Number: 001-57331				
Revision	**ECN**	**Submission Date**	**Orig. of Change**	**Description of Change**
*F	4174914	10/26/2013	NFB / ANMD	Updated Pinouts: Added Note 7 and referred the same note in 100 mA in description. Updated Electrical Specifications: Updated Absolute Maximum Ratings: Updated Table 11-1. Added Note 17 and referred the same note in Table 11-1. Added Note 19 and referred the same note in Ivddio parameter in Table 11-1. Updated Analog Peripherals: Updated Opamp: Updated Table 11-15. Updated Voltage Reference: Updated Table 11-20. Updated Packaging: Updated Table 13-1.
*G	4281204	02/14/2014	ANMD	Updated Digital Subsystem: Updated I^2C: Updated Note 16. Updated Electrical Specifications: Updated Analog Peripherals: Updated Delta-Sigma ADC: Updated Table 11-17: Updated Conditions of Vos parameter. Updated Memory: Updated Flash: Updated Table 11-50: Added Note 53 and referred the same note in “Flash data retention time, retention period measured from last erase cycle” in description column. Replaced “Tjavg” with “T_A” in last row in conditions column. Updated Packaging: spec 51-85048 – Changed revision from *H to *I. Completing Sunset Review.