

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | 8051 |
| Core Size | 8-Bit |
| Speed | 50MHz |
| Connectivity | EBI/EMI, I²C, LINbus, SPI, UART/USART |
| Peripherals | CapSense, DMA, LCD, POR, PWM, WDT |
| Number of I/O | 25 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 2K x 8 |
| RAM Size | 8K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.71V ~ 5.5V |
| Data Converters | A/D 16x12b; D/A 2x8b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 48-BSSOP (0.295", 7.50mm Width) |
| Supplier Device Package | 48-SSOP |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/cy8c3446pva-091 |

#### 4.3.1.5 Program Branching Instructions

The 8051 supports a set of conditional and unconditional jump instructions that help to modify the program execution flow. Table 4-5 shows the list of jump instructions.

**Table 4-5. Jump Instructions**

| Mnemonic | Description | Bytes | Cycles |
|---|---|---|---|
| ACALL addr11 | Absolute subroutine call | 2 | 4 |
| LCALL addr16 | Long subroutine call | 3 | 4 |
| RET | Return from subroutine | 1 | 4 |
| RETI | Return from interrupt | 1 | 4 |
| AJMP addr11 | Absolute jump | 2 | 3 |
| LJMP addr16 | Long jump | 3 | 4 |
| SJMP rel | Short jump (relative address) | 2 | 3 |
| JMP @A + DPTR | Jump indirect relative to DPTR | 1 | 5 |
| JZ rel | Jump if accumulator is zero | 2 | 4 |
| JNZ rel | Jump if accumulator is nonzero | 2 | 4 |
| CJNE A,Direct, rel | Compare direct byte to accumulator and jump if not equal | 3 | 5 |
| CJNE A, #data, rel | Compare immediate data to accumulator and jump if not equal | 3 | 4 |
| CJNE Rn, #data, rel | Compare immediate data to register and jump if not equal | 3 | 4 |
| CJNE @Ri, #data, rel | Compare immediate data to indirect RAM and jump if not equal | 3 | 5 |
| DJNZ Rn,rel | Decrement register and jump if not zero | 2 | 4 |
| DJNZ Direct, rel | Decrement direct byte and jump if not zero | 3 | 5 |
| NOP | No operation | 1 | 1 |

### 4.4 DMA and PHUB

The PHUB and the DMA controller are responsible for data transfer between the CPU and peripherals, and also data transfers between peripherals. The PHUB and DMA also control device configuration during boot. The PHUB consists of:

- A central hub that includes the DMA controller, arbiter, and router
- Multiple spokes that radiate outward from the hub to most peripherals

There are two PHUB masters: the CPU and the DMA controller. Both masters may initiate transactions on the bus. The DMA channels can handle peripheral communication without CPU intervention. The arbiter in the central hub determines which DMA channel is the highest priority if there are multiple requests.

#### 4.4.1 PHUB Features

- CPU and DMA controller are both bus masters to the PHUB
- Eight multi-layer AHB bus parallel access paths (spokes) for peripheral access
- Simultaneous CPU and DMA access to peripherals located on different spokes
- Simultaneous DMA source and destination burst transactions on different spokes
- Supports 8-, 16-, 24-, and 32-bit addressing and data

**Table 4-6. PHUB Spokes and Peripherals**

| PHUB Spokes | Peripherals |
|---|---|
| 0 | SRAM |
| 1 | IOs, PICU, EMIF |
| 2 | PHUB local configuration, Power manager, Clocks, IC, SWV, EEPROM, Flash programming interface |
| 3 | Analog interface and trim, Decimator |
| 4 | USB, CAN, I$^2$C, Timers, Counters, and PWMs |
| 5 | Reserved |
| 6 | UDBs group 1 |
| 7 | UDBs group 2 |

*4.4.2 DMA Features*

- 24 DMA channels
- Each channel has one or more transaction descriptors (TD) to configure channel behavior. Up to 128 total TDs can be defined
- TDs can be dynamically updated
- Eight levels of priority per channel
- Any digitally routable signal, the CPU, or another DMA channel, can trigger a transaction
- Each channel can generate up to two interrupts per transfer
- Transactions can be stalled or canceled
- Supports transaction size of infinite or 1 to 64 KB
- TDs may be nested and/or chained for complex transactions

*4.4.3 Priority Levels*

The CPU always has higher priority than the DMA controller when their accesses require the same bus resources. Due to the system architecture, the CPU can never starve the DMA. DMA channels of higher priority (lower priority number) may interrupt current DMA transfers. In the case of an interrupt, the current transfer is allowed to complete its current transaction. To ensure latency limits when multiple DMA accesses are requested simultaneously, a fairness algorithm guarantees an interleaved minimum percentage of bus bandwidth for priority levels 2 through 7. Priority levels 0 and 1 do not take part in the fairness algorithm and may use 100 percent of the bus bandwidth. If a tie occurs on two DMA requests of the same priority level, a simple round robin method is used to evenly share the allocated bandwidth. The round robin allocation can be disabled for each DMA channel, allowing it to always be at the head of the line.

Priority levels 2 to 7 are guaranteed the minimum bus bandwidth shown in Table 4-7 after the CPU and DMA priority levels 0 and 1 have satisfied their requirements.

**Table 4-7. Priority Levels**

| Priority Level | % Bus Bandwidth |
|---|---|
| 0 | 100.0 |
| 1 | 100.0 |
| 2 | 50.0 |
| 3 | 25.0 |
| 4 | 12.5 |
| 5 | 6.2 |
| 6 | 3.1 |
| 7 | 1.5 |

When the fairness algorithm is disabled, DMA access is granted based solely on the priority level; no bus bandwidth guarantees are made.

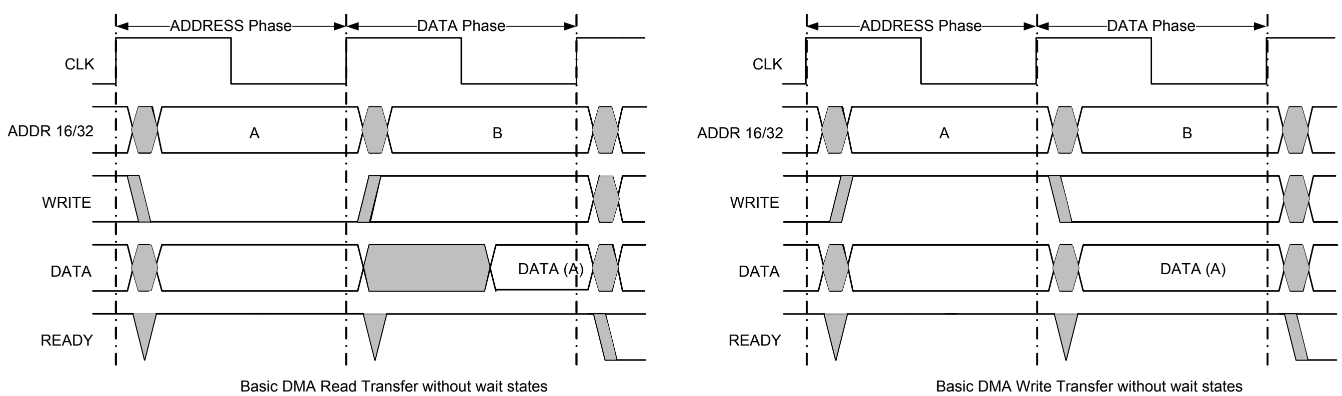
*4.4.4 Transaction Modes Supported*

The flexible configuration of each DMA channel and the ability to chain multiple channels allow the creation of both simple and complex use cases. General use cases include, but are not limited to:

*4.4.4.1 Simple DMA*

In a simple DMA case, a single TD transfers data between a source and sink (peripherals or memory location). The basic timing diagrams of DMA read and write cycles are shown in Figure 4-1. For more description on other transfer modes, refer to the Technical Reference Manual.

**Figure 4-1. DMA Timing Diagram**



# 5. Memory

## 5.1 Static RAM

CY8C34 SRAM is used for temporary data storage. Up to 8 KB of SRAM is provided and can be accessed by the 8051 or the DMA controller. See Memory Map on page 24. Simultaneous access of SRAM by the 8051 and the DMA controller is possible if different 4-KB blocks are accessed.

## 5.2 Flash Program Memory

Flash memory in PSoC devices provides nonvolatile storage for user firmware, user configuration data, bulk data storage, and optional ECC data. The main flash memory area contains up to 64 KB of user program space.

Up to an additional 8 KB of flash space is available for ECC. If ECC is not used this space can store device configuration data and bulk user data. User code may not be run out of the ECC flash memory section. ECC can correct one bit error and detect two bit errors per 8 bytes of firmware memory; an interrupt can be generated when an error is detected.

The CPU reads instructions located in flash through a cache controller. This improves instruction execution rate and reduces system power consumption by requiring less frequent flash access. The cache has 8 lines at 64 bytes per line for a total of 512 bytes. It is fully associative, automatically controls flash power, and can be enabled or disabled. If ECC is enabled, the cache controller also performs error checking and correction, and interrupt generation.

Flash programming is performed through a special interface and preempts code execution out of flash. The flash programming interface performs flash erasing, programming and setting code protection levels. Flash in-system serial programming (ISSP), typically used for production programming, is possible through both the SWD and JTAG interfaces. In-system programming, typically used for bootloaders, is also possible using serial interfaces such as $I^2C$, USB, UART, and SPI, or any communications protocol.

## 5.3 Flash Security

All PSoC devices include a flexible flash-protection model that prevents access and visibility to on-chip flash memory. This prevents duplication or reverse engineering of proprietary code. Flash memory is organized in blocks, where each block contains 256 bytes of program or data and 32 bytes of ECC or configuration data. A total of up to 256 blocks is provided on 64-KB flash devices.

The device offers the ability to assign one of four protection levels to each row of flash. Table 5-1 lists the protection modes available. Flash protection levels can only be changed by performing a complete flash erase. The Full Protection and Field Upgrade settings disable external access (through a debugging tool such as PSoC Creator, for example). If your application requires code update through a bootloader, then use the Field Upgrade setting. Use the Unprotected setting only when no security is needed in your application. The PSoC device also offers an advanced security feature called Device Security which permanently disables all test, programming, and debug ports, protecting your application from external access (see the “Device Security” section on page 63). For more information about how to take full advantage of the security features in PSoC, see the PSoC 3 TRM.

**Table 5-1. Flash Protection**

| Protection Setting | Allowed | Not Allowed |
|---|---|---|
| Unprotected | External read and write + internal read and write | – |
| Factory Upgrade | External write + internal read and write | External read |
| Field Upgrade | Internal read and write | External read and write |
| Full Protection | Internal read | External read and write + internal write |

**Disclaimer**

Note the following details of the flash code protection features on Cypress devices.

Cypress products meet the specifications contained in their particular Cypress data sheets. Cypress believes that its family of products is one of the most secure families of its kind on the market today, regardless of how they are used. There may be methods, unknown to Cypress, that can breach the code protection features. Any of these methods, to our knowledge, would be dishonest and possibly illegal. Neither Cypress nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as ‘unbreakable’. Cypress is willing to work with the customer who is concerned about the integrity of their code. Code protection is constantly evolving. We at Cypress are committed to continuously improving the code protection features of our products.

## 5.4 EEPROM

PSoC EEPROM memory is a byte-addressable nonvolatile memory. The CY8C34 has up to 2 KB of EEPROM memory to store user data. Reads from EEPROM are random access at the byte level. Reads are done directly; writes are done by sending write commands to an EEPROM programming interface. CPU code execution can continue from flash during EEPROM writes. EEPROM is erasable and writeable at the row level. The EEPROM is divided into 128 rows of 16 bytes each. The CPU can not execute out of EEPROM. There is no ECC hardware associated with EEPROM. If ECC is required it must be handled in firmware.

It can take as much as 20 milliseconds to write to EEPROM or flash. During this time the device should not be reset, or unexpected changes may be made to portions of EEPROM or flash. Reset sources (see Section 6.3.1) include XRES pin, software reset, and watchdog; care should be taken to make sure that these are not inadvertently activated. Also, the low voltage detect circuits should be configured to generate an interrupt instead of a reset.

*6.2.1 Power Modes*

PSoC 3 devices have four different power modes, as shown in Table 6-2 and Table 6-3. The power modes allow a design to easily provide required functionality and processing power while simultaneously minimizing power consumption and maximizing battery life in low-power and portable devices.

PSoC 3 power modes, in order of decreasing power consumption are:

- Active
- Alternate Active
- Sleep
- Hibernate

Active is the main processing mode. Its functionality is configurable. Each power controllable subsystem is enabled or disabled by using separate power configuration template registers. In alternate active mode, fewer subsystems are enabled, reducing power. In sleep mode most resources are disabled regardless of the template settings. Sleep mode is optimized to provide timed sleep intervals and Real Time Clock functionality. The lowest power mode is hibernate, which retains register and SRAM state, but no clocks, and allows wakeup only from I/O pins. Figure 6-5 on page 31 illustrates the allowable transitions between power modes. Sleep and hibernate modes should not be entered until all VDDIO supplies are at valid voltage levels.

**Table 6-2. Power Modes**

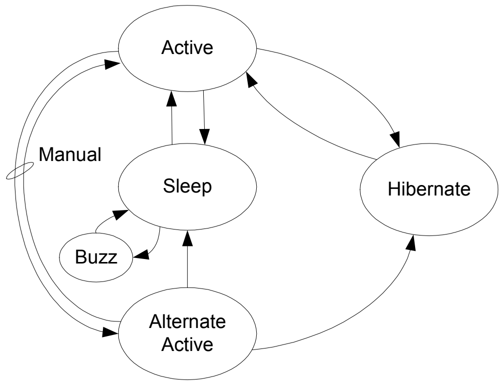
| Power Modes | Description | Entry Condition | Wakeup Source | Active Clocks | Regulator |
|---|---|---|---|---|---|
| Active | Primary mode of operation, all peripherals available (programmable) | Wakeup, reset, manual register entry | Any interrupt | Any (programmable) | All regulators available. Digital and analog regulators can be disabled if external regulation used. |
| Alternate Active | Similar to Active mode, and is typically configured to have fewer peripherals active to reduce power. One possible configuration is to use the UDBs for processing, with the CPU turned off | Manual register entry | Any interrupt | Any (programmable) | All regulators available. Digital and analog regulators can be disabled if external regulation used. |
| Sleep | All subsystems automatically disabled | Manual register entry | Comparator, PICU, $I^2C$, RTC, CTW, LVD | ILO/kHzECO | Both digital and analog regulators buzzed. Digital and analog regulators can be disabled if external regulation used. |
| Hibernate | All subsystems automatically disabled<br>Lowest power consuming mode with all peripherals and internal regulators disabled, except hibernate regulator is enabled<br>Configuration and memory contents retained | Manual register entry | PICU | | Only hibernate regulator active. |

**Table 6-3. Power Modes Wakeup Time and Power Consumption**

| Sleep Modes | Wakeup Time | Current (typ) | Code Execution | Digital Resources | Analog Resources | Clock Sources Available | Wakeup Sources | Reset Sources |
|---|---|---|---|---|---|---|---|---|
| Active | – | 1.2 mA[11] | Yes | All | All | All | – | All |
| Alternate Active | – | – | User defined | All | All | All | – | All |
| Sleep | <15 µs | 1 µA | No | $I^2C$ | Comparator | ILO/kHzECO | Comparator, PICU, $I^2C$, RTC, CTW, LVD | XRES, LVD, WDR |
| Hibernate | <100 µs | 200 nA | No | None | None | None | PICU | XRES |

**Note**
11. Bus clock off. Execute from cache at 6 MHz. See Table 11-2 on page 66.

**Figure 6-5. Power Mode Transitions**




*6.2.1.1 Active Mode*

Active mode is the primary operating mode of the device. When in active mode, the active configuration template bits control which available resources are enabled or disabled. When a resource is disabled, the digital clocks are gated, analog bias currents are disabled, and leakage currents are reduced as appropriate. User firmware can dynamically control subsystem power by setting and clearing bits in the active configuration template. The CPU can disable itself, in which case the CPU is automatically reenabled at the next wakeup event.

When a wakeup event occurs, the global mode is always returned to active, and the CPU is automatically enabled, regardless of its template settings. Active mode is the default global power mode upon boot.

*6.2.1.2 Alternate Active Mode*

Alternate Active mode is very similar to Active mode. In alternate active mode, fewer subsystems are enabled, to reduce power consumption. One possible configuration is to turn off the CPU and flash, and run peripherals at full speed.

*6.2.1.3 Sleep Mode*

Sleep mode reduces power consumption when a resume time of 15 µs is acceptable. The wake time is used to ensure that the regulator outputs are stable enough to directly enter active mode.

*6.2.1.4 Hibernate Mode*

In hibernate mode nearly all of the internal functions are disabled. Internal voltages are reduced to the minimal level to keep vital systems alive. Configuration state is preserved in hibernate mode and SRAM memory is retained. GPIOs configured as digital outputs maintain their previous values and external GPIO pin interrupt settings are preserved. The device can only return from hibernate mode in response to an external I/O interrupt. The resume time from hibernate mode is less than 100 µs.

To achieve an extremely low current, the hibernate regulator has limited capacity. This limits the frequency of any signal present on the input pins - no GPIO should toggle at a rate greater than 10 kHz while in hibernate mode. If pins must be toggled at a high rate while in a low power mode, use sleep mode instead.

*6.2.1.5 Wakeup Events*

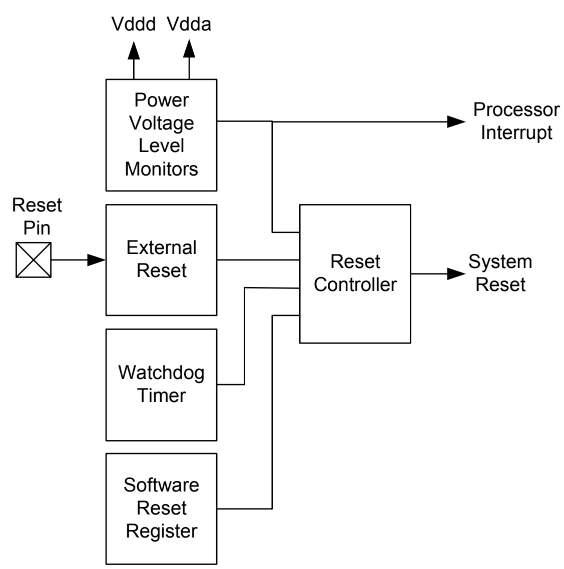
Wakeup events are configurable and can come from an interrupt or device reset. A wakeup event restores the system to active mode. Firmware enabled interrupt sources include internally generated interrupts, power supervisor, central timewheel, and I/O interrupts. Internal interrupt sources can come from a variety of peripherals, such as analog comparators and UDBs. The central timewheel provides periodic interrupts to allow the system to wake up, poll peripherals, or perform real-time functions. Reset event sources include the external reset I/O pin (XRES), WDT, and precision reset (PRES).

## 6.3 Reset

CY8C34 has multiple internal and external reset sources available. The reset sources are:

- Power source monitoring – The analog and digital power voltages, VDDA, VDDD, VCCA, and VCCD are monitored in several different modes during power up, active mode, and sleep mode (buzzing). If any of the voltages goes outside predetermined ranges then a reset is generated. The monitors are programmable to generate an interrupt to the processor under certain conditions before reaching the reset thresholds.
- External – The device can be reset from an external source by pulling the reset pin (XRES) low. The XRES pin includes an internal pull-up to VDDIO1. VDDD, VDDA, and VDDIO1 must all have voltage applied before the part comes out of reset.
- Watchdog timer – A watchdog timer monitors the execution of instructions by the processor. If the watchdog timer is not reset by firmware within a certain period of time, the watchdog timer generates a reset.
- Software – The device can be reset under program control.

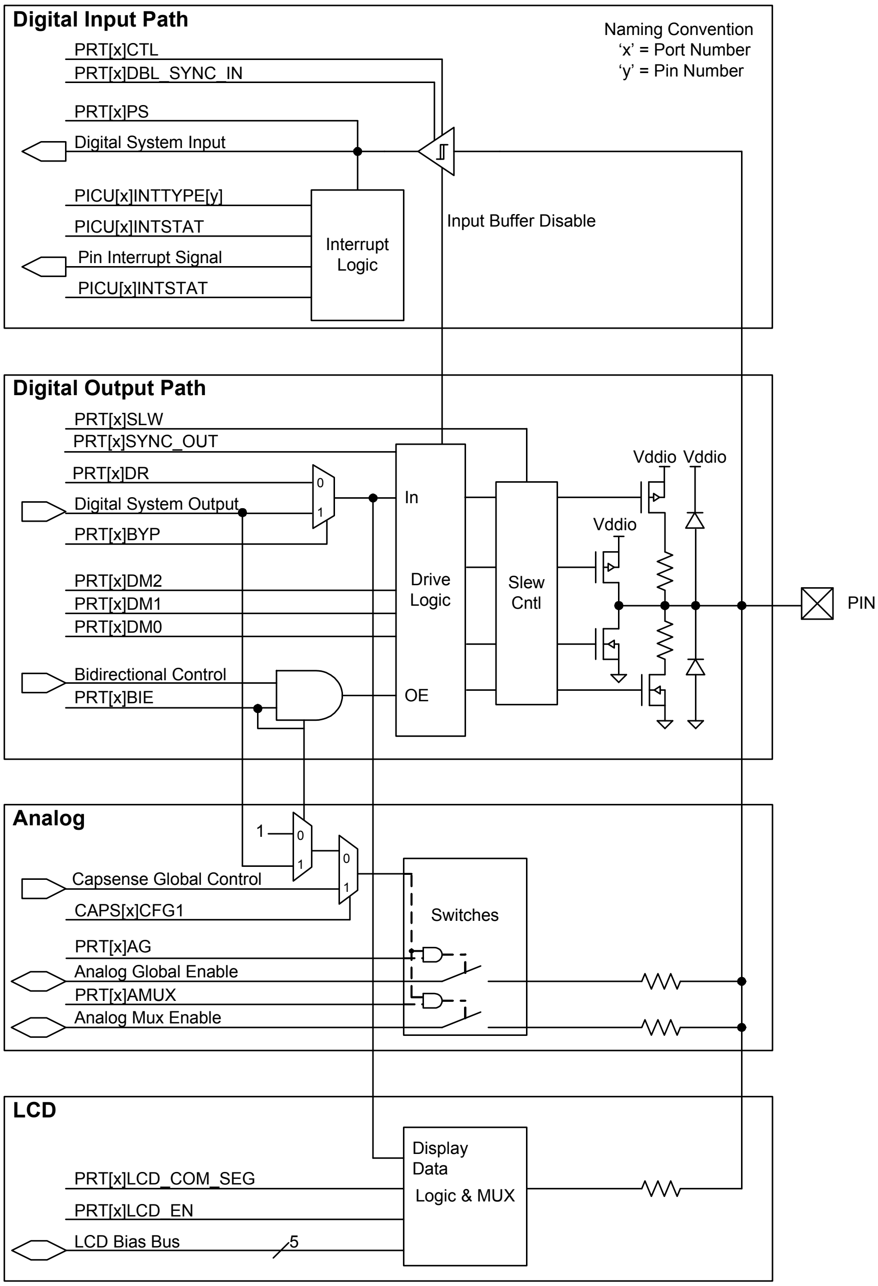
**Figure 6-6. Resets**




The term **device reset** indicates that the processor as well as analog and digital peripherals and registers are reset.

A reset status register shows some of the resets or power voltage monitoring interrupts. The program may examine this register to

**Figure 6-7. GPIO Block Diagram**



### 6.4.5 Pin Interrupts

All GPIO and SIO pins are able to generate interrupts to the system. All eight pins in each port interface to their own Port Interrupt Control Unit (PICU) and associated interrupt vector. Each pin of the port is independently configurable to detect rising edge, falling edge, both edge interrupts, or to not generate an interrupt.

Depending on the configured mode for each pin, each time an interrupt event occurs on a pin, its corresponding status bit of the interrupt status register is set to ‘1’ and an interrupt request is sent to the interrupt controller. Each PICU has its own interrupt vector in the interrupt controller and the pin status register providing easy determination of the interrupt source down to the pin level.

Port pin interrupts remain active in all sleep modes allowing the PSoC device to wake from an externally generated interrupt. While level sensitive interrupts are not directly supported; UDB provide this functionality to the system when needed.

### 6.4.6 Input Buffer Mode

GPIO and SIO input buffers can be configured at the port level for the default CMOS input thresholds or the optional LVTTL input thresholds. All input buffers incorporate Schmitt triggers for input hysteresis. Additionally, individual pin input buffers can be disabled in any drive mode.

### 6.4.7 I/O Power Supplies

Up to four I/O pin power supplies are provided depending on the device and package. Each I/O supply must be less than or equal to the voltage on the chip’s analog (VDDA) pin. This feature allows users to provide different I/O voltage levels for different pins on the device. Refer to the specific device package pinout to determine VDDIO capability for a given port and pin. The SIO port pins support an additional regulated high output capability, as described in Adjustable Output Level.

### 6.4.8 Analog Connections

These connections apply only to GPIO pins. All GPIO pins may be used as analog inputs or outputs. The analog voltage present on the pin must not exceed the VDDIO supply voltage to which the GPIO belongs. Each GPIO may connect to one of the analog global busses or to one of the analog mux buses to connect any pin to any internal analog resource such as ADC or comparators. In addition, select pins provide direct connections to specific analog features such as the high current DACs or uncommitted opamps.

### 6.4.9 CapSense

This section applies only to GPIO pins. All GPIO pins may be used to create CapSense buttons and sliders[14]. See the “CapSense” section on page 58 for more information.

### 6.4.10 LCD Segment Drive

This section applies only to GPIO pins. All GPIO pins may be used to generate Segment and Common drive signals for direct glass drive of LCD glass. See the “LCD Direct Drive” section on page 57 for details.

### 6.4.11 Adjustable Output Level

This section applies only to SIO pins. SIO port pins support the ability to provide a regulated high output level for interface to external signals that are lower in voltage than the SIO’s respective VDDIO. SIO pins are individually configurable to output either the standard VDDIO level or the regulated output, which is based on an internally generated reference. Typically a voltage DAC (VDAC) is used to generate the reference (see Figure 6-11). The “DAC” section on page 59 has more details on VDAC use and reference routing to the SIO pins. Resistive pullup and pull-down drive modes are not available with SIO in regulated output mode.

### 6.4.12 Adjustable Input Level

This section applies only to SIO pins. SIO pins by default support the standard CMOS and LVTTL input levels but also support a differential mode with programmable levels. SIO pins are grouped into pairs. Each pair shares a reference generator block which, is used to set the digital input buffer reference level for interface to external signals that differ in voltage from VDDIO. The reference sets the pins voltage threshold for a high logic level (see Figure 6-11). Available input thresholds are:

- $0.5 \times$ VDDIO
- $0.4 \times$ VDDIO
- $0.5 \times V_{REF}$
- $V_{REF}$

Typically a voltage DAC (VDAC) generates the $V_{REF}$ reference. “DAC” section on page 59 has more details on VDAC use and reference routing to the SIO pins.

**Note**

14. GPIOs with opamp outputs are not recommended for use with CapSense.

The opamp and resistor array is programmable to perform various analog functions including

- Naked operational amplifier – Continuous mode
- Unity-gain buffer – Continuous mode
- PGA – Continuous mode
- Transimpedance amplifier (TIA) – Continuous mode
- Up/down mixer – Continuous mode
- Sample and hold mixer (NRZ S/H) – Switched cap mode
- First order analog to digital modulator – Switched cap mode

### *8.5.1 Naked Opamp*

The Naked Opamp presents both inputs and the output for connection to internal or external signals. The opamp has a unity gain bandwidth greater than 6.0 MHz and output drive current up to 650 µA. This is sufficient for buffering internal signals (such as DAC outputs) and driving external loads greater than 7.5 kohms.

### *8.5.2 Unity Gain*

The Unity Gain buffer is a Naked Opamp with the output directly connected to the inverting input for a gain of 1.00. It has a –3 dB bandwidth greater than 6.0 MHz.

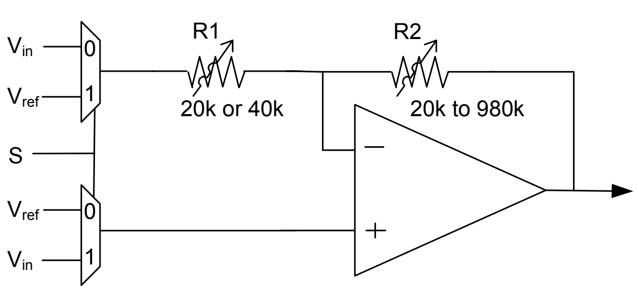
### *8.5.3 PGA*

The PGA amplifies an external or internal signal. The PGA can be configured to operate in inverting mode or noninverting mode. The PGA function may be configured for both positive and negative gains as high as 50 and 49 respectively. The gain is adjusted by changing the values of R1 and R2 as illustrated in Figure 8-8. The schematic in Figure 8-8 shows the configuration and possible resistor settings for the PGA. The gain is switched from inverting and non inverting by changing the shared select value of the both the input muxes. The bandwidth for each gain case is listed in Table 8-3.

**Table 8-3. Bandwidth**

| Gain | Bandwidth |
|---|---|
| 1 | 5.5 MHz |
| 24 | 340 kHz |
| 48 | 220 kHz |
| 50 | 215 kHz |

**Figure 8-8. PGA Resistor Settings**




The PGA is used in applications where the input signal may not be large enough to achieve the desired resolution in the ADC, or dynamic range of another SC/CT block such as a mixer. The gain is adjustable at runtime, including changing the gain of the PGA prior to each ADC sample.

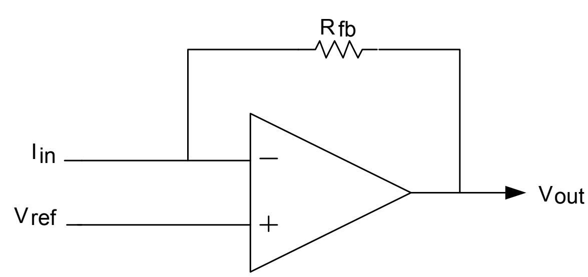
### *8.5.4 TIA*

The Transimpedance Amplifier (TIA) converts an internal or external current to an output voltage. The TIA uses an internal feedback resistor in a continuous time configuration to convert input current to output voltage. For an input current $I_{in}$, the output voltage is $V_{REF} - I_{in} \times R_{fb}$, where $V_{REF}$ is the value placed on the non inverting input. The feedback resistor Rfb is programmable between 20 KΩ and 1 MΩ through a configuration register. Table 8-4 shows the possible values of Rfb and associated configuration settings.

**Table 8-4. Feedback Resistor Settings**

| Configuration Word | Nominal $R_{fb}$ (KΩ) |
|---|---|
| 000b | 20 |
| 001b | 30 |
| 010b | 40 |
| 011b | 60 |
| 100b | 120 |
| 101b | 250 |
| 110b | 500 |
| 111b | 1000 |

**Figure 8-9. Continuous Time TIA Schematic**




The TIA configuration is used for applications where an external sensor's output is current as a function of some type of stimulus such as temperature, light, magnetic flux etc. In a common application, the voltage DAC output can be connected to the $V_{REF}$ TIA input to allow calibration of the external sensor bias current by adjusting the voltage DAC output voltage.

## 8.6 LCD Direct Drive

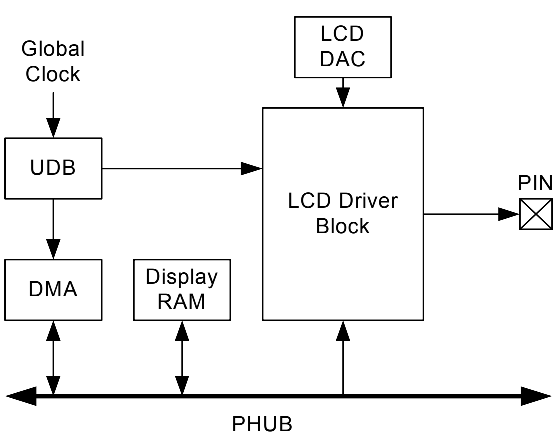
The PSoC LCD driver system is a highly configurable peripheral designed to allow PSoC to directly drive a broad range of LCD glass. All voltages are generated on chip, eliminating the need for external components. With a high multiplex ratio of up to 1/16, the CY8C34 family LCD driver system can drive a maximum of 736 segments. The PSoC LCD driver module was also designed with the conservative power budget of portable devices in mind, enabling different LCD drive modes and power down modes to conserve power.

PSoC Creator provides an LCD segment drive component. The component wizard provides easy and flexible configuration of LCD resources. You can specify pins for segments and commons along with other options. The software configures the device to meet the required specifications. This is possible because of the programmability inherent to PSoC devices.

Key features of the PSoC LCD segment system are:

- LCD panel direct driving
- Type A (standard) and Type B (low-power) waveform support
- Wide operating voltage range support (2 V to 5 V) for LCD panels
- Static, 1/2, 1/3, 1/4, 1/5 bias voltage levels
- Internal bias voltage generation through internal resistor ladder
- Up to 62 total common and segment outputs
- Up to 1/16 multiplex for a maximum of 16 backplane/common outputs
- Up to 62 front plane/segment outputs for direct drive
- Drives up to 736 total segments (16 backplane × 46 front plane)
- Up to 64 levels of software controlled contrast
- Ability to move display data from memory buffer to LCD driver through DMA (without CPU intervention)
- Adjustable LCD refresh rate from 10 Hz to 150 Hz
- Ability to invert LCD display for negative image
- Three LCD driver drive modes, allowing power optimization

**Figure 8-10. LCD System**




*8.6.1 LCD Segment Pin Driver*

Each GPIO pin contains an LCD driver circuit. The LCD driver buffers the appropriate output of the LCD DAC to directly drive the glass of the LCD. A register setting determines whether the pin is a common or segment. The pin's LCD driver then selects one of the six bias voltages to drive the I/O pin, as appropriate for the display data.

*8.6.2 Display Data Flow*

The LCD segment driver system reads display data and generates the proper output voltages to the LCD glass to produce the desired image. Display data resides in a memory buffer in the system SRAM. Each time you need to change the common and segment driver voltages, the next set of pixel data moves from the memory buffer into the Port Data Registers through the DMA.

*8.6.3 UDB and LCD Segment Control*

A UDB is configured to generate the global LCD control signals and clocking. This set of signals is routed to each LCD pin driver through a set of dedicated LCD global routing channels. In addition to generating the global LCD control signals, the UDB also produces a DMA request to initiate the transfer of the next frame of LCD data.

*8.6.4 LCD DAC*

The LCD DAC generates the contrast control and bias voltage for the LCD system. The LCD DAC produces up to five LCD drive voltages plus ground, based on the selected bias ratio. The bias voltages are driven out to GPIO pins on a dedicated LCD bias bus, as required.

## 8.7 CapSense

The CapSense system provides a versatile and efficient means for measuring capacitance in applications such as touch sense buttons, sliders, proximity detection, etc. The CapSense system uses a configuration of system resources, including a few hardware functions primarily targeted for CapSense. Specific resource usage is detailed in the CapSense component in PSoC Creator.

A capacitive sensing method using a Delta-sigma Modulator (CSD) is used. It provides capacitance sensing using a switched capacitor technique with a delta-sigma modulator to convert the sensing current to a digital code.

## 8.8 Temp Sensor

Die temperature is used to establish programming parameters for writing flash. Die temperature is measured using a dedicated sensor based on a forward biased transistor. The temperature sensor has its own auxiliary ADC.

**Table 11-2. DC Specifications** *(continued)*

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Idd[23, 24] | **Active Mode, VDD = 1.71 V - 5.5 V** | | | | | |
| | Execute from CPU instruction buffer, see Flash Program Memory on page 21 | | | | | |
| | CPU at 3 MHz | T = –40 °C | – | 1.3 | – | mA |
| | | T = 25 °C | – | 1.6 | – | mA |
| | | T = 85 °C | – | 4.8 | – | mA |
| | | T = 125 °C | – | 4.9 | – | mA |
| | CPU at 6 MHz | T = –40 °C | – | 2.1 | – | mA |
| | | T = 25 °C | – | 2.3 | – | mA |
| | | T = 85 °C | – | 5.6 | – | mA |
| | | T = 125 °C | – | 5.8 | – | mA |
| | CPU at 12 MHz | T = –40 °C | – | 3.5 | – | mA |
| | | T = 25 °C | – | 3.8 | – | mA |
| | | T = 85 °C | – | 7.1 | – | mA |
| | | T = 125 °C | – | 9.0 | – | mA |
| | CPU at 24 MHz | T = –40 °C | – | 6.3 | – | mA |
| | | T = 25 °C | – | 6.6 | – | mA |
| | | T = 85 °C | – | 10 | – | mA |
| | | T = 125 °C | – | 15.8 | – | mA |
| | CPU at 48 MHz | T = –40 °C | – | 11.5 | – | mA |
| | | T = 25 °C | – | 12 | – | mA |
| | | T = 85 °C | – | 15.5 | – | mA |
| | | T = 125 °C | – | 21.7 | – | mA |
| | CPU at 62 MHz | T = –40 °C | – | 16 | – | mA |
| | | T = 25 °C | – | 16 | – | mA |
| | | T = 85 °C | – | 19.5 | – | mA |
| | | T = 125 °C | – | 27.8 | – | mA |

**Notes**

23. The current consumption of additional peripherals that are implemented only in programmed logic blocks can be found in their respective data sheets, available in PSoC Creator, the integrated design environment. To compute total current, find CPU current at frequency of interest and add peripheral currents for your particular system from the device data sheet and component data sheets.
24. Total current for all power domains: digital ($I_{DDD}$), analog ($I_{DDA}$), and I/Os ($I_{DDIO0, 1, 2, 3}$). All I/Os floating.

**Table 11-18. Delta-sigma ADC AC Specifications**

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| | Startup time | | – | – | 4 | Samples |
| THD | Total harmonic distortion[37] | Buffer gain = 1, 16 bit, Range = ±1.024 V | – | – | 0.0040 | % |
| **12-Bit Resolution Mode** | | | | | | |
| SR12 | Sample rate, continuous, high power[37] | Range = ±1.024 V, unbuffered | 4 | – | 192 | ksps |
| BW12 | Input bandwidth at max sample rate[37] | Range = ±1.024 V, unbuffered | – | 44 | – | kHz |
| SINAD12int | Signal to noise ratio, 12-bit, internal reference[37] | Range = ±1.024 V, unbuffered | 66 | – | – | dB |
| **8-Bit Resolution Mode** | | | | | | |
| SR8 | Sample rate, continuous, high power[37] | Range = ±1.024 V, unbuffered | 8 | – | 384 | ksps |
| BW8 | Input bandwidth at max sample rate[37] | Range = ±1.024 V, unbuffered | – | 88 | – | kHz |
| SINAD8int | Signal to noise ratio, 8-bit, internal reference[37] | Range = ±1.024 V, unbuffered | 43 | – | – | dB |

**Table 11-19. Delta-sigma ADC Sample Rates, Range = ±1.024 V**

| Resolution, Bits | Continuous | | Multi-Sample | | Multi-Sample Turbo | |
|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max |
| 8 | 8000 | 384000 | 1911 | 91701 | 1829 | 87771 |
| 9 | 6400 | 307200 | 1543 | 74024 | 1489 | 71441 |
| 10 | 5566 | 267130 | 1348 | 64673 | 1307 | 62693 |
| 11 | 4741 | 227555 | 1154 | 55351 | 1123 | 53894 |
| 12 | 4000 | 192000 | 978 | 46900 | 956 | 45850 |

**Figure 11-31. IDAC INL vs Temperature, Range = 255 µA, High speed mode**

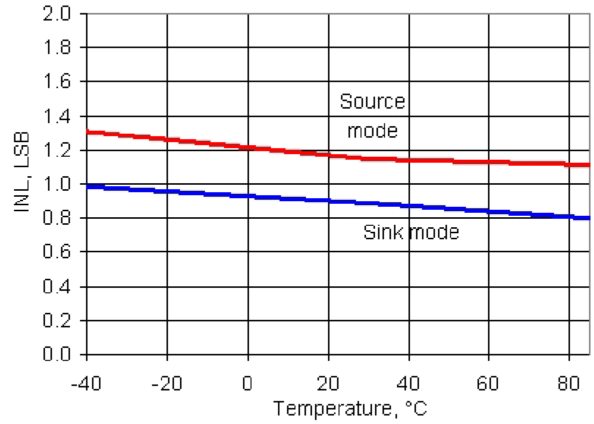



**Figure 11-32. IDAC DNL vs Temperature, Range = 255 µA, High speed mode**

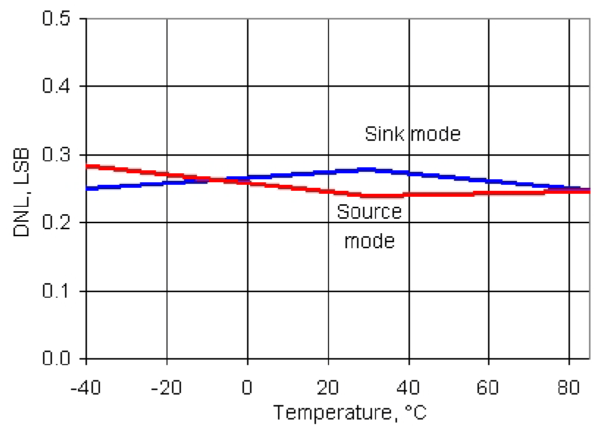



**Figure 11-33. IDAC Full Scale Error vs Temperature, Range = 255 µA, Source Mode**

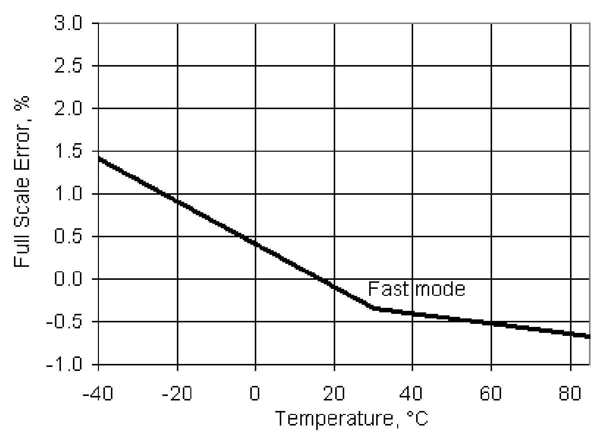


**Figure 11-51. VDAC PSRR vs Frequency**

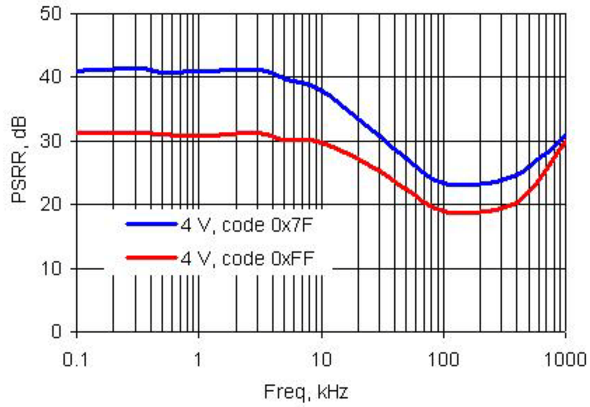
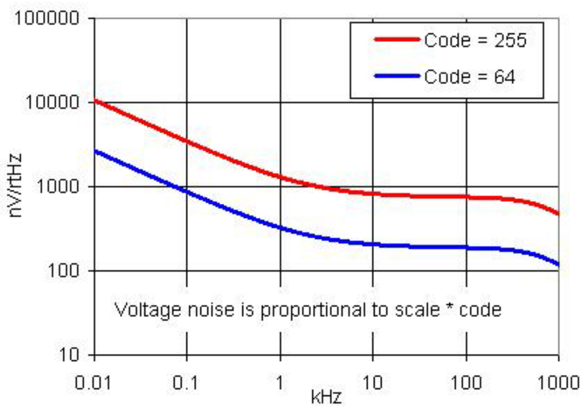



**Figure 11-52. VDAC Voltage Noise, 1 V Mode, High speed mode, Vdda = 5 V**



### 11.6 Digital Peripherals

Specifications are valid for -40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

#### *11.6.1 Timer*

**Table 11-37. Timer DC Specifications**

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| | Block current consumption | 16-bit timer, at listed input clock frequency | – | – | – | µA |
| | 3 MHz | | – | 15 | – | µA |
| | 12 MHz | | – | 60 | – | µA |
| | 50 MHz | | – | 260 | – | µA |

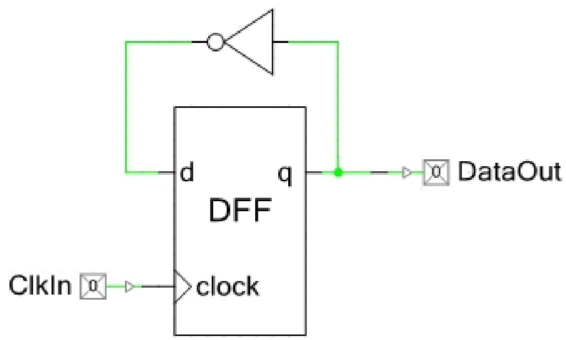
**Table 11-38. Timer AC Specifications**

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| | Operating frequency | -40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C | DC | - | 50 [45] | MHz |
| | | -40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C | DC | - | 50 | MHz |
| | Capture pulse width (Internal) | -40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C | 15 | - | - | ns |
| | | -40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C | 21 | - | - | ns |
| | Capture pulse width (external) | -40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C | 30 | - | - | ns |
| | | -40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C | 42 | - | - | ns |
| | Timer resolution | -40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C | 15 | - | - | ns |
| | | -40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C | 21 | - | - | ns |
| | Enable pulse width | -40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C | 15 | - | - | ns |
| | | -40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C | 21 | - | - | ns |
| | Enable pulse width (external) | -40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C | 30 | - | - | ns |
| | | -40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C | 42 | - | - | ns |
| | Reset pulse width | -40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C | 15 | - | - | ns |
| | | -40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C | 21 | - | - | ns |
| | Reset pulse width (external) | -40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C | 30 | - | - | ns |
| | | -40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C | 42 | - | - | ns |

**Note**

45. Applicable at -40°C to 85°C; 50 MHz at -40°C to 125°C.

**Figure 11-55. Clock to Output Performance**



### 11.8 PSoC System Resources

Specifications are valid for -40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

#### 11.8.1 POR with Brown Out

For brown out detect in regulated mode, Vddd and Vdda must be ≥ 2.0 V. Brown out detect is available in externally regulated mode.

**Table 11-61. Precise Power On Reset (PRES) with Brown Out DC Specifications**

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| PRESR | Rising trip voltage | Factory trim | 1.64 | – | 1.68 | V |
| PRESF | Falling trip voltage | | 1.62 | – | 1.66 | V |

**Table 11-62. Precise Power On Reset (PRES) with Brown Out AC Specifications**

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| PRES_TR | Response time | | – | – | 0.5 | µs |
| | $V_{DDD}/V_{DDA}$ droop rate | Sleep mode | – | 5 | – | V/sec |

#### 11.8.2 Voltage Monitors

**Table 11-63. Voltage Monitors DC Specifications**

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| LVI | Trip voltage | | | | | |
| | LVI_A/D_SEL[3:0] = 0000b | | 1.68 | 1.73 | 1.77 | V |
| | LVI_A/D_SEL[3:0] = 0001b | | 1.89 | 1.95 | 2.01 | V |
| | LVI_A/D_SEL[3:0] = 0010b | | 2.14 | 2.20 | 2.27 | V |
| | LVI_A/D_SEL[3:0] = 0011b | | 2.38 | 2.45 | 2.53 | V |
| | LVI_A/D_SEL[3:0] = 0100b | | 2.62 | 2.71 | 2.79 | V |
| | LVI_A/D_SEL[3:0] = 0101b | | 2.87 | 2.95 | 3.04 | V |
| | LVI_A/D_SEL[3:0] = 0110b | | 3.11 | 3.21 | 3.31 | V |
| | LVI_A/D_SEL[3:0] = 0111b | | 3.35 | 3.46 | 3.56 | V |
| | LVI_A/D_SEL[3:0] = 1000b | | 3.59 | 3.70 | 3.81 | V |
| | LVI_A/D_SEL[3:0] = 1001b | | 3.84 | 3.95 | 4.07 | V |
| | LVI_A/D_SEL[3:0] = 1010b | | 4.08 | 4.20 | 4.33 | V |
| | LVI_A/D_SEL[3:0] = 1011b | | 4.32 | 4.45 | 4.59 | V |
| | LVI_A/D_SEL[3:0] = 1100b | | 4.56 | 4.70 | 4.84 | V |
| | LVI_A/D_SEL[3:0] = 1101b | | 4.83 | 4.98 | 5.13 | V |
| | LVI_A/D_SEL[3:0] = 1110b | | 5.05 | 5.21 | 5.37 | V |
| | LVI_A/D_SEL[3:0] = 1111b | | 5.30 | 5.47 | 5.63 | V |
| HVI | Trip voltage | | 5.57 | 5.75 | 5.92 | V |

**Table 11-64. Voltage Monitors AC Specifications**

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| | Response time[57] | | – | – | 1 | µs |

**Note**
57. Based on device characterization (Not production tested).

**Table 11-70. IMO AC Specifications**

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $F_{IMO}$ | IMO frequency stability (with factory trim) | | | | | |
| | 62.6 MHz | | –7 | – | 7 | % |
| | 48 MHz | | –5 | – | 5 | % |
| | 24 MHz – Non USB mode | | –4 | – | 4 | % |
| | 24 MHz – USB mode | With oscillator locking to USB bus | –0.25 | – | 0.25 | % |
| | 12 MHz | | –3 | – | 3 | % |
| | 6 MHz | | –2 | – | 2 | % |
| | 3 MHz | | –2 | – | 2 | % |
| | Startup time[60] | From enable (during normal system operation) | – | – | 13 | µs |
| Jp–p | Jitter (peak to peak)[60] | | | | | |
| | F = 24 MHz | | – | 0.9 | – | ns |
| | F = 3 MHz | | – | 1.6 | – | ns |
| Jperiod | Jitter (long term)[60] | | | | | |
| | F = 24 MHz | | – | 0.9 | – | ns |
| | F = 3 MHz | | – | 12 | – | ns |

**Note**
60. Based on device characterization (Not production tested).

### 11.9.3 External Crystal Oscillator

**Table 11-73. 32 kHz External Crystal DC Specifications[63]**

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Icc | Operating current | Low power mode; $C_L$ = 6 pF;<br>-40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C | – | 0.25 | 1.0 | µA |
| DL | Drive level | Low-power mode; $C_L$ = 6 pF | – | – | 1 | µW |

**Table 11-74. 32 kHz External Crystal AC Specifications**

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| F | Frequency | | – | 32.768 | – | kHz |
| Ton | Startup time | High power mode | – | 1 | – | s |

**Table 11-75. MHz ECO AC Specifications**

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| F | Crystal frequency range | | 4 | – | 25 | MHz |

### 11.9.4 External Clock Reference

**Table 11-76. External Clock Reference AC Specifications**

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| | External frequency range | | 0 | – | 33 | MHz |
| | Input duty cycle range | Measured at $V_{DDIO}/2$ | 30 | 50 | 70 | % |
| | Input edge rate | $V_{IL}$ to $V_{IH}$ | 0.51 | – | – | V/ns |

### 11.9.5 Phase-Locked Loop

**Table 11-77. PLL DC Specifications**

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $I_{DD}$ | PLL operating current | In = 3 MHz, Out = 24 MHz | – | 200 | – | µA |

**Table 11-78. PLL AC Specifications**

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Fpllin | PLL input frequency[64] | Output of Prescalar | 1 | - | 48 | MHz |
| | PLL intermediate frequency[65] | | 1 | - | 3 | MHz |
| Fpllout | PLL output frequency[64] | -40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C | 24 | - | 50 | MHz |
| | | -40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C | 24 | - | 50 | MHz |
| | Lock time at startup | | - | - | 250 | µs |
| Jperiod-rms | Jitter (rms)[29] | -40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C | - | - | 250 | ps |
| | | -40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C | - | - | 400 | ps |

**Notes**

63. Based on device characterization (not production tested).
64. This specification is guaranteed by testing the PLL across the specified range using the IMO as the source for the PLL.
65. PLL input divider, Q, must be set so that the input frequency is divided down to the intermediate frequency range. Value for Q ranges from 1 to 16.

# 16. Document Conventions

## 16.1 Units of Measure

**Table 16-1. Units of Measure**

| Symbol | Unit of Measure |
|---|---|
| °C | degrees Celsius |
| dB | decibels |
| fF | femtofarads |
| Hz | hertz |
| KB | 1024 bytes |
| kbps | kilobits per second |
| Khr | kilohours |
| kHz | kilohertz |
| kΩ | kilohms |
| ksps | kilosamples per second |
| LSB | least significant bit |
| Mbps | megabits per second |
| MHz | megahertz |
| MΩ | megaohms |
| Msps | megasamples per second |
| µA | microamperes |
| µF | microfarads |
| µH | microhenrys |
| µs | microseconds |
| µV | microvolts |
| µW | microwatts |
| mA | milliamperes |
| ms | milliseconds |
| mV | millivolts |
| nA | nanoamperes |
| ns | nanoseconds |
| nV | nanovolts |
| Ω | ohms |
| pF | picofarads |
| ppm | parts per million |
| ps | picoseconds |
| s | seconds |
| sps | samples per second |
| sqrtHz | square root of hertz |
| V | volts |

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