**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | 8051 |
| Core Size | 8-Bit |
| Speed | 50MHz |
| Connectivity | CANbus, EBI/EMI, I²C, LINbus, SPI, UART/USART |
| Peripherals | CapSense, DMA, LCD, POR, PWM, WDT |
| Number of I/O | 25 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 2K x 8 |
| RAM Size | 8K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.71V ~ 5.5V |
| Data Converters | A/D 16x12b; D/A 2x8b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 48-BSSOP (0.295", 7.50mm Width) |
| Supplier Device Package | 48-SSOP |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/cy8c3446pve-102 |

It also contains a separate, very low-power internal low-speed oscillator (ILO) for the sleep and watchdog timers. A 32.768-kHz external watch crystal is also supported for use in real-time clock (RTC) applications. The clocks, together with programmable clock dividers, provide the flexibility to integrate most timing requirements.

The CY8C34 family supports a wide supply operating range from 1.71 V to 5.5 V. This allows operation from regulated supplies such as 1.8 V ± 5%, 2.5 V ±10%, 3.3 V ± 10%, or 5.0 V ± 10%, or directly from a wide range of battery types.

PSoC supports a wide range of low-power modes. These include a 200-nA hibernate mode with RAM retention and a 1-µA sleep mode with RTC. In the second mode, the optional 32.768-kHz watch crystal runs continuously and maintains an accurate RTC.

Power to all major functional blocks, including the programmable digital and analog peripherals, can be controlled independently by firmware. This allows low-power background processing when some peripherals are not in use. This, in turn, provides a total device current of only 1.2 mA when the CPU is running at 6 MHz, or 0.8 mA running at 3 MHz.

The details of the PSoC power modes are covered in the "Power System" section on page 29 of this data sheet.

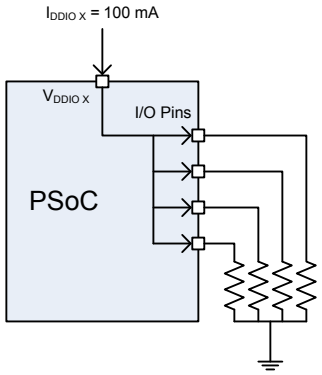
PSoC uses JTAG (4-wire) or SWD (2-wire) interfaces for programming, debug, and test. The 1-wire SWV may also be used for 'printf' style debugging. By combining SWD and SWV, you can implement a full debugging interface with just three pins. Using these standard interfaces you can debug or program the PSoC with a variety of hardware solutions from Cypress or third party vendors. PSoC supports on-chip break points and 4-KB instruction and data race memory for debug. Details of the programming, test, and debugging interfaces are discussed in the "Programming, Debug Interfaces, Resources" section on page 60 of this data sheet.

## 2. Pinouts

Each VDDIO pin powers a specific set of I/O pins. (The USBIOs are powered from VDDD.) Using the VDDIO pins, a single PSoC can support multiple voltage levels, reducing the need for off-chip level shifters. The black lines drawn on the pinout diagrams in Figure 2-3 through Figure 2-4 show the pins that are powered by each VDDIO.

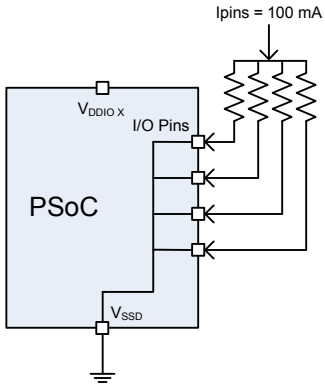
Each VDDIO may source up to 100 mA [7] total to its associated I/O pins, as shown in Figure 2-1.

**Figure 2-1. VDDIO Current Limit**




Conversely, for the 100-pin and 68-pin devices, the set of I/O pins associated with any VDDIO may sink up to 100 mA [7] total, as shown in Figure 2-2.

**Figure 2-2. I/O Pins Current Limit**




For the 48-pin devices, the set of I/O pins associated with VDDIO0 plus VDDIO2 may sink up to 100 mA [7] total. The set of I/O pins associated with VDDIO1 plus VDDIO3 may sink up to a total of 100 mA.

**Note**
7. The 100 mA source/ sink current per Vddio is valid only for temperature range of –40 °C to +85 °C. For extended temperature range of –40 °C to +125 °C, the maximum source or sink current per Vddio is 40 mA.

### 5.7.4 XData Space Access SFRs

The 8051 core features dual DPTR registers for faster data transfer operations. The data pointer select SFR, DPS, selects which data pointer register, DPTR0 or DPTR1, is used for the following instructions:

- MOVX @DPTR, A
- MOVX A, @DPTR
- MOVC A, @A+DPTR
- JMP @A+DPTR
- INC DPTR
- MOV DPTR, #data16

The extended data pointer SFRs, DPX0, DPX1, MXAX, and P2AX, hold the most significant parts of memory addresses during access to the xdata space. These SFRs are used only with the MOVX instructions.

During a MOVX instruction using the DPTR0/DPTR1 register, the most significant byte of the address is always equal to the contents of DPX0/DPX1.

During a MOVX instruction using the R0 or R1 register, the most significant byte of the address is always equal to the contents of MXAX, and the next most significant byte is always equal to the contents of P2AX.

### 5.7.5 I/O Port SFRs

The I/O ports provide digital input sensing, output drive, pin interrupts, connectivity for analog inputs and outputs, LCD, and access to peripherals through the DSI. Full information on I/O ports is found in I/O System and Routing on page 33.

I/O ports are linked to the CPU through the PHUB and are also available in the SFRs. Using the SFRs allows faster access to a limited set of I/O port registers, while using the PHUB allows boot configuration and access to all I/O port registers.

Each SFR supported I/O port provides three SFRs:

- SFRPRTxDR sets the output data state of the port (where × is port number and includes ports 0–6, 12 and 15).
- The SFRPRTxSEL selects whether the PHUB PRTxDR register or the SFRPRTxDR controls each pin's output buffer within the port. If a SFRPRTxSEL[y] bit is high, the corresponding SFRPRTxDR[y] bit sets the output state for that pin. If a SFRPRTxSEL[y] bit is low, the corresponding PRTxDR[y] bit sets the output state of the pin (where y varies from 0 to 7).
- The SFRPRTxPS is a read only register that contains pin state values of the port pins.

#### 5.7.5.1 xdata Space

The 8051 xdata space is 24-bit, or 16 MB in size. The majority of this space is not 'external'—it is used by on-chip components. See Table 5-5. External, that is, off-chip, memory can be accessed using the EMIF. See External Memory Interface on page 23.

**Table 5-5. XDATA Data Address Map**

| Address Range | Purpose |
|---|---|
| 0×00 0000 – 0×00 1FFF | SRAM |
| 0×00 4000 – 0×00 42FF | Clocking, PLLs, and oscillators |
| 0×00 4300 – 0×00 43FF | Power management |
| 0×00 4400 – 0×00 44FF | Interrupt controller |
| 0×00 4500 – 0×00 45FF | Ports interrupt control |
| 0×00 4700 – 0×00 47FF | Flash programming interface |
| 0×00 4800 - 0×00 48FF | Cache controller |
| 0×00 4900 – 0×00 49FF | $I^2C$ controller |
| 0×00 4E00 – 0×00 4EFF | Decimator |
| 0×00 4F00 – 0×00 4FFF | Fixed timer/counter/PWMs |
| 0×00 5000 – 0×00 51FF | I/O ports control |
| 0×00 5400 – 0×00 54FF | EMIF control registers |
| 0×00 5800 – 0×00 5FFF | Analog subsystem interface |
| 0×00 6000 – 0×00 60FF | USB controller |
| 0×00 6400 – 0×00 6FFF | UDB Working Registers |
| 0×00 7000 – 0×00 7FFF | PHUB configuration |
| 0×00 8000 – 0×00 8FFF | EEPROM |
| 0×00 A000 – 0×00 A400 | CAN |
| 0×00 C000 – 0×00 C800 | Reserved |
| 0×01 0000 – 0×01 FFFF | Digital Interconnect configuration |
| 0×05 0220 – 0×05 02F0 | Debug controller |
| 0×08 0000 – 0×08 1FFF | Flash ECC bytes |
| 0×80 0000 – 0×FF FFFF | External memory interface |

# 6. System Integration

## 6.1 Clocking System

The clocking system generates, divides, and distributes clocks throughout the PSoC system. For the majority of systems, no external crystal is required. The IMO and PLL together can generate up to a 50 MHz clock, accurate to ±1 percent over voltage and temperature. Additional internal and external clock sources allow each design to optimize accuracy, power, and cost. Any of the clock sources can be used to generate other clock frequencies in the 16-bit clock dividers and UDBs for anything the user wants, for example a UART baud rate generator.

Clock generation and distribution is automatically configured through the PSoC Creator IDE graphical interface. This is based on the complete system's requirements. It greatly speeds the design process. PSoC Creator allows you to build clocking systems with minimal input. You can specify desired clock frequencies and accuracies, and the software locates or builds a clock that meets the required specifications. This is possible because of the programmability inherent in PSoC.

Key features of the clocking system include:

- Seven general purpose clock sources
  - 3- to 62-MHz IMO, ±1% at 3 MHz
  - 4- to 25-MHz external crystal oscillator (MHzECO)
  - Clock doubler provides a doubled clock frequency output for the USB block, see USB Clock Domain on page 28.
  - DSI signal from an external I/O pin or other logic
  - 24- to 50-MHz fractional PLL sourced from IMO, MHzECO, or DSI
  - 1-kHz, 33-kHz, 100-kHz ILO for WDT and sleep timer
  - 32.768-kHz external crystal oscillator (kHzECO) for RTC
- IMO has a USB mode that auto locks to the USB bus clock requiring no external crystal for USB (USB equipped parts only)
- Independently sourced clock in all clock dividers
- Eight 16-bit clock dividers for the digital system
- Four 16-bit clock dividers for the analog system
- Dedicated 16-bit divider for the bus clock
- Dedicated 4-bit divider for the CPU clock
- Automatic clock configuration in PSoC Creator

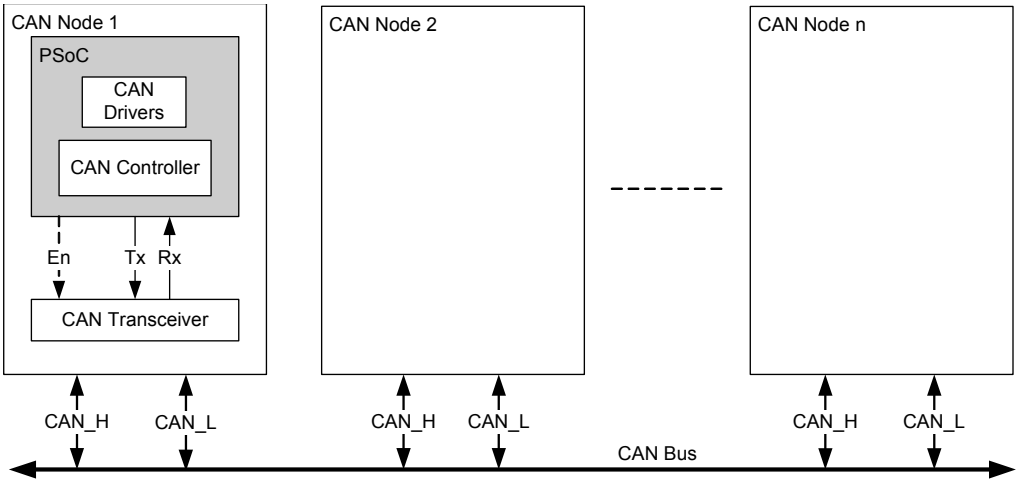
**Table 6-1. Oscillator Summary**

| Source | Fmin | Tolerance at Fmin | Fmax | Tolerance at Fmax | Startup Time |
|---|---|---|---|---|---|
| IMO | 3 MHz | ±1% over voltage and temperature | 62 MHz | ±7% | 13 µs max |
| MHzECO | 4 MHz | Crystal dependent | 25 MHz | Crystal dependent | 5 ms typ, max is crystal dependent |
| DSI | 0 MHz | Input dependent | 50 MHz | Input dependent | Input dependent |
| PLL | 24 MHz | Input dependent | 50 MHz | Input dependent | 250 µs max |
| Doubler | 48 MHz | Input dependent | 48 MHz | Input dependent | 1 µs max |
| ILO | 1 kHz | –50%, +100% | 100 kHz | –55%, +100% | 15 ms max in lowest power mode |
| kHzECO | 32 kHz | Crystal dependent | 32 kHz | Crystal dependent | 500 ms typ, max is crystal dependent |

## 7.5 CAN

The CAN peripheral is a fully functional controller area network (CAN) supporting communication baud rates up to 1 Mbps. The CAN controller implements the CAN2.0A and CAN2.0B specifications as defined in the Bosch specification and conforms to the ISO-11898-1 standard. The CAN protocol was originally designed for automotive applications with a focus on a high level of fault detection. This ensures high communication reliability at a low cost. Because of its success in automotive applications, CAN is used as a standard communication protocol for motion oriented machine control networks (CANOpen) and factory automation applications (DeviceNet). The CAN controller features allow the efficient implementation of higher level protocols without affecting the performance of the microcontroller CPU. Full configuration support is provided in PSoC Creator.

**Figure 7-14. CAN Bus System Implementation**




### *7.5.1 CAN Features*

- CAN2.0A/B protocol implementation – ISO 11898 compliant
  - Standard and extended frames with up to 8 bytes of data per frame
  - Message filter capabilities
  - Remote Transmission Request (RTR) support
  - Programmable bit rate up to 1 Mbps
- Listen Only mode
- SW readable error counter and indicator
- Sleep mode: Wake the device from sleep with activity on the Rx pin
- Supports two or three wire interface to external transceiver (Tx, Rx, and Enable). The three-wire interface is compatible with the Philips PHY; the PHY is not included on-chip. The three wires can be routed to any I/O
- Enhanced interrupt controller
  - CAN receive and transmit buffers status
  - CAN controller error status including BusOff
- Receive path
  - 16 receive buffers each with its own message filter
  - Enhanced hardware message filter implementation that covers the ID, IDE, and RTR
  - DeviceNet addressing support
  - Multiple receive buffers linkable to build a larger receive message array
  - Automatic transmission request (RTR) response handler
  - Lost received message notification
- Transmit path
  - Eight transmit buffers
  - Programmable transmit priority
  - Round robin
  - Fixed priority
  - Message transmissions abort capability

### *7.5.2 Software Tools Support*

CAN Controller configuration integrated into PSoC Creator:

- CAN Configuration walkthrough with bit timing analyzer
- Receive filter setup

## 7.8 I²C

The I²C peripheral provides a synchronous two wire interface designed to interface the PSoC device with a two wire I²C serial communication bus. It is compatible[15] with I²C Standard-mode, Fast-mode, and Fast-mode Plus devices as defined in the NXP I2C-bus specification and user manual (UM10204). The I2C bus I/O may be implemented with GPIO or SIO in open-drain modes. Additional I²C interfaces can be instantiated using Universal Digital Blocks (UDBs) in PSoC Creator, as required.

To eliminate the need for excessive CPU intervention and overhead, I²C specific support is provided for status detection and generation of framing bits. I²C operates as a slave, a master, or multimaster (Slave and Master).[16]. In slave mode, the unit always listens for a start condition to begin sending or receiving data. Master mode supplies the ability to generate the Start and Stop conditions and initiate transactions. Multimaster mode provides clock synchronization and arbitration to allow multiple masters on the same bus. If Master mode is enabled and Slave mode is not enabled, the block does not generate interrupts on externally generated Start conditions. I²C interfaces through DSI routing and allows direct connections to any GPIO or SIO pins.

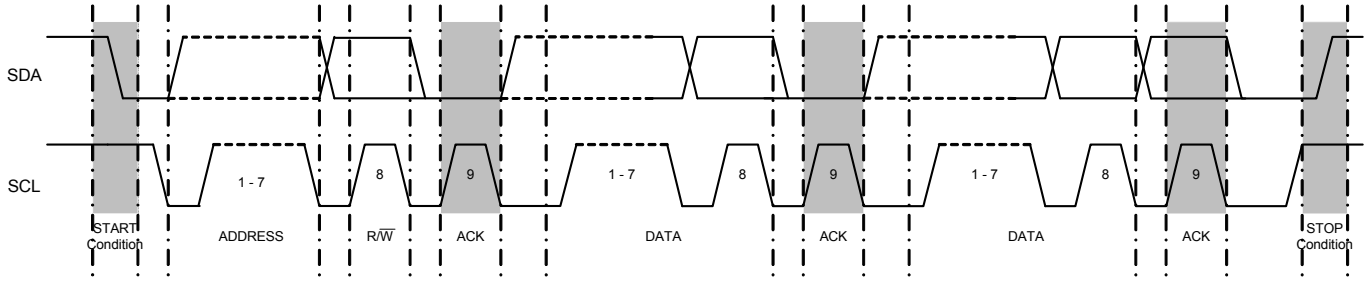
I²C provides hardware address detect of a 7-bit address without CPU intervention. Additionally the device can wake from low-power modes on a 7-bit hardware address match. If wakeup functionality is required, I²C pin connections are limited to the two special sets of SIO pins.

I²C features include:

- Slave and master, transmitter, and receiver operation
- Byte processing for low CPU overhead
- Interrupt or polling CPU interface
- Support for bus speeds up to 1 Mbps
- 7 or 10-bit addressing (10-bit addressing requires firmware support)
- SMBus operation (through firmware support - SMBus supported in hardware in UDBs)
- 7-bit hardware address compare
- Wake from low-power modes on address match
- Glitch filtering (active and alternate-active modes only)

Data transfers follow the format shown in Figure 7-18. After the START condition (S), a slave address is sent. This address is 7 bits long followed by an eighth bit which is a data direction bit (R/W) - a 'zero' indicates a transmission (WRITE), a 'one' indicates a request for data (READ). A data transfer is always terminated by a STOP condition (P) generated by the master.

**Figure 7-18. I²C Complete Transfer Timing**




**Notes**

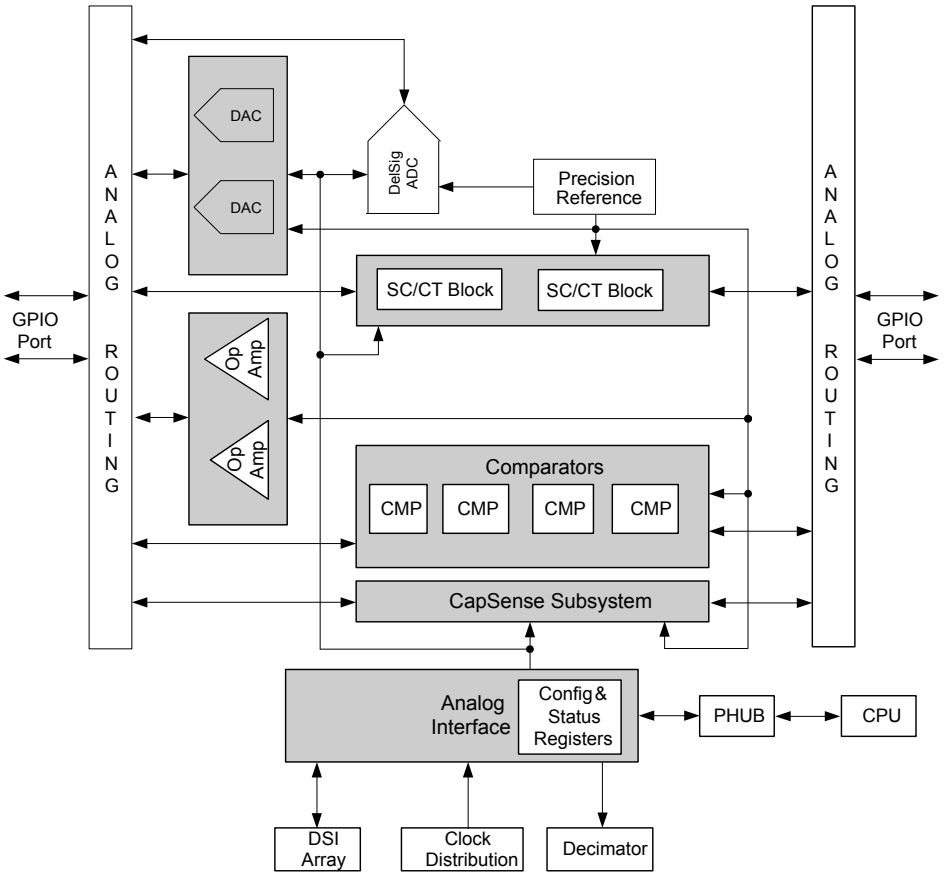
15. The I²C peripheral is non-compliant with the NXP I²C specification in the following areas: analog glitch filter, I/O $V_{OL}/I_{OL}$, I/O hysteresis. The I²C Block has a digital glitch filter (not available in sleep mode). The Fast-mode minimum fall-time specification can be met by setting the I/Os to slow speed mode. See the I/O Electrical Specifications in "Inputs and Outputs" section on page 74 for details.
16. Fixed-block I²C does not support undefined bus conditions, nor does it support Repeated Start in Slave mode. These conditions should be avoided, or the UDB-based I²C component should be used instead.

## 8. Analog Subsystem

The analog programmable system creates application specific combinations of both standard and advanced analog signal processing blocks. These blocks are then interconnected to each other and also to any pin on the device, providing a high level of design flexibility and IP security. The features of the analog subsystem are outlined here to provide an overview of capabilities and architecture.

- Flexible, configurable analog routing architecture provided by analog globals, analog mux bus, and analog local buses.
- High resolution delta-sigma ADC.
- Two 8-bit DACs that provide either voltage or current output.
- Four comparators with optional connection to configurable LUT outputs.
- Two configurable switched capacitor/continuous time (SC/CT) blocks for functions that include opamp, unity gain buffer, programmable gain amplifier, transimpedance amplifier, and mixer.
- Two opamps for internal use and connection to GPIO that can be used as high current output buffers.
- CapSense subsystem to enable capacitive touch sensing.
- Precision reference for generating an accurate analog voltage for internal analog blocks.

**Figure 8-1. Analog Subsystem Block Diagram**

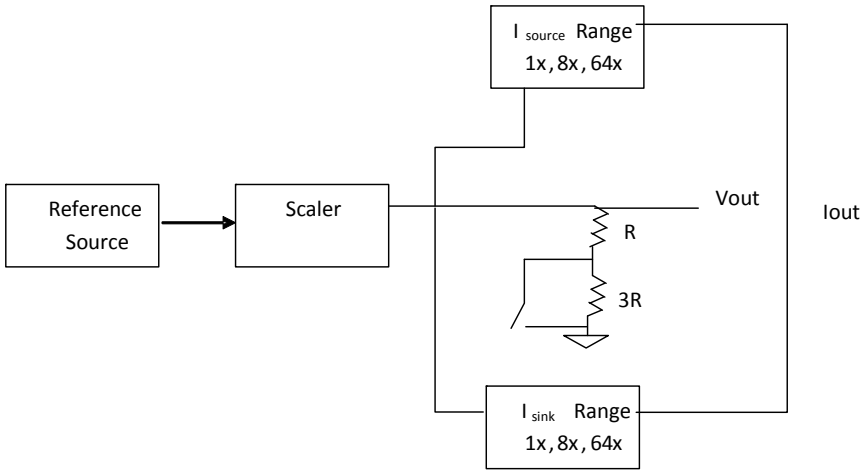


## 8.9 DAC

The CY8C34 parts contain up to two Digital to Analog Convertors (DACs). Each DAC is 8-bit and can be configured for either voltage or current output. The DACs support CapSense, power supply regulation, and waveform generation. Each DAC has the following features:

- Adjustable voltage or current output in 255 steps
- Programmable step size (range selection)
- Eight bits of calibration to correct ± 25 percent of gain error
- Source and sink option for current output
- High and low speed / power modes
- 8 Msps conversion rate for current output
- 1 Msps conversion rate for voltage output
- Monotonic in nature
- Data and strobe inputs can be provided by the CPU or DMA, or routed directly from the DSI
- Dedicated low-resistance output pin for high-current mode

**Figure 8-11. DAC Block Diagram**




### *8.9.1 Current DAC*

The current DAC (IDAC) can be configured for the ranges 0 to 31.875 µA, 0 to 255 µA, and 0 to 2.04 mA. The IDAC can be configured to source or sink current.

### *8.9.2 Voltage DAC*

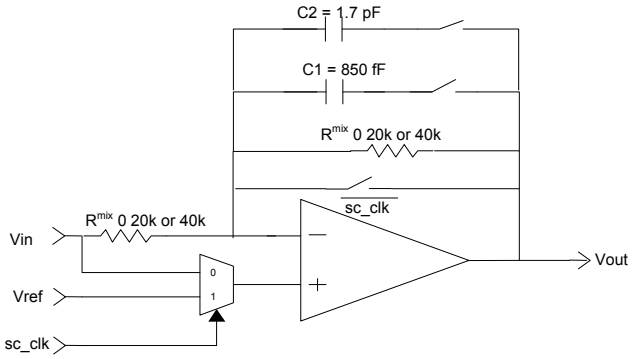
For the voltage DAC (VDAC), the current DAC output is routed through resistors. The two ranges available for the VDAC are 0 to 1.02 V and 0 to 4.08 V. In voltage mode any load connected to the output of a DAC should be purely capacitive (the output of the VDAC is not buffered).

## 8.10 Up/Down Mixer

In continuous time mode, the SC/CT block components are used to build an up or down mixer. Any mixing application contains an input signal frequency and a local oscillator frequency. The polarity of the clock, Fclk, switches the amplifier between inverting or noninverting gain. The output is the product of the input and the switching function from the local oscillator, with frequency components at the local oscillator plus and minus the signal frequency (Fclk + Fin and Fclk – Fin) and reduced-level frequency components at odd integer multiples of the local oscillator frequency. The local oscillator frequency is provided by the selected clock source for the mixer.

Continuous time up and down mixing works for applications with input signals and local oscillator frequencies up to 1 MHz.

**Figure 8-12. Mixer Configuration**



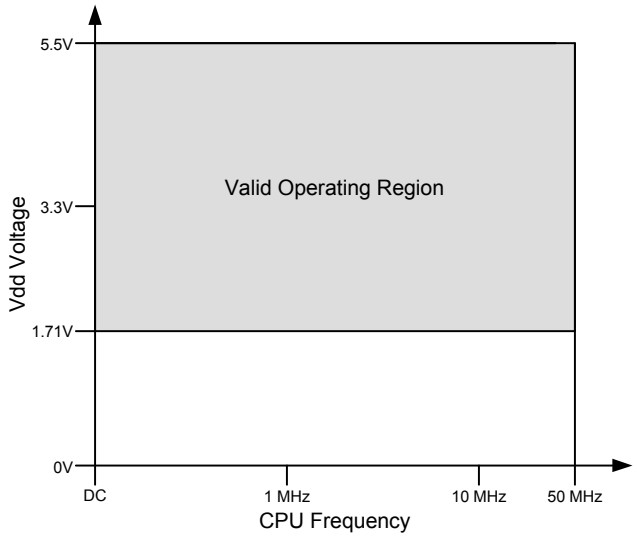

## 8.11 Sample and Hold

The main application for a sample and hold, is to hold a value stable while an ADC is performing a conversion. Some applications require multiple signals to be sampled simultaneously, such as for power calculations (V and I).

**Table 11-3. AC Specifications**[29]

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $F_{CPU}$ | CPU frequency | 1.71 V ≤ Vddd ≤ 5.5 V, -40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C | DC | – | 50 | MHz |
| | | 1.71 V ≤ Vddd ≤ 5.5 V, -40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C | DC | – | 50 | MHz |
| $F_{busclk}$ | Bus frequency | 1.71 V ≤ Vddd ≤ 5.5 V, -40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C | DC | – | 50 | MHz |
| | | 1.71 V ≤ Vddd ≤ 5.5 V, -40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C | DC | – | 50 | MHz |
| Svdd | Vdd ramp rate | | – | – | 0.066 | V/µs |
| Tio_init | Time from Vddd/Vdda/Vccd/Vcca ≥ IPOR to I/O ports set to their reset states | | – | – | 10 | µs |
| Tstartup | Time from Vddd/Vdda/Vccd/Vcca ≥ PRES to CPU executing code at reset vector | Vcca/Vccd = regulated from Vdda/Vddd, no PLL used, slow IMO boot mode (12 MHz typ.) | – | – | 66 | µs |
| Tsleep | Wakeup from sleep mode - Occurrence of LVD interrupt to beginning of execution of next CPU instruction | 1.71 V ≤ Vddd ≤ 5.5 V, Tj ≤ 100°C | – | – | 15 | µs |
| Thibernate | Wakeup from hibernate mode - Application of external interrupt to beginning of execution of next CPU instruction | | – | – | 100 | µs |

**Figure 11-2. Fcpu vs. Vdd**




**Note**
29. Based on device characterization (not production tested).

**Table 11-17. 12-bit Delta-sigma ADC DC Specifications** *(continued)*

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Rin_Buff | ADC input resistance | Input buffer used | 10 | – | – | MΩ |
| Rin_ADC12 | ADC input resistance | Input buffer bypassed, 12 bit, Range = ±1.024 V | – | 148[36] | – | kΩ |
| Vextref | ADC external reference input voltage | Pins P0[3], P3[2] | 0.9 | – | 1.3 | V |
| **Current Consumption** | | | | | | |
| $I_{DD\_12}$ | $I_{DDD}$ + $I_{DDA}$ Current consumption, 12 bit [37] | 192 ksps, unbuffered | – | – | 1.95 | mA |
| $I_{BUFF}$ | Buffer current consumption[37] | | – | – | 2.5 | mA |

**Notes**
36. By using switched capacitors at the ADC input an effective input resistance is created. Holding the gain and number of bits constant, the resistance is proportional to the inverse of the clock frequency. This value is calculated, not measured. For more information see the Technical Reference Manual.
37. Based on device characterization (Not production tested).

**Figure 11-31. IDAC INL vs Temperature, Range = 255 µA, High speed mode**

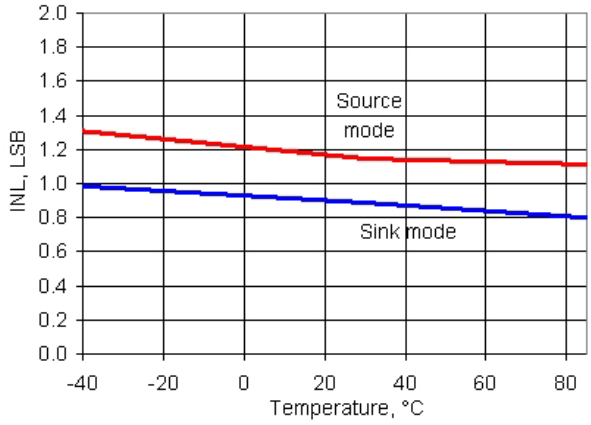



**Figure 11-32. IDAC DNL vs Temperature, Range = 255 µA, High speed mode**

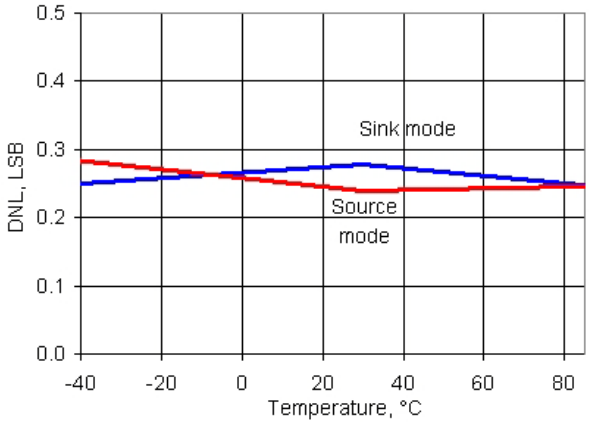



**Figure 11-33. IDAC Full Scale Error vs Temperature, Range = 255 µA, Source Mode**

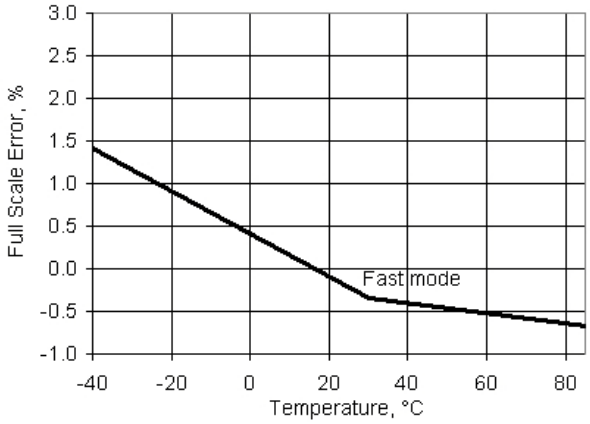


**Table 11-25. IDAC (Current Digital-to-Analog Converter) AC Specifications**

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Fdac | Update rate | | – | – | 8 | Msps |
| $T_{SETTLE}$ | Settling time to 0.5 LSB | Range = 31.875 µA or 255 µA, full scale transition, High speed mode, 600 Ω 15-pF load | – | – | 125 | ns |
| | Current noise | Range = 255 µA, source mode, High speed mode, Vdda = 5 V, 10 kHz | – | 340 | – | pA/sqrtHz |

**Figure 11-37. IDAC Step Response, Codes 0x40 - 0xC0, 255 µA Mode, Source Mode, High speed mode, Vdda = 5 V**

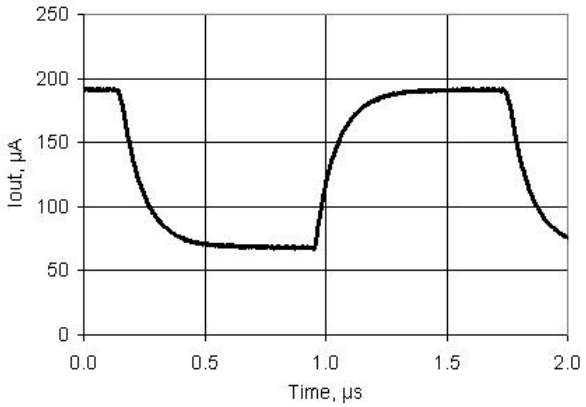



**Figure 11-38. IDAC Glitch Response, Codes 0x7F - 0x80, 255 µA Mode, Source Mode, High speed mode, Vdda = 5 V**

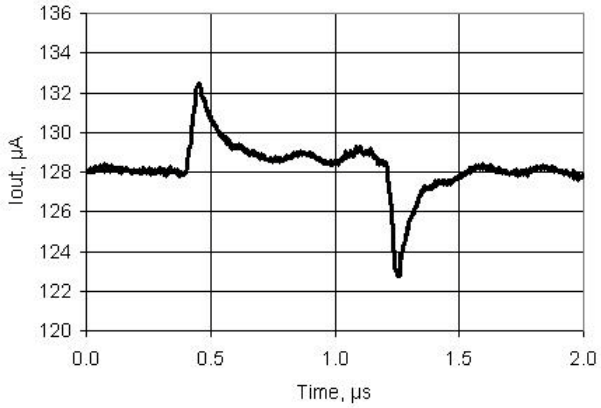


**Figure 11-42. VDAC DNL vs Input Code, 1 V Mode**

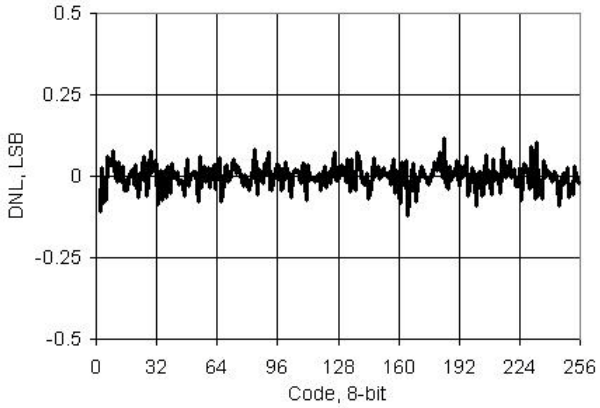



**Figure 11-43. VDAC INL vs Temperature, 1 V Mode**

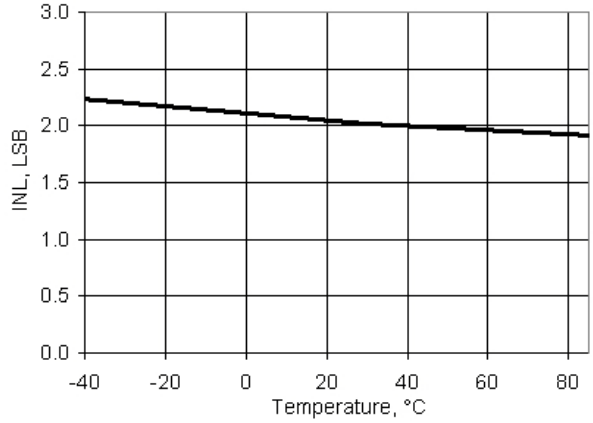



**Figure 11-44. VDAC DNL vs Temperature, 1 V Mode**

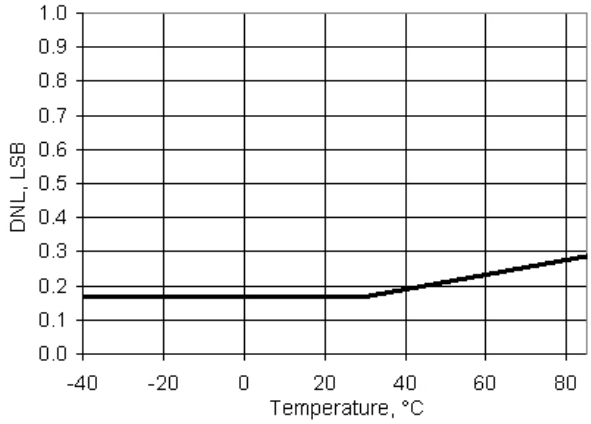
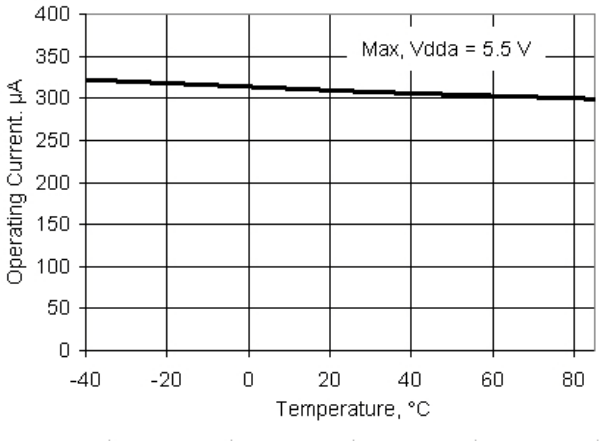


**Figure 11-48. VDAC Operating Current vs Temperature, 1 V Mode, High speed mode**



### *11.5.9 Transimpedance Amplifier*

The TIA is created using a SC/CT Analog Block, see the TIA component data sheet in PSoC Creator for full AC/DC specifications, and APIs and example code.

**Table 11-30. Transimpedance Amplifier (TIA) DC Specifications**

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Vioff | Input offset voltage | | - | - | 10 | mV |
| Rconv | Conversion resistance[44] | | | | | |
| | R = 20K | 40 pF load | -25 | - | +35 | % |
| | R = 30K | 40 pF load | -25 | - | +35 | % |
| | R = 40K | 40 pF load | -25 | - | +35 | % |
| | R = 80K | 40 pF load | -25 | - | +35 | % |
| | R = 120K | 40 pF load | -25 | - | +35 | % |
| | R = 250K | 40 pF load | -25 | - | +35 | % |
| | R= 500K | 40 pF load | -25 | - | +35 | % |
| | R = 1M | 40 pF load | -25 | - | +35 | % |
| | Quiescent current | | – | 1.1 | 2 | mA |

**Table 11-31. Transimpedance Amplifier (TIA) AC Specifications**

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| BW | Input bandwidth (–3 dB) | R = 20K; –40 pF load | 1000 | – | – | kHz |
| | | R = 120K; –40 pF load | 220 | – | – | kHz |
| | | R = 1M; –40 pF load | 25 | – | – | kHz |

**Note**
44. Conversion resistance values are not calibrated. Calibrated values and details about calibration are provided in PSoC Creator component data sheets. External precision resistors can also be used.

### 11.5.12 LCD Direct Drive

**Table 11-35. LCD Direct Drive DC Specifications**

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $I_{CC}$ | LCD system operating current | Device sleep mode with wakeup at 400-Hz rate to refresh LCDs, bus clock = 3 Mhz, Vddio = Vdda = 3 V, 4 commons, 16 segments, 1/4 duty cycle, 50 Hz frame rate, no glass connected | – | 38 | – | µA |
| $I_{CC\_SEG}$ | Current per segment driver | Strong drive mode | – | 260 | – | µA |
| $V_{BIAS}$ | LCD bias range ($V_{BIAS}$ refers to the main output voltage(V0) of LCD DAC) | $V_{DDA} \geq 3$ V and $V_{DDA} \geq V_{BIAS}$ | 2 | – | 5 | V |
| | LCD bias step size | $V_{DDA} \geq 3$ V and $V_{DDA} \geq V_{BIAS}$ | – | 9.1 × $V_{DDA}$ | – | mV |
| | LCD capacitance per segment/common driver | Drivers may be combined | – | 500 | 5000 | pF |
| | Long term segment offset | | – | – | 20 | mV |
| $I_{OUT}$ | Output drive current per segment driver) | Vddio = 5.5V, strong drive mode | 355 | – | 710 | µA |

**Table 11-36. LCD Direct Drive AC Specifications**

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $f_{LCD}$ | LCD frame rate | | 10 | 50 | 150 | Hz |

## 11.9 Clocking

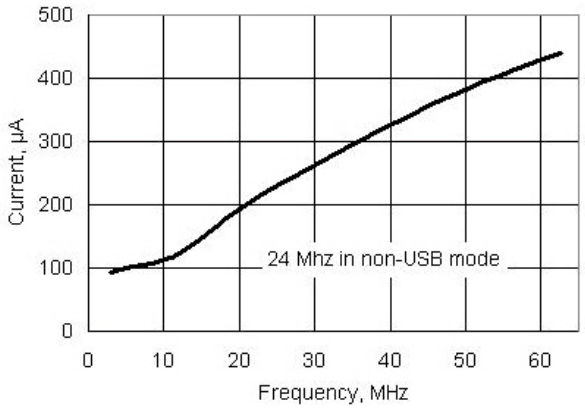
Specifications are valid for -40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

### *11.9.1 Internal Main Oscillator*

**Table 11-69. IMO DC Specifications**

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| | Supply current | | | | | |
| | 62.6 MHz | | – | – | 600 | µA |
| | 48 MHz | | – | – | 500 | µA |
| | 24 MHz – USB mode | With oscillator locking to USB bus | – | – | 500 | µA |
| | 24 MHz – non USB mode | | – | – | 300 | µA |
| | 12 MHz | | – | – | 200 | µA |
| | 6 MHz | | – | – | 180 | µA |
| | 3 MHz | | – | – | 150 | µA |

**Figure 11-62. IMO Current vs. Frequency**



### 11.9.3 External Crystal Oscillator

**Table 11-73. 32 kHz External Crystal DC Specifications[63]**

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Icc | Operating current | Low power mode; $C_L$ = 6 pF; -40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C | – | 0.25 | 1.0 | µA |
| DL | Drive level | Low-power mode; $C_L$ = 6 pF | – | – | 1 | µW |

**Table 11-74. 32 kHz External Crystal AC Specifications**

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| F | Frequency | | – | 32.768 | – | kHz |
| Ton | Startup time | High power mode | – | 1 | – | s |

**Table 11-75. MHz ECO AC Specifications**

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| F | Crystal frequency range | | 4 | – | 25 | MHz |

### 11.9.4 External Clock Reference

**Table 11-76. External Clock Reference AC Specifications**

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| | External frequency range | | 0 | – | 33 | MHz |
| | Input duty cycle range | Measured at $V_{DDIO}$/2 | 30 | 50 | 70 | % |
| | Input edge rate | $V_{IL}$ to $V_{IH}$ | 0.51 | – | – | V/ns |

### 11.9.5 Phase-Locked Loop

**Table 11-77. PLL DC Specifications**

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $I_{DD}$ | PLL operating current | In = 3 MHz, Out = 24 MHz | – | 200 | – | µA |

**Table 11-78. PLL AC Specifications**

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Fpllin | PLL input frequency[64] | Output of Prescalar | 1 | - | 48 | MHz |
| | PLL intermediate frequency[65] | | 1 | - | 3 | MHz |
| Fpllout | PLL output frequency[64] | -40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C | 24 | - | 50 | MHz |
| | | -40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C | 24 | - | 50 | MHz |
| | Lock time at startup | | - | - | 250 | µs |
| Jperiod-rms | Jitter (rms)[29] | -40°C ≤ Ta ≤ 85°C and Tj ≤ 100°C | - | - | 250 | ps |
| | | -40°C ≤ Ta ≤ 125°C and Tj ≤ 150°C | - | - | 400 | ps |

**Notes**
63. Based on device characterization (not production tested).
64. This specification is guaranteed by testing the PLL across the specified range using the IMO as the source for the PLL.
65. PLL input divider, Q, must be set so that the input frequency is divided down to the intermediate frequency range. Value for Q ranges from 1 to 16.

# 13. Packaging

**Table 13-1. Package Characteristics**

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $T_A$ | Operating ambient temperature | | –40 | 25.00 | 125 | °C |
| $T_J$ | Operating junction temperature | | –40 | – | 150 | °C |
| $T_{JA}$ | Package $\theta_{JA}$ (48-pin SSOP) | | – | 49 | – | °C/W |
| $T_{JA}$ | Package $\theta_{JA}$ (100-pin TQFP) | | – | 34 | – | °C/W |
| $T_{JC}$ | Package $\theta_{JC}$ (48-pin SSOP) | | – | 24 | – | °C/W |
| $T_{JC}$ | Package $\theta_{JC}$ (100-pin TQFP) | | – | 10 | – | °C/W |

**Table 13-2. Solder Reflow Peak Temperature**

| Package | Maximum Peak Temperature | Maximum Time at Peak Temperature |
|---|---|---|
| 48-pin SSOP | 260 °C | 30 seconds |
| 100-pin TQFP | 260 °C | 30 seconds |

**Table 13-3. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2**

| Package | MSL |
|---|---|
| 48-pin SSOP | MSL 3 |
| 100-pin TQFP | MSL 3 |

**Figure 13-1. 48-pin (300 mil) SSOP Package Outline**

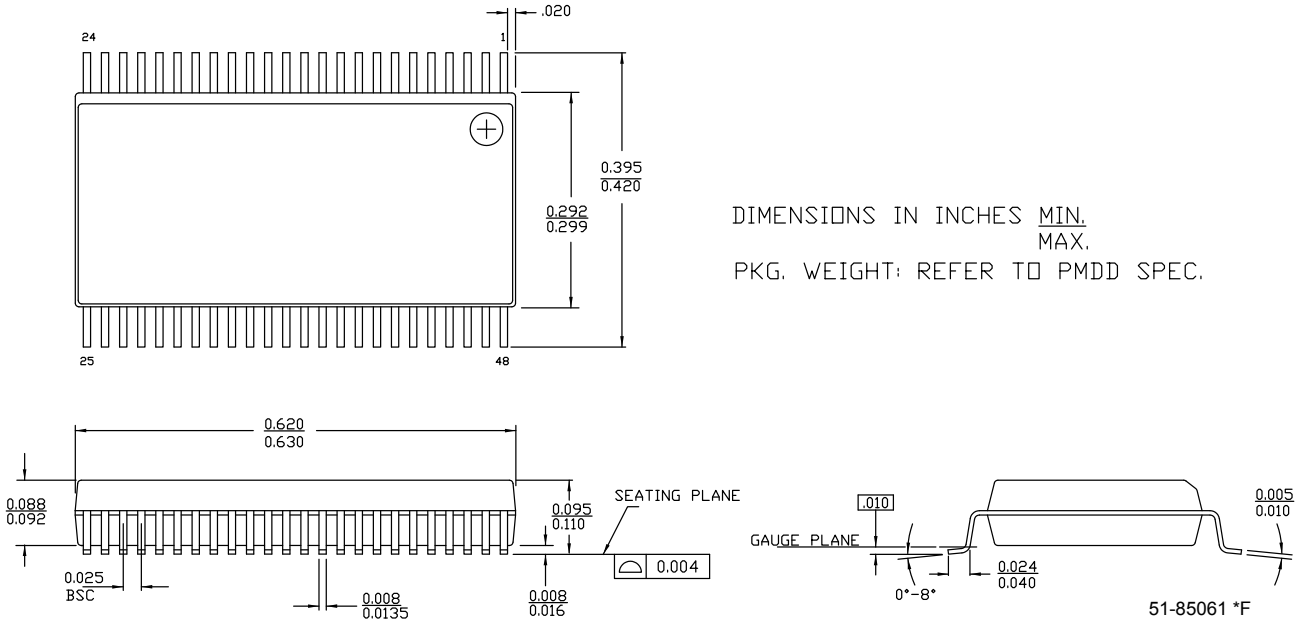
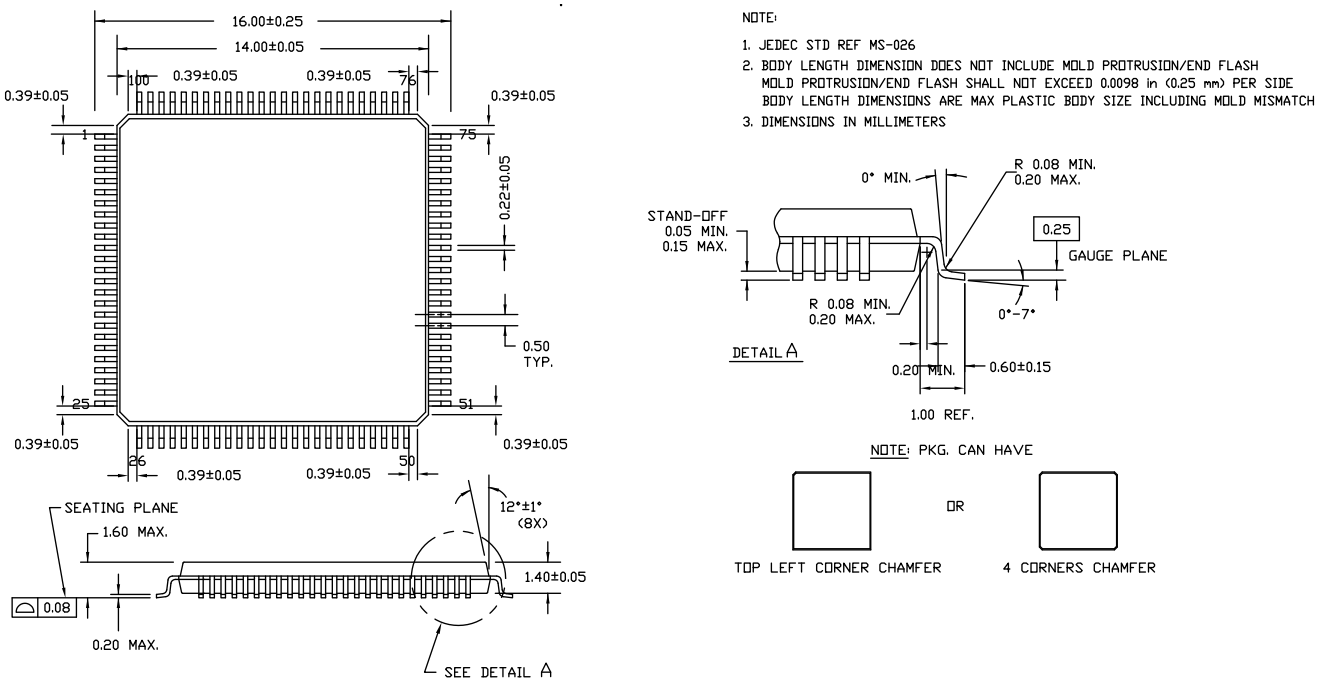


**Figure 13-2. 100-pin TQFP (14 × 14 × 1.4 mm) Package Outline**




51-85048 *I

## 14. Acronyms

**Table 14-1. Acronyms Used in this Document**

| Acronym | Description |
|---|---|
| abus | analog local bus |
| ADC | analog-to-digital converter |
| AG | analog global |
| AHB | AMBA (advanced microcontroller bus architecture) high-performance bus, an ARM data transfer bus |
| ALU | arithmetic logic unit |
| AMUXBUS | analog multiplexer bus |
| API | application programming interface |
| APSR | application program status register |
| ARM® | advanced RISC machine, a CPU architecture |
| ATM | automatic thump mode |
| BW | bandwidth |
| CAN | Controller Area Network, a communications protocol |
| CMRR | common-mode rejection ratio |
| CPU | central processing unit |
| CRC | cyclic redundancy check, an error-checking protocol |
| DAC | digital-to-analog converter, see also IDAC, VDAC |
| DFB | digital filter block |
| DIO | digital input/output, GPIO with only digital capabilities, no analog. See GPIO. |
| DMA | direct memory access, see also TD |
| DNL | differential nonlinearity, see also INL |
| DNU | do not use |
| DR | port write data registers |
| DSI | digital system interconnect |
| DWT | data watchpoint and trace |
| ECC | error correcting code |
| ECO | external crystal oscillator |
| EEPROM | electrically erasable programmable read-only memory |
| EMI | electromagnetic interference |
| EMIF | external memory interface |
| EOC | end of conversion |
| EOF | end of frame |
| EPSR | execution program status register |
| ESD | electrostatic discharge |
| ETM | embedded trace macrocell |

**Table 14-1. Acronyms Used in this Document** *(continued)*

| Acronym | Description |
|---|---|
| FIR | finite impulse response, see also IIR |
| FPB | flash patch and breakpoint |
| FS | full-speed |
| GPIO | general-purpose input/output, applies to a PSoC pin |
| HVI | high-voltage interrupt, see also LVI, LVD |
| IC | integrated circuit |
| IDAC | current DAC, see also DAC, VDAC |
| IDE | integrated development environment |
| $I^2C$, or IIC | Inter-Integrated Circuit, a communications protocol |
| IIR | infinite impulse response, see also FIR |
| ILO | internal low-speed oscillator, see also IMO |
| IMO | internal main oscillator, see also ILO |
| INL | integral nonlinearity, see also DNL |
| I/O | input/output, see also GPIO, DIO, SIO, USBIO |
| IPOR | initial power-on reset |
| IPSR | interrupt program status register |
| IRQ | interrupt request |
| ITM | instrumentation trace macrocell |
| LCD | liquid crystal display |
| LIN | Local Interconnect Network, a communications protocol. |
| LR | link register |
| LUT | lookup table |
| LVD | low-voltage detect, see also LVI |
| LVI | low-voltage interrupt, see also HVI |
| LVTTL | low-voltage transistor-transistor logic |
| MAC | multiply-accumulate |
| MCU | microcontroller unit |
| MISO | master-in slave-out |
| NC | no connect |
| NMI | nonmaskable interrupt |
| NRZ | non-return-to-zero |
| NVIC | nested vectored interrupt controller |
| NVL | nonvolatile latch, see also WOL |
| opamp | operational amplifier |
| PAL | programmable array logic, see also PLD |
| PC | program counter |
| PCB | printed circuit board |
| PGA | programmable gain amplifier |