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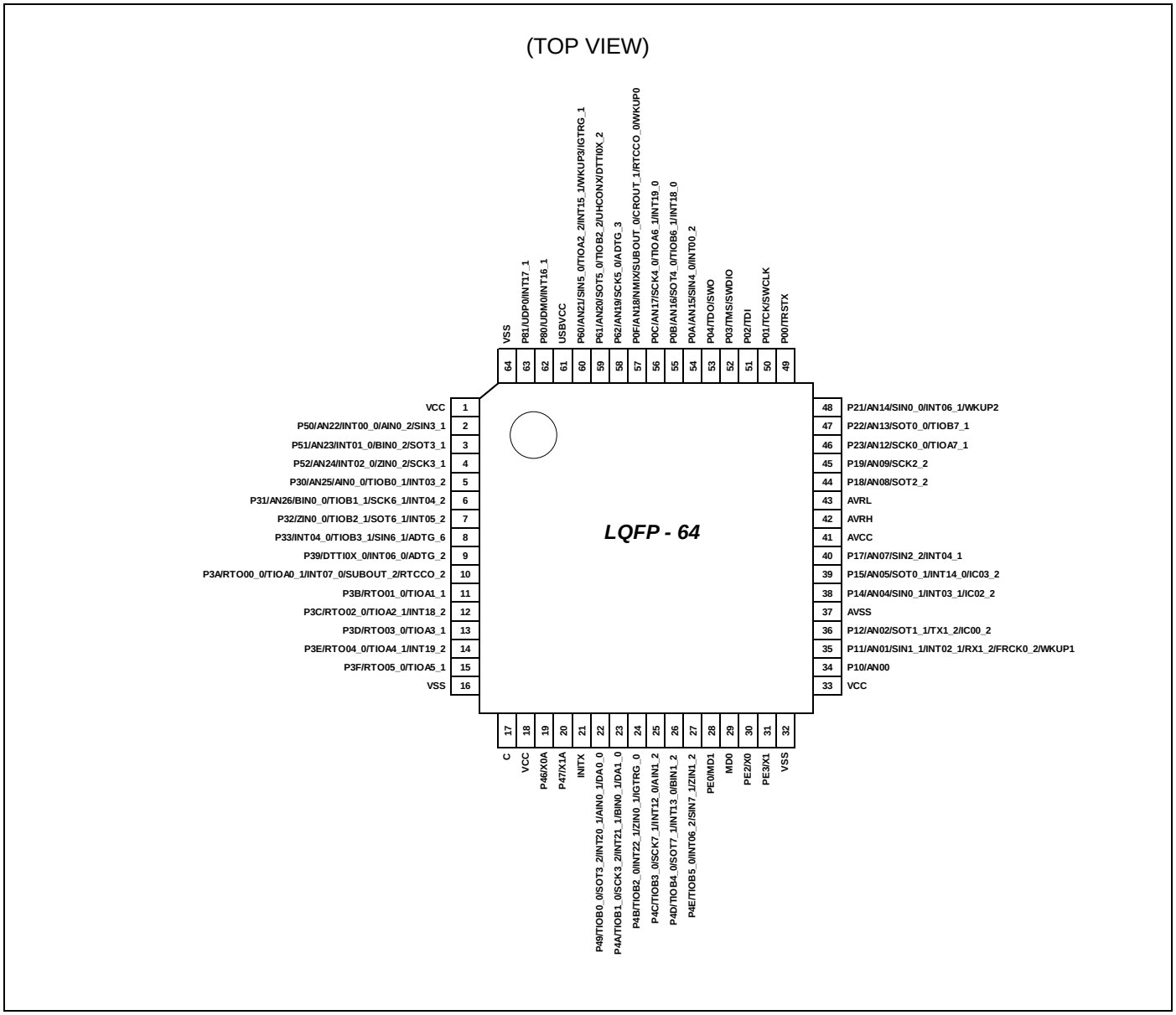
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, CSIO, I²C, LINbus, UART/USART, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	35
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 14x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb9bf521kpmc-g-jne2

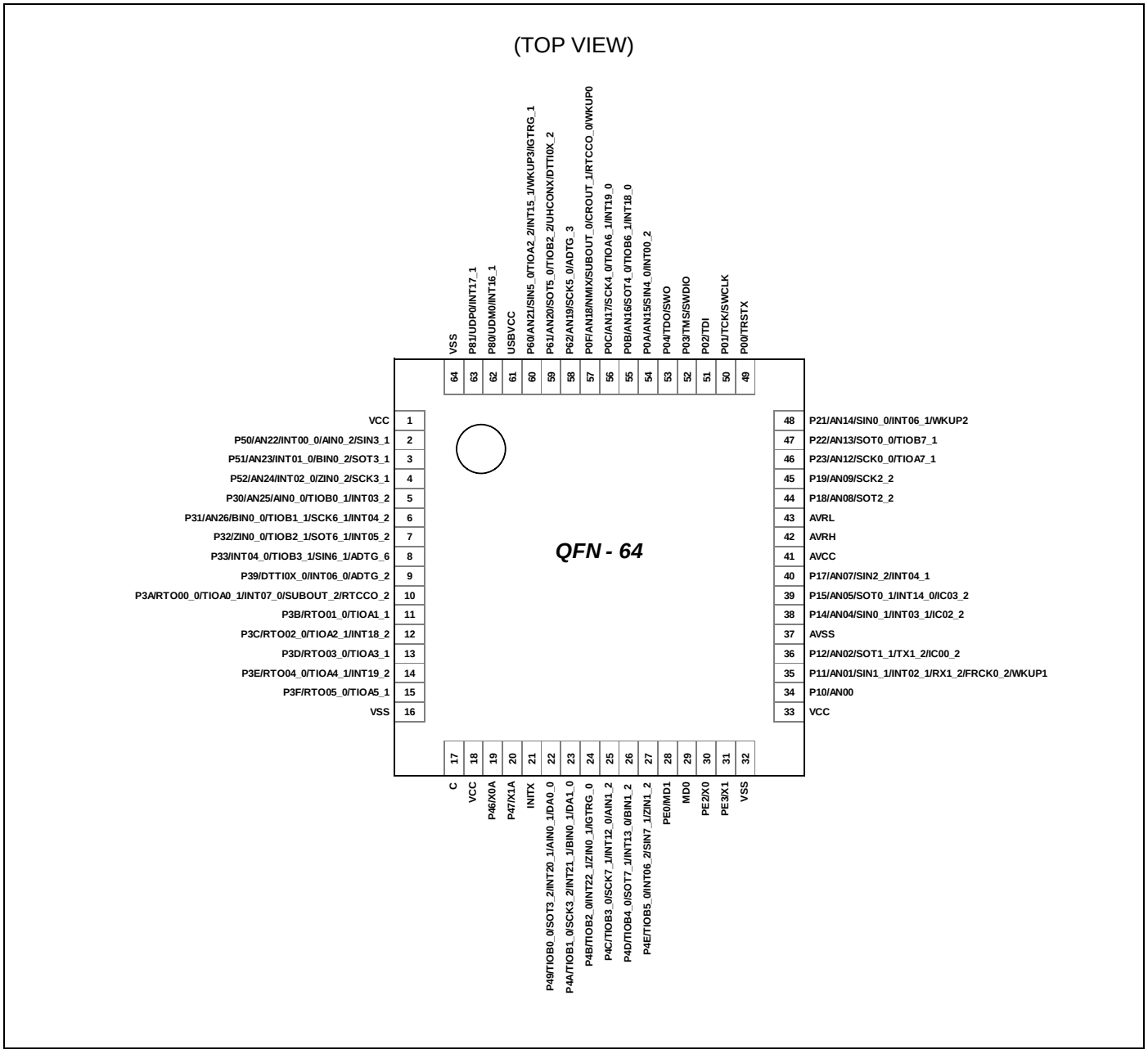
FPT-64P-M38/M39



Note:

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

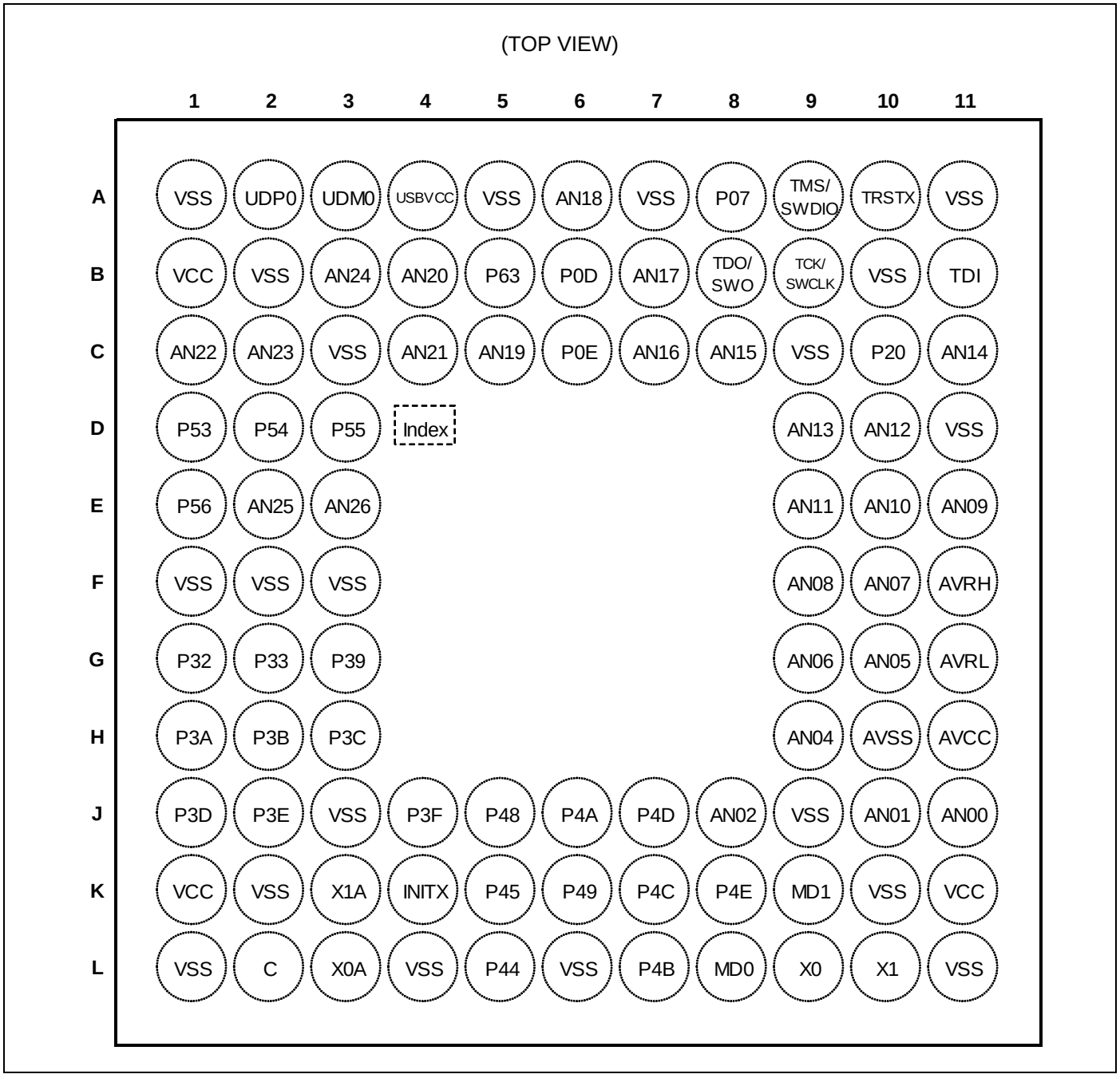
LCC-64P-M24



Note:

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

BGA-96P-M07



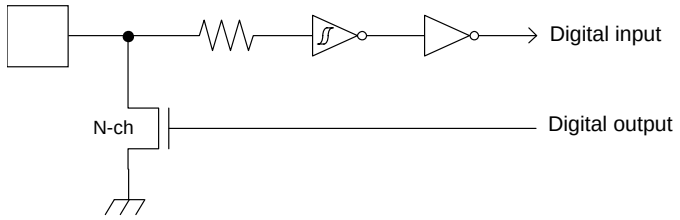
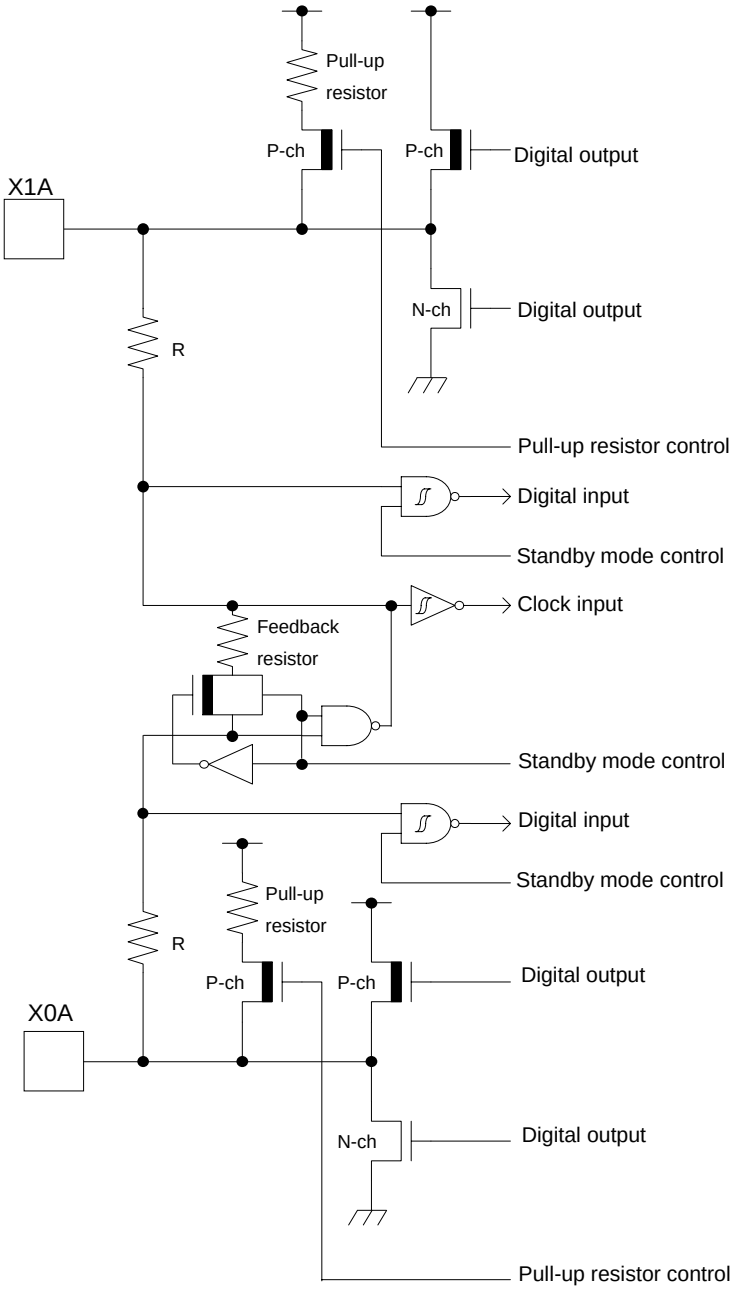
Note:

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Pin No				Pin Name	I/O circuit type	Pin state type
LQFP-80	BGA-96	LQFP-64 QFN-64	LQFP-48 QFN-48			
45	H10	37	28	AVSS	-	
46	H9	38	29	P14	F	N
				AN04		
				INT03_1		
				IC02_2		
				SIN0_1		
47	G10	39	30	P15	F	N
				AN05		
				IC03_2		
				SOT0_1 (SDA0_1)		
				INT14_0		
48	G9	-	-	P16	F	N
				AN06		
				SCK0_1 (SCL0_1)		
				INT15_0		
49	F10	40	-	P17	F	N
				AN07		
				SIN2_2		
				INT04_1		
50	H11	41	31	AVCC	-	
51	F11	42	32	AVRH	-	
52	G11	43	33	AVRL	-	
53	F9	44	-	P18	F	M
				AN08		
				SOT2_2 (SDA2_2)		
54	E11	45	-	P19	F	M
				AN09		
				SCK2_2 (SCL2_2)		
55	E10	-	-	P1A	F	N
				AN10		
				SIN4_1		
				INT05_1		
				IC00_1		

Pin No				Pin Name	I/O circuit type	Pin state type
LQFP-80	BGA-96	LQFP-64 QFN-64	LQFP-48 QFN-48			
56	E9	-	-	P1B	F	N
				AN11		
				SOT4_1 (SDA4_1)		
				IC01_1		
				INT20_2		
57	D10	46	34	P23	F	M
				SCK0_0 (SCL0_0)		
				TIOA7_1		
				AN12		
58	D9	47	35	P22	F	M
				SOT0_0 (SDA0_0)		
				TIOB7_1		
				AN13		
		-	-	ZIN1_1		
59	C11	48	36	P21	F	N
				SIN0_0		
				INT06_1		
				WKUP2		
				BIN1_1		
				AN14		
60	C10	-	-	P20	E	N
				INT05_0		
				CROUT_0		
				AIN1_1		
61	A10	49	37	P00	E	J
				TRSTX		
62	B9	50	38	P01	E	J
				TCK		
				SWCLK		
63	B11	51	39	P02	E	J
				TDI		
64	A9	52	40	P03	E	J
				TMS		
				SWDIO		
65	B8	53	41	P04	E	J
				TDO		
				SWO		
66	A8	-	-	P07	E	L
				ADTG_0		
				INT23_1		

Pin function	Pin name	Function description	Pin No			
			LQFP-80	BGA-96	LQFP-64 QFN-64	LQFP-48 QFN-48
External Interrupt	INT20_0	External interrupt request 20 input pin	70	B6	-	-
	INT20_1		30	K6	22	18
	INT20_2		56	E9	-	-
	INT21_0	External interrupt request 21 input pin	71	C6	-	-
	INT21_1		31	J6	23	19
	INT22_1	External interrupt request 22 input pin	32	L7	24	-
	INT23_1	External interrupt request 23 input pin	66	A8	-	-
	NMIX	Non-Maskable Interrupt input pin	72	A6	57	42
GPIO	P00	General-purpose I/O port 0	61	A10	49	37
	P01		62	B9	50	38
	P02		63	B11	51	39
	P03		64	A9	52	40
	P04		65	B8	53	41
	P07		66	A8	-	-
	P0A		67	C8	54	-
	P0B		68	C7	55	-
	P0C		69	B7	56	-
	P0D		70	B6	-	-
	P0E		71	C6	-	-
	P0F		72	A6	57	42
	P10	General-purpose I/O port 1	42	J11	34	25
	P11		43	J10	35	26
	P12		44	J8	36	27
	P14		46	H9	38	29
	P15		47	G10	39	30
	P16		48	G9	-	-
	P17		49	F10	40	-
	P18		53	F9	44	-
	P19		54	E11	45	-
	P1A		55	E10	-	-
	P1B		56	E9	-	-
	P20	General-purpose I/O port 2	60	C10	-	-
	P21		59	C11	48	36
	P22		58	D9	47	35
	P23		57	D10	46	34

Type	Circuit	Remarks
C		• Open drain output • CMOS level hysteresis input
D		It is possible to select the sub oscillation / GPIO function When the sub oscillation is selected. • Oscillation feedback resistor : Approximately 5 MΩ • With Standby mode control When the GPIO is selected. • CMOS level output. • CMOS level hysteresis input • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50 kΩ • I_{OH}= -4 mA, I_{OL}= 4 mA

Precautions Related to Usage of Devices

Cypress semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

6.2 Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Cypress's recommended conditions. For detailed information about mount conditions, contact your sales representative.

Lead Insertion Type

Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Cypress recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

Surface Mount Type

Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. Cypress. recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Cypress ranking of recommended conditions.

Lead-Free Packaging

CAUTION: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

Storage of Semiconductor Devices

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

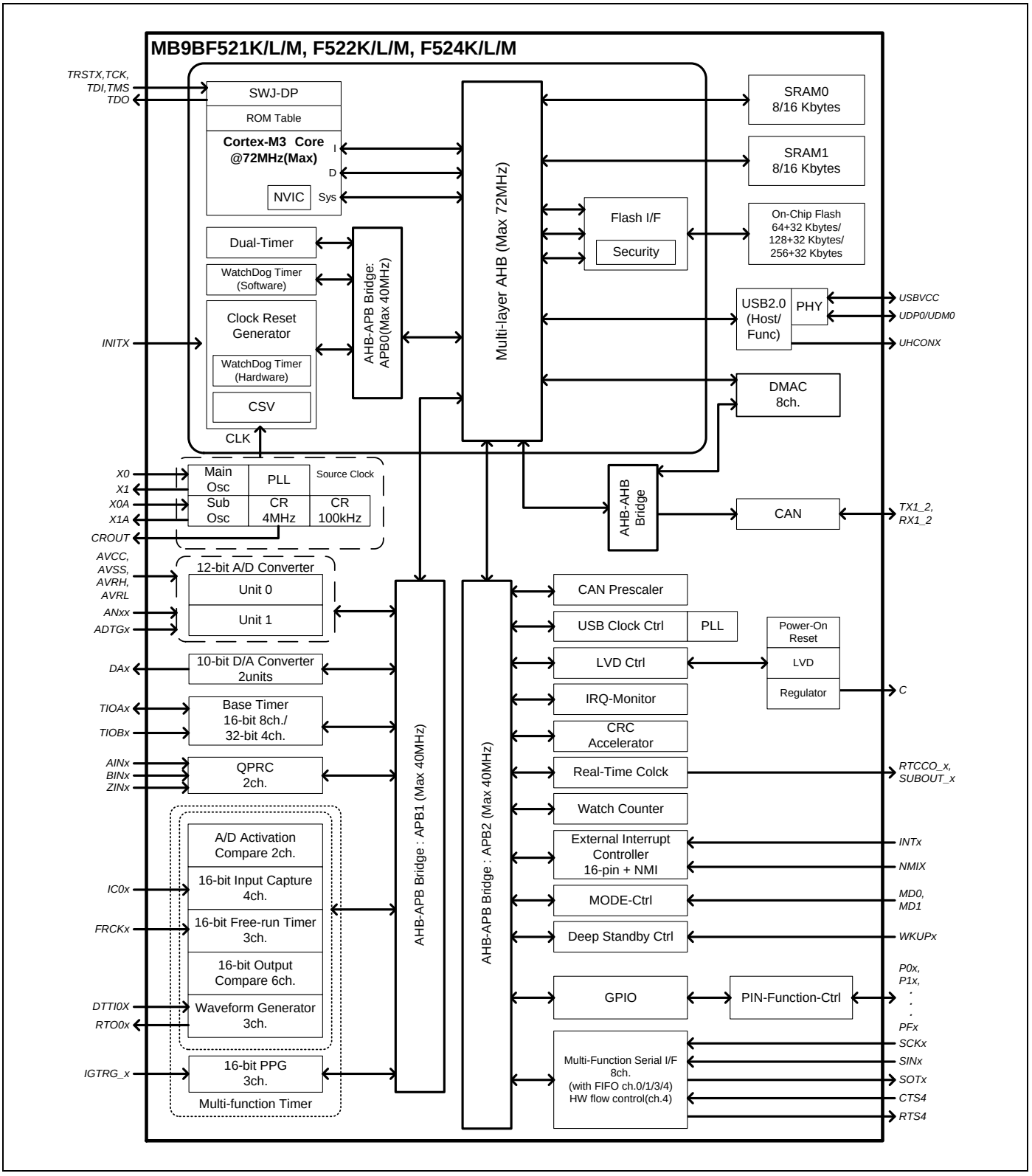
1. Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product. Store products in locations where temperature changes are slight.
2. Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5°C and 30°C.
   When you open Dry Package that recommends humidity 40% to 70% relative humidity.
3. When necessary, Cypress. packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.
4. Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

Baking

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Cypress recommended conditions for baking.

Condition: 125°C/24 h

8. Block Diagram



12.3 DC Characteristics

12.3.1 Current Rating

(V_{CC} = AV_{CC} = $USBV_{CC}$ = 2.7V to 5.5V, V_{SS} = AV_{SS} = AVRL = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions		Value		Unit	Remarks
					Typ	Max		
Run mode current	I_{CC}	VCC	PLL Run mode	CPU : 72 MHz, Peripheral : 36 MHz	32.5	41	mA	*1, *5
				CPU:72 MHz, Peripheral clock stops NOP operation	18	23	mA	*1, *5
			High-speed CR Run mode	CPU/ Peripheral : 4 MHz*2	2.5	3.4	mA	*1
			Sub Run mode	CPU/ Peripheral : 32 kHz	110	980	µA	*1, *6
			Low-speed CR Run mode	CPU/ Peripheral : 100 kHz	130	1030	µA	*1
Sleep mode current	I_{CCS}		PLL Sleep mode	Peripheral : 36 MHz	22	28	mA	*1, *5
			High-speed CR Sleep mode	Peripheral : 4 MHz*2	1.6	2.6	mA	*1
			Sub Sleep mode	Peripheral : 32 kHz	96	955	µA	*1, *6
			Low-speed CR Sleep mode	Peripheral : 100 kHz	115	975	µA	*1

*1: When all ports are fixed.

*2: When setting it to 4 MHz by trimming.

*3: T_A=+25°C, V_{CC}=5.5 V

*4: T_A=+105°C, V_{CC}=5.5 V

*5: When using the crystal oscillator of 4 MHz(Including the current consumption of the oscillation circuit)

*6: When using the crystal oscillator of 32 kHz(Including the current consumption of the oscillation circuit)

12.4 AC Characteristics

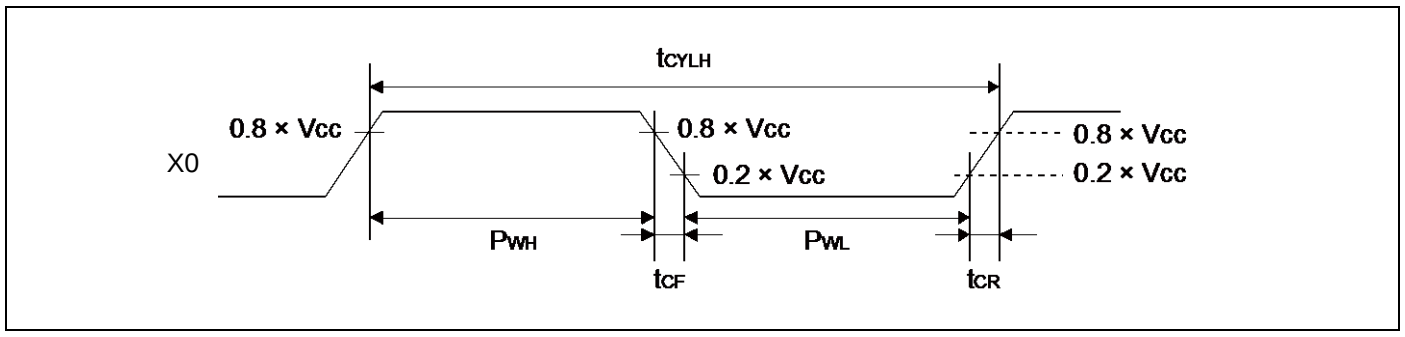
12.4.1 Main Clock Input Characteristics

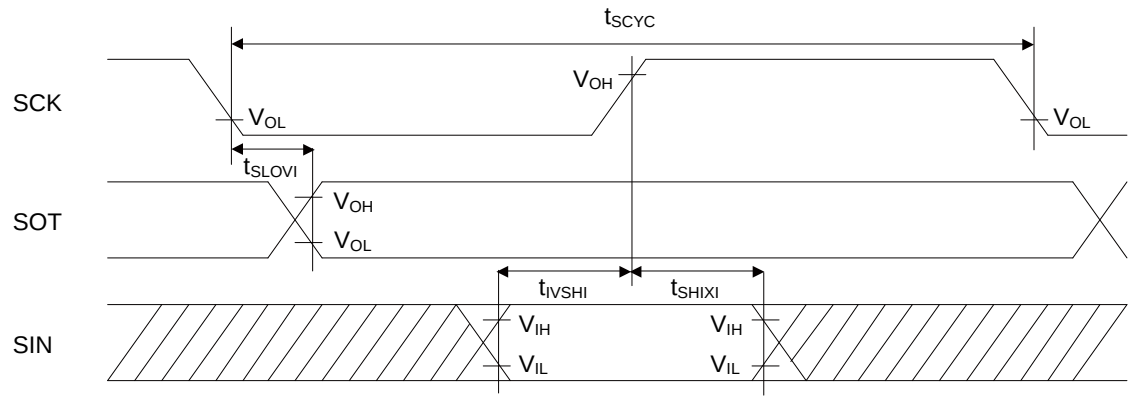
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input frequency	f_{CH}	X0, X1	$V_{CC} \geq 4.5$ V	4	48	MHz	When crystal oscillator is connected
			$V_{CC} < 4.5$ V	4	20		
			$V_{CC} \geq 4.5$ V	4	48	MHz	When using external Clock
			$V_{CC} < 4.5$ V	4	20		
Input clock cycle	t_{CYLH}		$V_{CC} \geq 4.5$ V	20.83	250	ns	When using external Clock
			$V_{CC} < 4.5$ V	50	250		
Input clock pulse width	-		P_{WH}/t_{CYLH}, P_{WL}/t_{CYLH}	45	55	%	When using external Clock
Input clock rising time and falling time	t_{CF}, t_{CR}		-	-	5	ns	When using external Clock
Internal operating clock frequency*1	f_{CM}	-	-	-	72	MHz	Master clock
	f_{CC}	-	-	-	72	MHz	Base clock (HCLK/FCLK)
	f_{CP0}	-	-	-	40	MHz	APB0 bus clock*2
	f_{CP1}	-	-	-	40	MHz	APB1 bus clock*2
	f_{CP2}	-	-	-	40	MHz	APB2 bus clock*2
Internal operating clock cycle time*1	t_{CYCC}	-	-	13.8	-	ns	Base clock (HCLK/FCLK)
	t_{CYCP0}	-	-	25	-	ns	APB0 bus clock*2
	t_{CYCP1}	-	-	25	-	ns	APB1 bus clock*2
	t_{CYCP2}	-	-	25	-	ns	APB2 bus clock*2

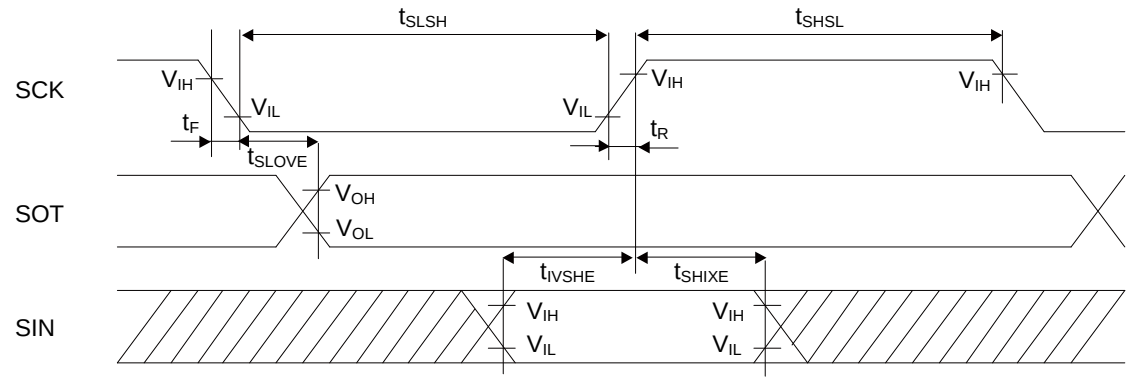
*1: For more information about each internal operating clock, see “Chapter: Clock” in “FM3 Family Peripheral Manual”.

*2: For about each APB bus which each peripheral is connected to, see “Block Diagram” in this datasheet.





Master mode



Slave mode

12.4.10 External Input Timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{INH}, t_{INL}	ADTG	-	$2t_{CYCP}$*1	-	ns	A/D converter trigger input
		FRCKx					Free-run timer input clock
		ICxx					Input capture
		DTTIxX	-	$2t_{CYCP}$*1	-	ns	Waveform generator
		INTxx,	*2	$2t_{CYCP}$ + 100*1	-	ns	External interrupt
		NMIX	*3	500	-	ns	NMI
		WKUPx	*4	500	-	ns	Deep standby wake up

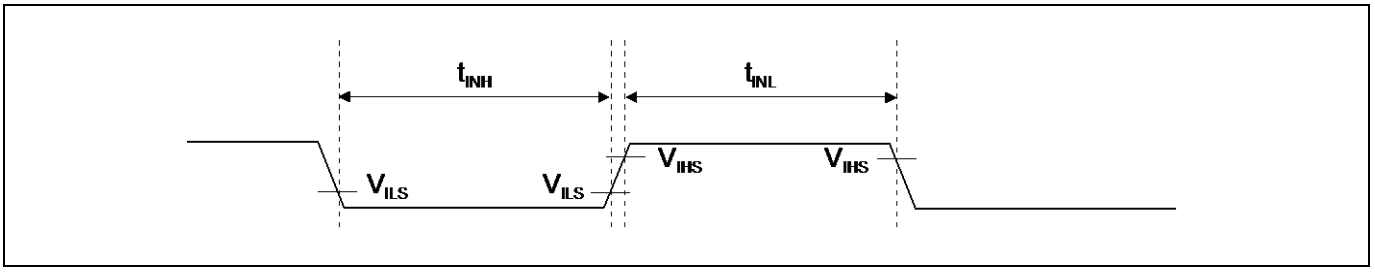
*1: t_{CYCP} indicates the APB bus clock cycle time.

About the APB bus number which the A/D converter, Multi-function Timer, External interrupt are connected to, see "Block Diagram" in this data sheet.

*2: When in Run mode, in Sleep mode.

*3: When in Stop mode, in RTL mode, in Timer mode.

*4: When in Deep Standby RTC mode, in Deep Standby Stop mode.



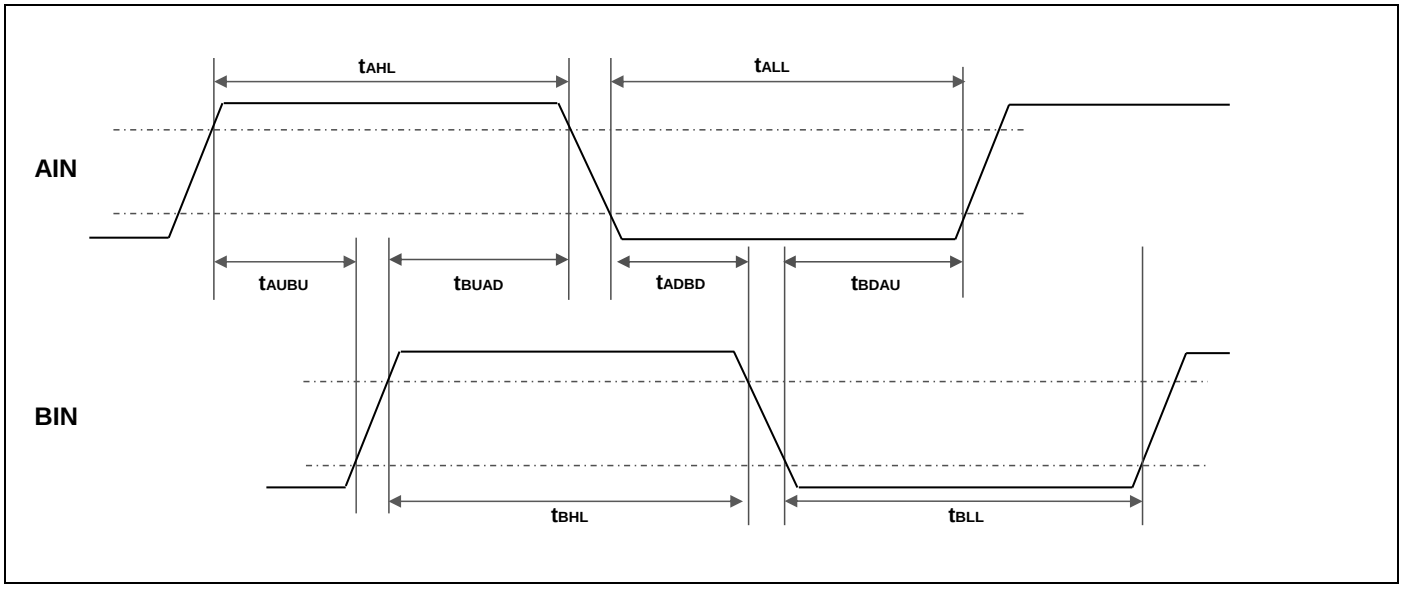
12.4.11 Quadrature Position/Revolution Counter timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Conditions	Value		Unit
			Min	Max	
AIN pin H width	t_{AHL}	-	$2t_{CYCP}$*	-	ns
AIN pin L width	t_{ALL}	-			
BIN pin H width	t_{BHL}	-			
BIN pin L width	t_{BLL}	-			
BIN rising time from AIN pin H level	t_{AUBU}	PC_Mode2 or PC_Mode3			
AIN falling time from BIN pin H level	t_{BUAD}	PC_Mode2 or PC_Mode3			
BIN falling time from AIN pin L level	t_{ADBD}	PC_Mode2 or PC_Mode3			
AIN rising time from BIN pin L level	t_{BDAU}	PC_Mode2 or PC_Mode3			
AIN rising time from BIN pin H level	t_{BUAU}	PC_Mode2 or PC_Mode3			
BIN falling time from AIN pin H level	t_{AUBD}	PC_Mode2 or PC_Mode3			
AIN falling time from BIN pin L level	t_{BDAD}	PC_Mode2 or PC_Mode3			
BIN rising time from AIN pin L level	t_{ADBU}	PC_Mode2 or PC_Mode3			
ZIN pin H width	t_{ZHL}	QCR:CGSC=0			
ZIN pin L width	t_{ZLL}	QCR:CGSC=0			
AIN/BIN rising and falling time from determined ZIN level	t_{ZABE}	QCR:CGSC=1			
Determined ZIN level from AIN/BIN rising and falling time	t_{ABEZ}	QCR:CGSC=1			

*: t_{CYCP} indicates the APB bus clock cycle time.

About the APB bus number which the Quadrature Position/Revolution Counter is connected to, see “Block Diagram” in this data sheet.



12.5 12-bit A/D Converter

Electrical characteristics for the A/D converter

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = AVRL = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	12	bit	
Integral Nonlinearity	-	-	-	± 1.5	± 4.5	LSB	AVRH = 2.7 V to 5.5 V
Differential Nonlinearity	-	-	-	± 1.7	± 2.5	LSB	
Zero transition voltage	V_{ZT}	ANxx	-	± 10	± 15	mV	
Full-scale transition voltage	V_{FST}	ANxx	-	AVRH ± 5	AVRH ± 15	mV	
Conversion time	-	-	0.8*1	-	-	µs	AV_{CC} ≥ 4.5 V
			1.0*1	-	-		AV_{CC} < 4.5 V
Sampling time*2	t_S	-	0.24	-	10	µs	AV_{CC} ≥ 4.5 V
			0.3	-			AV_{CC} < 4.5 V
Compare clock cycle*3	t_{CCK}	-	40	-	1000	ns	AV_{CC} ≥ 4.5 V
			50	-			AV_{CC} < 4.5 V
State transition time to operation permission	t_{STT}	-	-	-	1.0	µs	
Analog input capacity	C_{AIN}	-	-	-	9.7	pF	
Analog input resistor	R_{AIN}	-	-	-	1.7	kΩ	AV_{CC} ≥ 4.5 V
					2.4		AV_{CC} < 4.5 V
Interchannel disparity	-	-	-	-	4	LSB	
Analog port input current	-	ANxx	-	-	5	µA	
Analog input voltage	-	ANxx	AVRL	-	AVRH	V	
Reference voltage	-	AVRH	2.7	-	AV_{CC}	V	
	-	AVRL	AV_{SS}	-	AV_{SS}	V	

*1: The conversion time is the value of sampling time (t_S) + compare time (t_C).

The condition of the minimum conversion time is the following.

AV_{CC} ≥ 4.5 V, HCLK=50 MHz sampling time: 240 ns, compare time: 560 ns
AV_{CC} < 4.5 V, HCLK=40 MHz sampling time: 300 ns, compare time: 700 ns

Ensure that it satisfies the value of the sampling time (t_S) and compare clock cycle (t_{CCK}).
For setting of the sampling time and compare clock cycle, see "Chapter 1-1: A/D Converter" in “FM3 Family Peripheral Manual Analog Macro Part”.

The register settings of the A/D Converter are reflected in the operation according to the APB bus clock timing.
For the number of the APB bus to which the A/D Converter is connected, see "Block Diagram".
The base clock (HCLK) is used to generate the sampling time and the compare clock cycle.

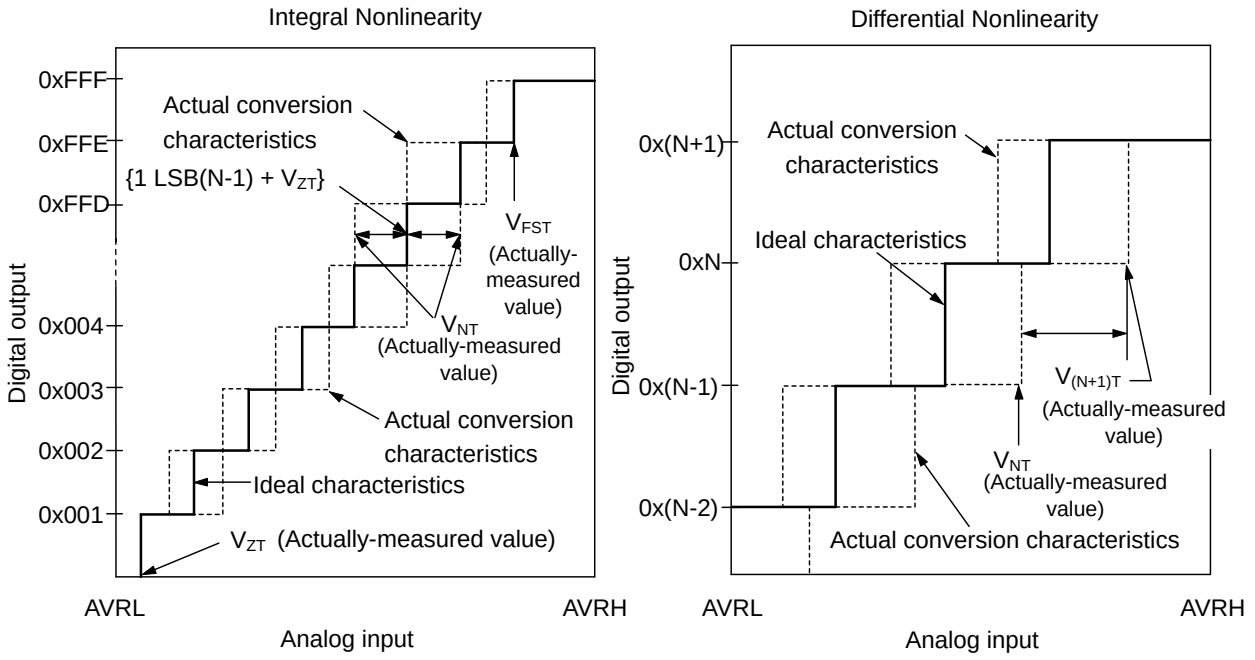
*2: A necessary sampling time changes by external impedance.

Ensure that it sets the sampling time to satisfy (Equation 1).

*3: The compare time (t_C) is the value of (Equation 2).

12.5.1 Definition of 12-bit A/D Converter Terms

- Resolution: Analog variation that is recognized by an A/D converter.
- Integral Nonlinearity: Deviation of the line between the zero-transition point (0b000000000000 ⟷ 0b000000000001) and the full-scale transition point (0b111111111110 ⟷ 0b111111111111) from the actual conversion characteristics.
- Differential Nonlinearity: Deviation from the ideal value of the input voltage that is required to change the output code by 1 LSB.



$$\text{Integral Nonlinearity of digital output N} = \frac{V_{NT} - \{1LSB \times (N - 1) + V_{ZT}\}}{1LSB} \text{ [LSB]}$$

$$\text{Differential Nonlinearity of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1LSB} - 1 \text{ [LSB]}$$

$$1LSB = \frac{V_{FST} - V_{ZT}}{4094}$$

N: A/D converter digital output value.

V_{ZT}: Voltage at which the digital output changes from 0x000 to 0x001.

V_{FST}: Voltage at which the digital output changes from 0xFFE to 0xFFF.

V_{NT}: Voltage at which the digital output changes from 0x(N − 1) to 0xN.

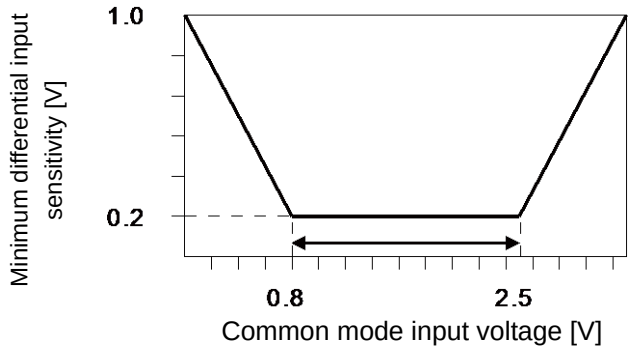
12.7 USB Characteristics

(V_{CC} = 2.7V to 5.5V, $USBV_{CC}$ = 3.0V to 3.6V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter		Symbol	Pin name	Conditions	Value		Unit	Remarks
					Min	Max		
Input characteristics	Input H level voltage	V_{IH}	UDP0, UDM0	-	2.0	$USBV_{CC}$ + 0.3	V	*1
	Input L level voltage	V_{IL}		-	V_{SS} - 0.3	0.8	V	*1
	Differential input sensitivity	V_{DI}		-	0.2	-	V	*2
	Different common mode range	V_{CM}		-	0.8	2.5	V	*2
Output characteristics	Output H level voltage	V_{OH}		External pull-down resistor = 15 kΩ	2.8	3.6	V	*3
	Output L level voltage	V_{OL}		External pull-up resistor = 1.5 kΩ	0.0	0.3	V	*3
	Crossover voltage	V_{CRS}		-	1.3	2.0	V	*4
	Rising time	t_{FR}		Full-Speed	4	20	ns	*5
	Falling time	t_{FF}		Full-Speed	4	20	ns	*5
	Rising/falling time matching	t_{FRFM}		Full-Speed	90	111.11	%	*5
	Output impedance	Z_{DRV}		Full-Speed	28	44	Ω	*6
	Rising time	t_{LR}		Low-Speed	75	300	ns	*7
	Falling time	t_{LF}		Low-Speed	75	300	ns	*7
	Rising/falling time matching	t_{LRFM}		Low-Speed	80	125	%	*7

*1: The switching threshold voltage of the Single-End-Receiver of USB I/O buffer is set as within V_{IL} (Max) = 0.8V, V_{IH} (Min) = 2.0 V (TTL input standard).
There are some hysteresis to lower noise sensitivity.

*2: Use the differential-Receiver to receive the USB differential data signal.
The Differential-Receiver has 200 mV of differential input sensitivity when the differential data input is within 0.8 V to 2.5 V to the local ground reference level.
The voltage range above is said to be the common mode input voltage range.



12.10.2 Return Factor: Reset

The return time from Low-Power consumption mode is indicated as follows. It is from releasing reset to starting the program operation.

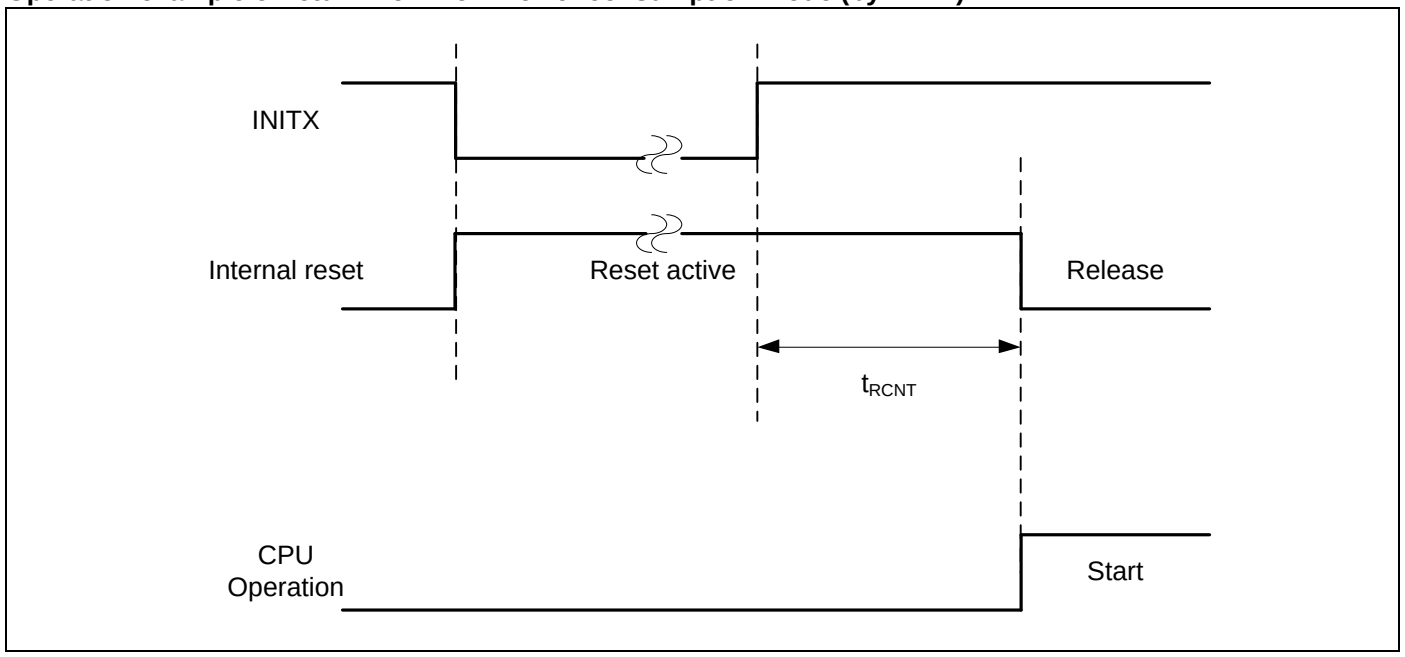
Return Count Time

(V_{CC} = 2.7V to 5.5V, T_A = - 40°C to + 105°C)

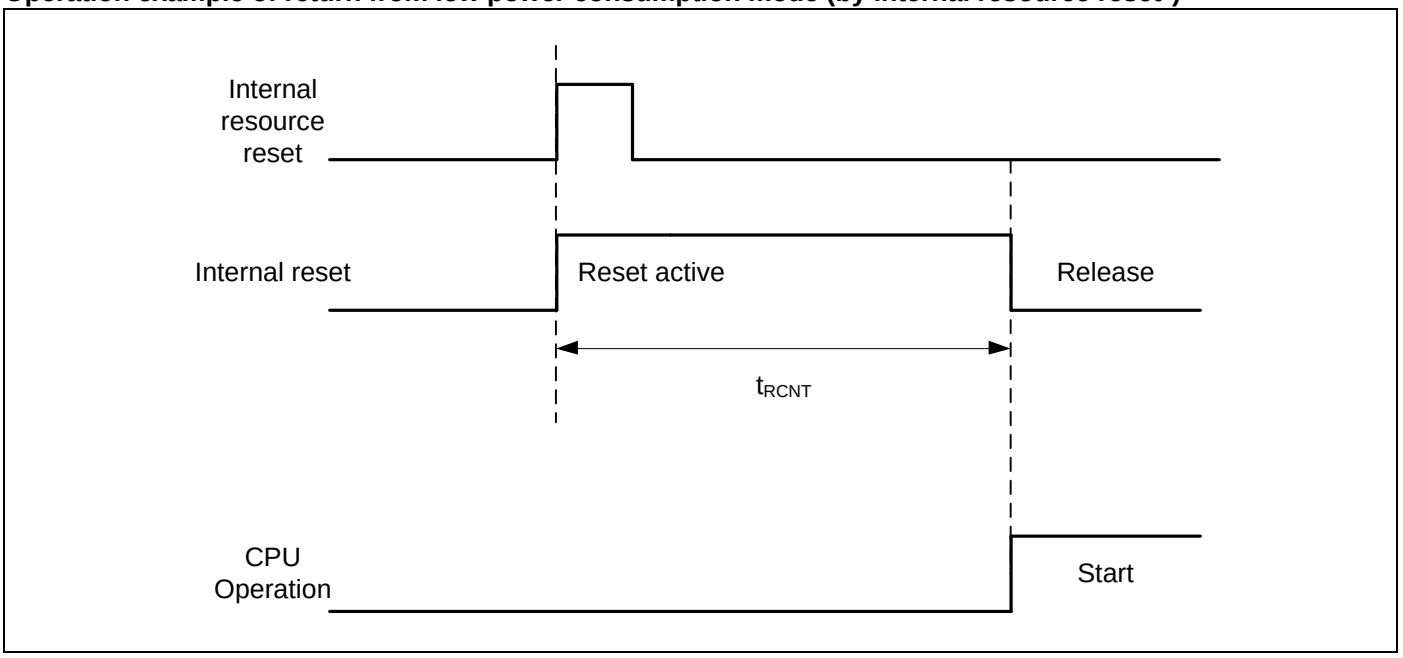
Parameter	Symbol	Value		Unit	Remarks
		Typ	Max*		
Sleep mode	t_{RCNT}	148	263	µs	
High-speed CR Timer mode, Main Timer mode, PLL Timer mode		148	263	µs	
Low-speed CR Timer mode		248	463	µs	
Sub Timer mode		312	496	µs	
RTC mode, Stop mode		268	503	µs	
Deep Standby RTC mode		308	583	µs	When RAM is off
Deep Standby Stop mode		268	503	µs	When RAM is on

*: The maximum value depends on the accuracy of built-in CR.

Operation example of return from Low-Power consumption mode (by INITX)



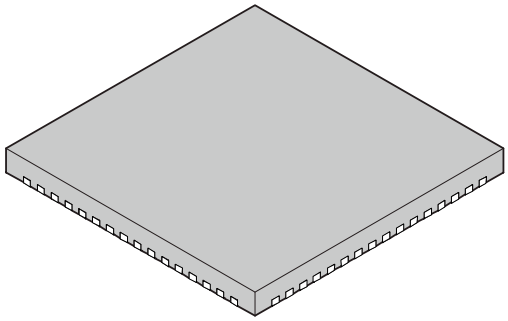
Operation example of return from low power consumption mode (by internal resource reset*)



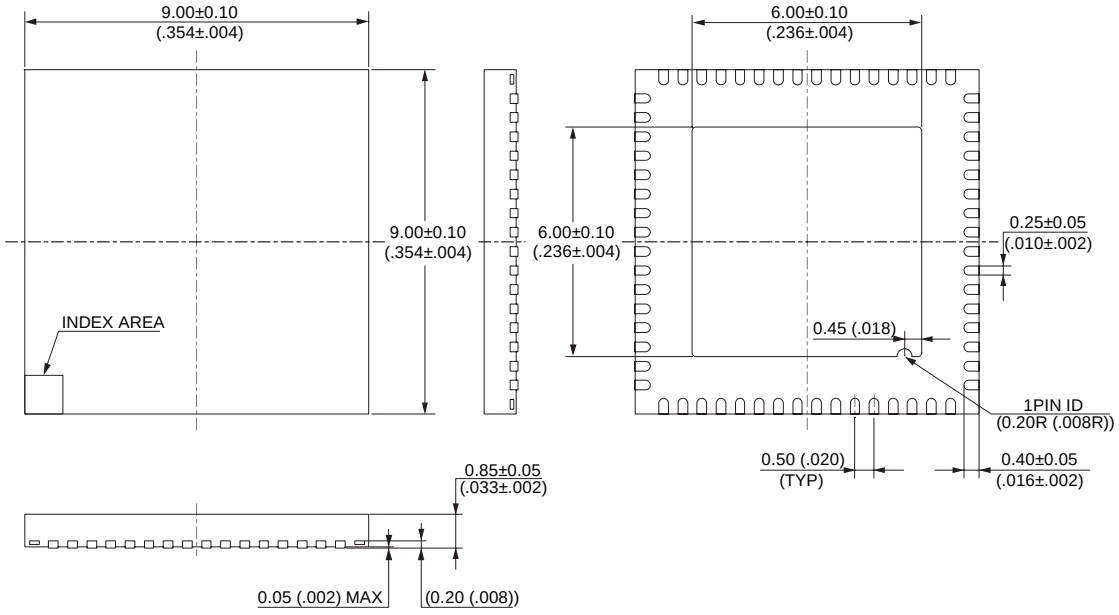
*: Internal resource reset is not included in return factor by the kind of Low-Power consumption mode.

Notes:

- The return factor is different in each Low-Power consumption modes.
  See “Chapter 6: Low Power Consumption Mode” and “Operations of Standby Modes” in FM3 Family Peripheral Manual.
- When interrupt recoveries, the operation mode that CPU recoveries depends on the state before the Low-Power consumption mode transition. See “Chapter 6: Low Power Consumption Mode” in “FM3 Family Peripheral Manual”.
- The time during the power-on reset/low-voltage detection reset is excluded. See “12.4.7. Power-on Reset Timing in 12.4. AC Characteristics in 12.Electrical Characteristics” for the detail on the time during the power-on reset/low -voltage detection reset.
- When in recovery from reset, CPU changes to the high-speed CR run mode. When using the main clock or the PLL clock, it is necessary to add the main clock oscillation stabilization wait time or the Main PLL clock stabilization wait time.
- The internal resource reset means the watchdog reset and the CSV reset.

64-pin plastic QFN		
	Lead pitch	0.50 mm
	Package width × package length	9.00 mm × 9.00 mm
	Sealing method	Plastic mold
	Mounting height	0.90 mm MAX
	Weight	-
(LCC-64P-M24)		

64-pin plastic QFN
(LCC-64P-M24)



Dimensions in mm (inches).
Note: The values in parentheses are reference values.