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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, CSIO, I²C, LINbus, UART/USART, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	50
Program Memory Size	288KB (288K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 23x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb9bf524lpmc-g-jne2

4. List of Pin Functions

List of pin numbers

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Pin No				Pin Name	I/O circuit type	Pin state type
LQFP-80	BGA-96	LQFP-64 QFN-64	LQFP-48 QFN-48			
1	B1	1	1	VCC	-	
2	C1	2	2	P50 INT00_0 AIN0_2 SIN3_1 AN22	F	N
3	C2	3	3	P51 INT01_0 BIN0_2 SOT3_1 (SDA3_1) AN23	F	N
4	B3	4	4	P52 INT02_0 ZIN0_2 SCK3_1 (SCL3_1) AN24	F	N
5	D1	-	-	P53 SIN6_0 TIOA1_2 INT07_2	E	L
6	D2	-	-	P54 SOT6_0 (SDA6_0) TIOB1_2 INT18_1	E	L
7	D3	-	-	P55 SCK6_0 (SCL6_0) ADTG_1 INT19_1	E	L
8	E1	-	-	P56 INT08_2	E	L
9	E2	5	-	P30 AIN0_0 TIOB0_1 INT03_2 AN25	F	N

Pin No				Pin Name	I/O circuit type	Pin state type
LQFP-80	BGA-96	LQFP-64 QFN-64	LQFP-48 QFN-48			
18	J2	14	10	P3E RTO04_0 (PPG04_0) TIOA4_1 INT19_2	G	L
19	J4	15	11	P3F RTO05_0 (PPG04_0) TIOA5_1	G	K
20	L1	16	12	VSS	-	
21	L5	-	-	P44 TIOA4_0 INT10_0	G	L
22	K5	-	-	P45 TIOA5_0 INT11_0	G	L
23	L2	17	13	C	-	
24	L4	-	-	VSS	-	
25	K1	18	14	VCC	-	
26	L3	19	15	P46 X0A	D	F
27	K3	20	16	P47 X1A	D	G
28	K4	21	17	INITX	B	C
29	J5	-	-	P48 INT14_1 SIN3_2	E	L
30	K6	22	18	P49 TIOB0_0 INT20_1 DA0_0	L	L
			-	SOT3_2 (SDA3_2) AIN0_1		
31	J6	23	19	P4A TIOB1_0 INT21_1 DA1_0	L	L
			-	SCK3_2 (SCL3_2) BIN0_1		

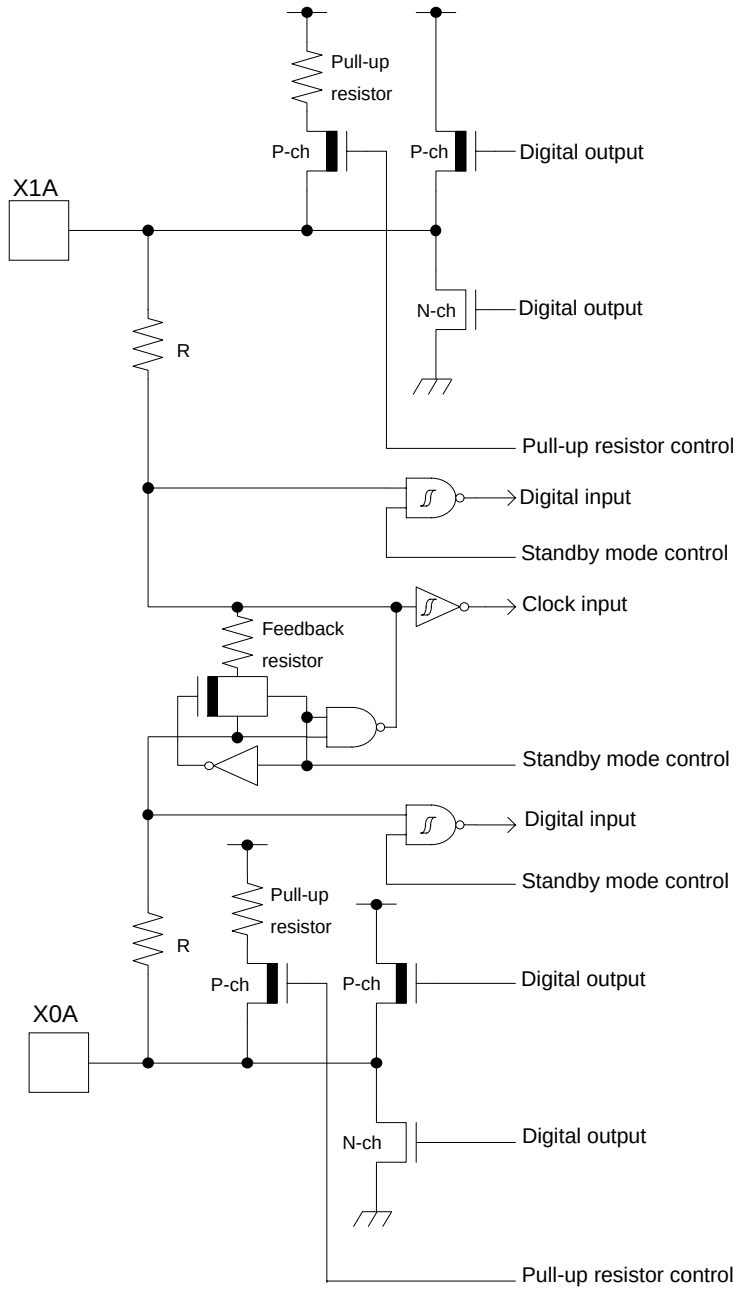
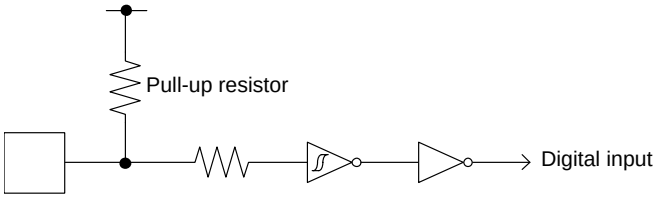
Pin No				Pin Name	I/O circuit type	Pin state type
LQFP-80	BGA-96	LQFP-64 QFN-64	LQFP-48 QFN-48			
45	H10	37	28	AVSS	-	
46	H9	38	29	P14	F	N
				AN04		
				INT03_1		
				IC02_2		
				SIN0_1		
47	G10	39	30	P15	F	N
				AN05		
				IC03_2		
				SOT0_1 (SDA0_1)		
				INT14_0		
48	G9	-	-	P16	F	N
				AN06		
				SCK0_1 (SCL0_1)		
				INT15_0		
49	F10	40	-	P17	F	N
				AN07		
				SIN2_2		
				INT04_1		
50	H11	41	31	AVCC	-	
51	F11	42	32	AVRH	-	
52	G11	43	33	AVRL	-	
53	F9	44	-	P18	F	M
				AN08		
				SOT2_2 (SDA2_2)		
54	E11	45	-	P19	F	M
				AN09		
				SCK2_2 (SCL2_2)		
55	E10	-	-	P1A	F	N
				AN10		
				SIN4_1		
				INT05_1		
				IC00_1		

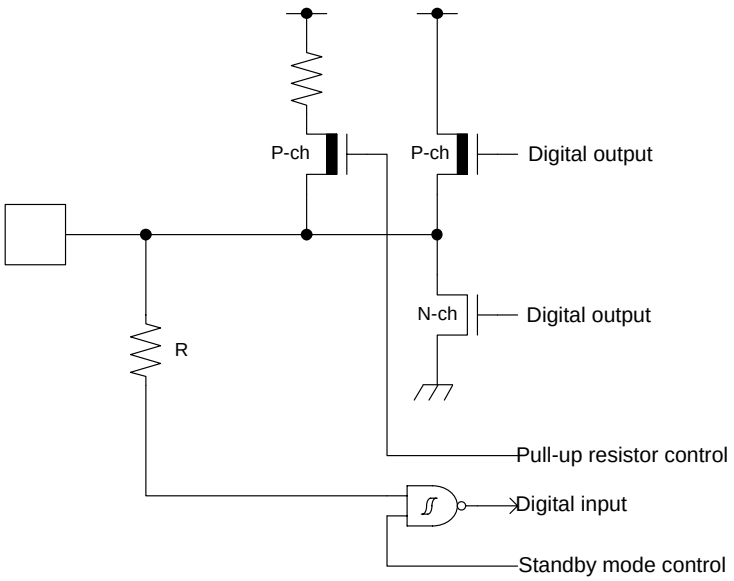
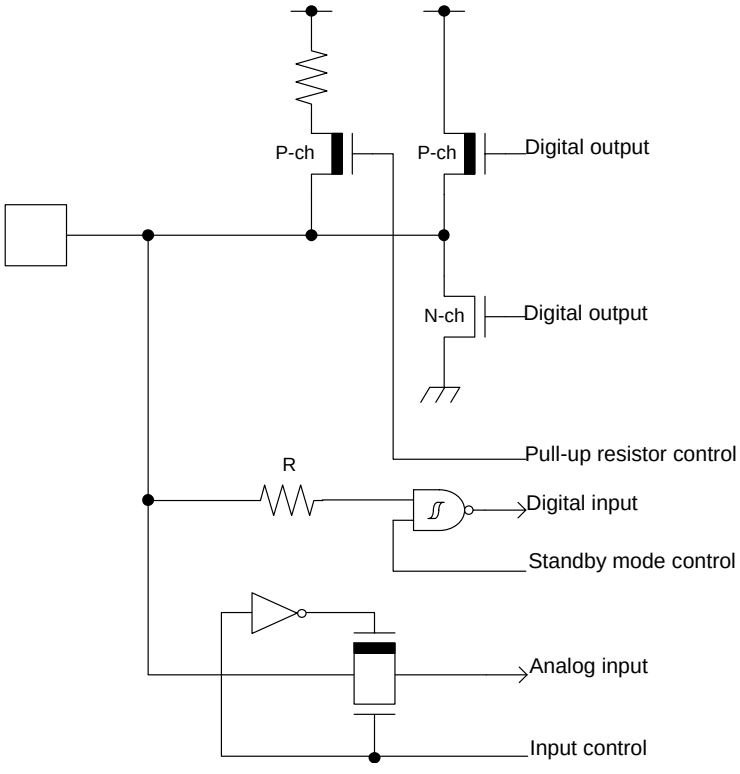
Pin No				Pin Name	I/O circuit type	Pin state type
LQFP-80	BGA-96	LQFP-64 QFN-64	LQFP-48 QFN-48			
56	E9	-	-	P1B	F	N
				AN11		
				SOT4_1 (SDA4_1)		
				IC01_1		
				INT20_2		
57	D10	46	34	P23	F	M
				SCK0_0 (SCL0_0)		
				TIOA7_1		
				AN12		
58	D9	47	35	P22	F	M
				SOT0_0 (SDA0_0)		
				TIOB7_1		
				AN13		
		-	-	ZIN1_1		
59	C11	48	36	P21	F	N
				SIN0_0		
				INT06_1		
				WKUP2		
				BIN1_1		
				AN14		
60	C10	-	-	P20	E	N
				INT05_0		
				CROUT_0		
				AIN1_1		
61	A10	49	37	P00	E	J
				TRSTX		
62	B9	50	38	P01	E	J
				TCK		
				SWCLK		
63	B11	51	39	P02	E	J
				TDI		
64	A9	52	40	P03	E	J
				TMS		
				SWDIO		
65	B8	53	41	P04	E	J
				TDO		
				SWO		
66	A8	-	-	P07	E	L
				ADTG_0		
				INT23_1		

Pin No				Pin Name	I/O circuit type	Pin state type
LQFP-80	BGA-96	LQFP-64 QFN-64	LQFP-48 QFN-48			
76	C4	60	44	P60 SIN5_0 TIOA2_2 INT15_1 WKUP3 IGTRG_1 AN21	J*	N
77	A4	61	45	USBVCC	-	
78	A3	62	46	P80 UDM0 INT16_1	H	H
79	A2	63	47	P81 UDP0 INT17_1	H	H
80	A1	64	48	VSS	-	
-	A5, A7, A11, B2, B10, C3, C9, F1, F2, F3, J3, J9, K2, K10, L6	-	-	VSS	-	

*: 5 V tolerant I/O

5. I/O Circuit Type

Type	Circuit	Remarks
A		It is possible to select the main oscillation / GPIO function When the main oscillation is selected. • Oscillation feedback resistor : Approximately 1 MΩ • With Standby mode control When the GPIO is selected. • CMOS level output. • CMOS level hysteresis input • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50 kΩ • I_{OH}= -4 mA, I_{OL}= 4 mA
B		• CMOS level hysteresis input • Pull-up resistor : Approximately 50 kΩ

Type	Circuit	Remarks
E		• CMOS level output • CMOS level hysteresis input • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50 kΩ • I_{OH}= -4 mA, I_{OL}= 4 mA • When this pin is used as an I^2C pin, the digital output P-ch transistor is always off • +B input is available
F		• CMOS level output • CMOS level hysteresis input • With input control • Analog input • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50 kΩ • I_{OH}= -4 mA, I_{OL}= 4 mA • When this pin is used as an I^2C pin, the digital output P-ch transistor is always off • +B input is available

6. Handling Precautions

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Cypress semiconductor devices.

6.1 Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

Recommended Operating Conditions

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

Processing and Protection of Pins

These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

1. Preventing Over-Voltage and Over-Current Conditions

   Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.
2. Protection of Output Pins

   Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device.
   Therefore, avoid this type of connection.
3. Handling of Unused Input Pins

   Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

Latch-up

Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNPN junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

1. Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.
2. Be sure that abnormal current flows do not occur during the power-on sequence.

Observance of Safety Regulations and Standards

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

Fail-Safe Design

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

Precautions Related to Usage of Devices

Cypress semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

6.2 Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Cypress's recommended conditions. For detailed information about mount conditions, contact your sales representative.

Lead Insertion Type

Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Cypress recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

Surface Mount Type

Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. Cypress. recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Cypress ranking of recommended conditions.

Lead-Free Packaging

CAUTION: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

Storage of Semiconductor Devices

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

1. Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product. Store products in locations where temperature changes are slight.
2. Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5°C and 30°C.
   When you open Dry Package that recommends humidity 40% to 70% relative humidity.
3. When necessary, Cypress. packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.
4. Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

Baking

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Cypress recommended conditions for baking.

Condition: 125°C/24 h

7. Handling Devices

Power supply pins

In products with multiple VCC and VSS pins, respective pins at the same potential are interconnected within the device in order to prevent malfunctions such as latch-up. However, all of these pins should be connected externally to the power supply or ground lines in order to reduce electromagnetic emission levels, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating.

Moreover, connect the current supply source with each Power supply pin and GND pin of this device at low impedance. It is also advisable that a ceramic capacitor of approximately 0.1 µF be connected as a bypass capacitor between each Power supply pin and GND pin, between AVCC pin and AVSS pin, between AVRH pin and AVRL pin near this device.

Stabilizing power supply voltage

A malfunction may occur when the power supply voltage fluctuates rapidly even though the fluctuation is within the recommended operating conditions of the VCC power supply voltage. As a rule, with voltage stabilization, suppress the voltage fluctuation so that the fluctuation in VCC ripple (peak-to-peak value) at the commercial frequency (50 Hz/60 Hz) does not exceed 10% of the VCC value in the recommended operating conditions, and the transient fluctuation rate does not exceed 0.1 V/µs when there is a momentary fluctuation on switching the power supply.

Crystal oscillator circuit

Noise near the X0/X1 and X0A/X1A pins may cause the device to malfunction. Design the printed circuit board so that X0/X1, X0A/X1A pins, the crystal oscillator, and the bypass capacitor to ground are located as close to the device as possible.

It is strongly recommended that the PC board artwork be designed such that the X0/X1 and X0A/X1A pins are surrounded by ground plane as this is expected to produce stable operation.

Evaluate oscillation of your using crystal oscillator by your mount board.

Sub crystal oscillator

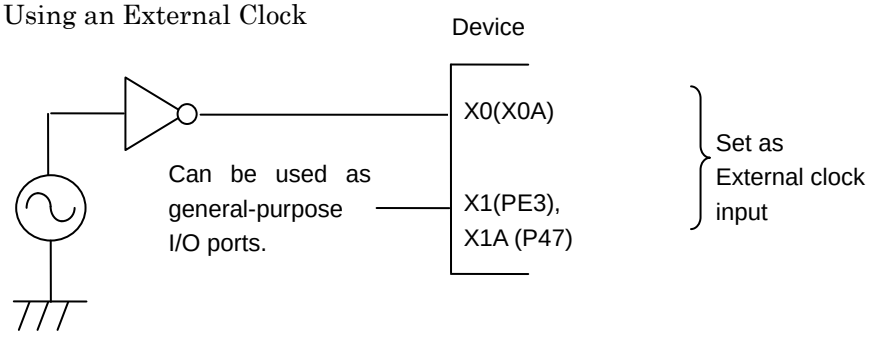
This series sub oscillator circuit is low gain to keep the low current consumption. The crystal oscillator to fill the following conditions is recommended for sub crystal oscillator to stabilize the oscillation.

- Surface mount type
  Size : More than 3.2 mm × 1.5 mm
  Load capacitance : Approximately 6 pF to 7 pF
- Lead type
  Load capacitance : Approximately 6 pF to 7 pF

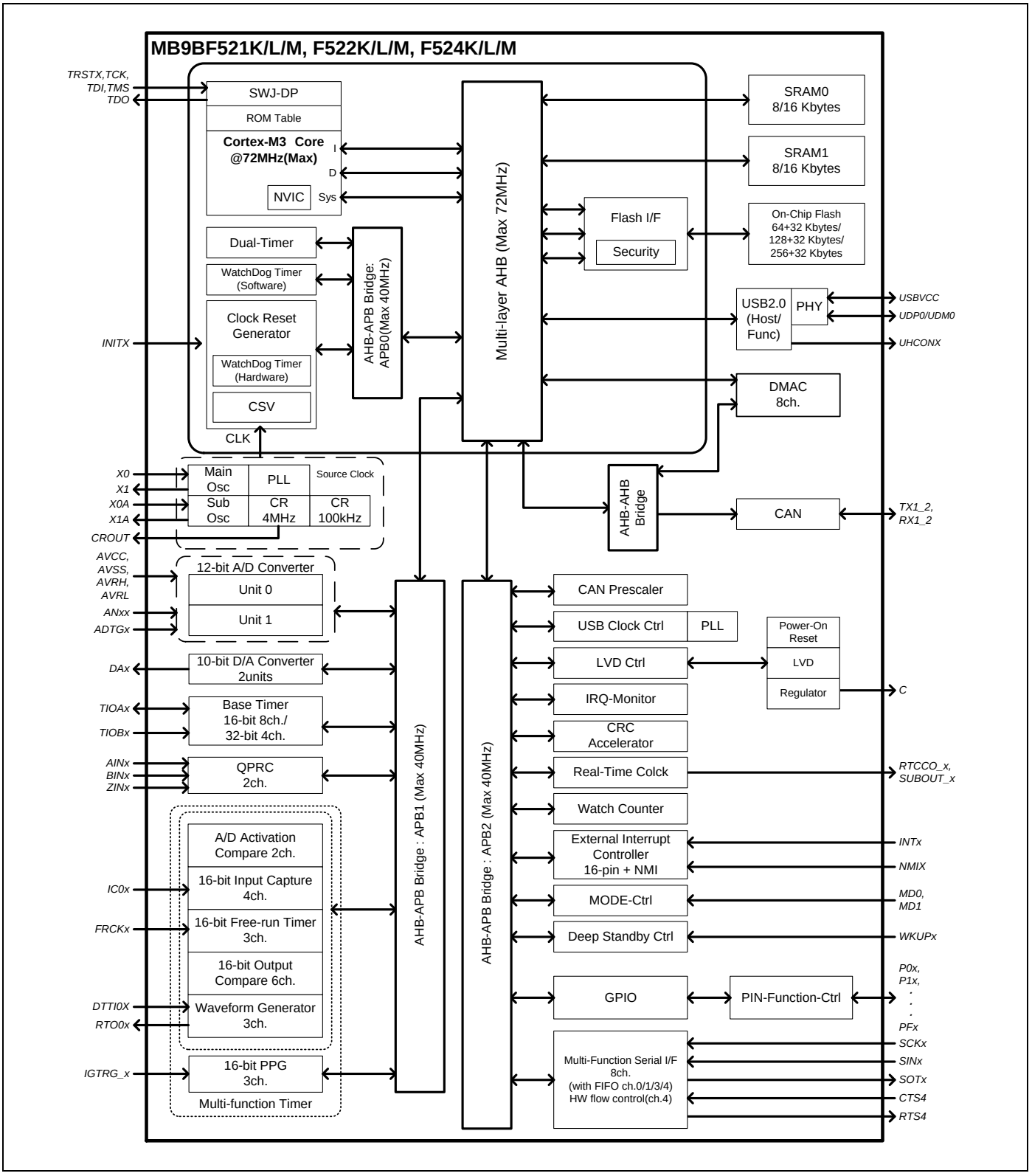
Using an external clock

When using an external clock as an input of the main clock, set X0/X1 to the external clock input, and input the clock to X0. X1(PE3) can be used as a general-purpose I/O port.
Similarly, when using an external clock as an input of the sub clock, set X0A/X1A to the external clock input, and input the clock to X0A. X1A (P47) can be used as a general-purpose I/O port.

- Example of Using an External Clock



8. Block Diagram



12.2 Recommended Operating Conditions

(V_{SS} = AV_{SS} = AVRL = 0.0V)

Parameter	Symbol	Conditions	Value		Unit	Remarks
			Min	Max		
Power supply voltage	V_{CC}	-	2.7*4	5.5	V	
Power supply voltage (3V power supply) for USB	$USBV_{CC}$	-	3.0	3.6 (≤ V_{CC})	V	*1
			2.7	5.5 (≤ V_{CC})		*2
Analog power supply voltage	AV_{CC}	-	2.7	5.5	V	AV_{CC} = V_{CC}
Analog reference voltage	AVRH	-	2.7	AV_{CC}	V	
	AVRL	-	AV_{SS}	AV_{SS}	V	
Smoothing capacitor	C_S	-	1	10	µF	For Regulator*3
Operating temperature	T_A	-	- 40	+ 105	°C	

*1: When P81/UDP0 and P80/UDM0 pins are used as USB (UDP0, UDM0).

*2: When P81/UDP0 and P80/UDM0 pins are used as GPIO (P81, P80).

*3: See “C Pin” in “Handling Devices" for the connection of the smoothing capacitor.

*4: In between less than the minimum power supply voltage and low voltage reset/interrupt detection voltage or more, instruction execution and low voltage detection function by built-in High-speed CR(including Main PLL is used) or bulit-in Low-speed CR is possible to operate only.

WARNING:

The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.
Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure. No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

12.3 DC Characteristics

12.3.1 Current Rating

(V_{CC} = AV_{CC} = $USBV_{CC}$ = 2.7V to 5.5V, V_{SS} = AV_{SS} = AVRL = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions		Value		Unit	Remarks
					Typ	Max		
Run mode current	I_{CC}	VCC	PLL Run mode	CPU : 72 MHz, Peripheral : 36 MHz	32.5	41	mA	*1, *5
				CPU:72 MHz, Peripheral clock stops NOP operation	18	23	mA	*1, *5
			High-speed CR Run mode	CPU/ Peripheral : 4 MHz*2	2.5	3.4	mA	*1
			Sub Run mode	CPU/ Peripheral : 32 kHz	110	980	µA	*1, *6
			Low-speed CR Run mode	CPU/ Peripheral : 100 kHz	130	1030	µA	*1
Sleep mode current	I_{CCS}		PLL Sleep mode	Peripheral : 36 MHz	22	28	mA	*1, *5
			High-speed CR Sleep mode	Peripheral : 4 MHz*2	1.6	2.6	mA	*1
			Sub Sleep mode	Peripheral : 32 kHz	96	955	µA	*1, *6
			Low-speed CR Sleep mode	Peripheral : 100 kHz	115	975	µA	*1

*1: When all ports are fixed.

*2: When setting it to 4 MHz by trimming.

*3: T_A=+25°C, V_{CC}=5.5 V

*4: T_A=+105°C, V_{CC}=5.5 V

*5: When using the crystal oscillator of 4 MHz(Including the current consumption of the oscillation circuit)

*6: When using the crystal oscillator of 32 kHz(Including the current consumption of the oscillation circuit)

(V_{CC} = AV_{CC} = $USBV_{CC}$ = 2.7V to 5.5V, V_{SS} = AV_{SS} = AVRL = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions		Value		Unit	Remarks
					Typ*2	Max*2		
Timer mode current	I_{CCT}	VCC	Main Timer mode	T_A = + 25°C, When LVD is off	4.1	4.8	mA	*1, *4
				T_A = + 105°C, When LVD is off	-	5.4	mA	*1, *4
	I_{CCT}		Sub Timer mode	T_A = + 25°C, When LVD is off	17	66	µA	*1, *5
				T_A = + 105°C, When LVD is off	-	835	µA	*1, *5
RTC mode current	I_{CCR}		RTC mode	T_A = + 25°C, When LVD is off	15	61	µA	*1, *5
				T_A = + 105°C, When LVD is off	-	680	µA	*1, *5
Stop mode current	I_{CCH}		Stop mode	T_A = + 25°C, When LVD is off	14	53	µA	*1
				T_A = + 105°C, When LVD is off	-	600	µA	*1
Deep Standby mode current	I_{CCRD}		Deep Standby RTC mode	T_A = + 25°C, When LVD is off, When RAM is off	2.2	11	µA	*1, *3, *5
				T_A = + 25°C, When LVD is off, When RAM is on	6.2	23	µA	*1, *3, *5
				T_A = + 105°C, When LVD is off, When RAM is off	-	155	µA	*1, *3, *5
				T_A = + 105°C, When LVD is off, When RAM is on		215	µA	*1, *3, *5
	I_{CCHD}		Deep Standby Stop mode	T_A = + 25°C, When LVD is off, When RAM is off	1.6	9.6	µA	*1, *3
				T_A = + 25°C, When LVD is off, When RAM is on	5.6	22	µA	*1, *3
				T_A = + 105°C, When LVD is off, When RAM is off	-	150	µA	*1, *3
				T_A = + 105°C, When LVD is off, When RAM is on		210	µA	*1, *3

*1: When all ports are fixed.

*2: V_{CC}=5.5 V

*3: RAM on/off setting is on-chip SRAM only.

*4: When using the crystal oscillator of 4 MHz(Including the current consumption of the oscillation circuit)

*5: When using the crystal oscillator of 32 kHz(Including the current consumption of the oscillation circuit)

12.4 AC Characteristics

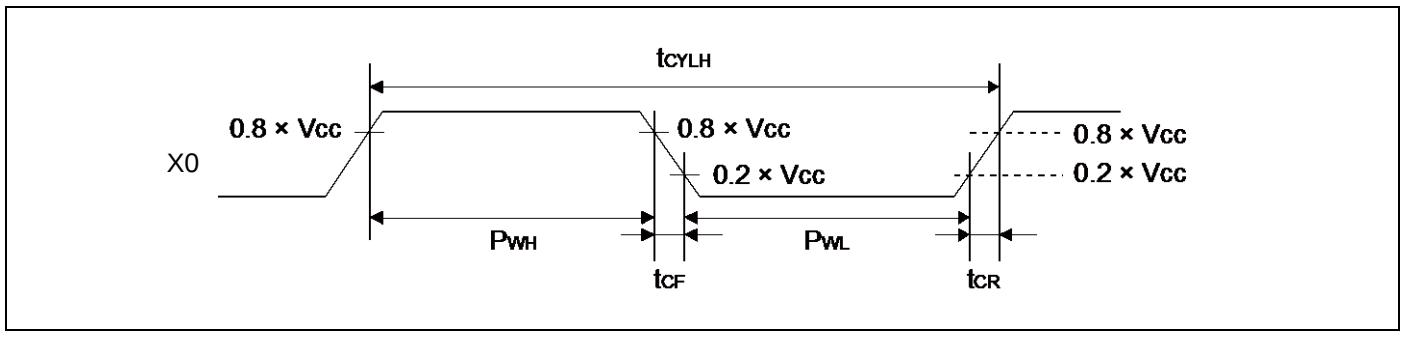
12.4.1 Main Clock Input Characteristics

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

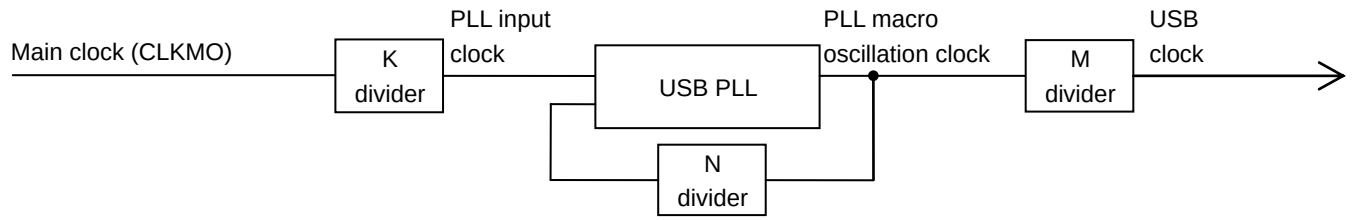
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input frequency	f_{CH}	X0, X1	$V_{CC} \geq 4.5$ V	4	48	MHz	When crystal oscillator is connected
			$V_{CC} < 4.5$ V	4	20		
			$V_{CC} \geq 4.5$ V	4	48	MHz	When using external Clock
			$V_{CC} < 4.5$ V	4	20		
Input clock cycle	t_{CYLH}		$V_{CC} \geq 4.5$ V	20.83	250	ns	When using external Clock
			$V_{CC} < 4.5$ V	50	250		
Input clock pulse width	-		P_{WH}/t_{CYLH}, P_{WL}/t_{CYLH}	45	55	%	When using external Clock
Input clock rising time and falling time	t_{CF}, t_{CR}		-	-	5	ns	When using external Clock
Internal operating clock frequency*1	f_{CM}	-	-	-	72	MHz	Master clock
	f_{CC}	-	-	-	72	MHz	Base clock (HCLK/FCLK)
	f_{CP0}	-	-	-	40	MHz	APB0 bus clock*2
	f_{CP1}	-	-	-	40	MHz	APB1 bus clock*2
	f_{CP2}	-	-	-	40	MHz	APB2 bus clock*2
Internal operating clock cycle time*1	t_{CYCC}	-	-	13.8	-	ns	Base clock (HCLK/FCLK)
	t_{CYCP0}	-	-	25	-	ns	APB0 bus clock*2
	t_{CYCP1}	-	-	25	-	ns	APB1 bus clock*2
	t_{CYCP2}	-	-	25	-	ns	APB2 bus clock*2

*1: For more information about each internal operating clock, see “Chapter: Clock” in “FM3 Family Peripheral Manual”.

*2: For about each APB bus which each peripheral is connected to, see “Block Diagram” in this datasheet.



USB PLL connection



12.4.6 Reset Input Characteristics

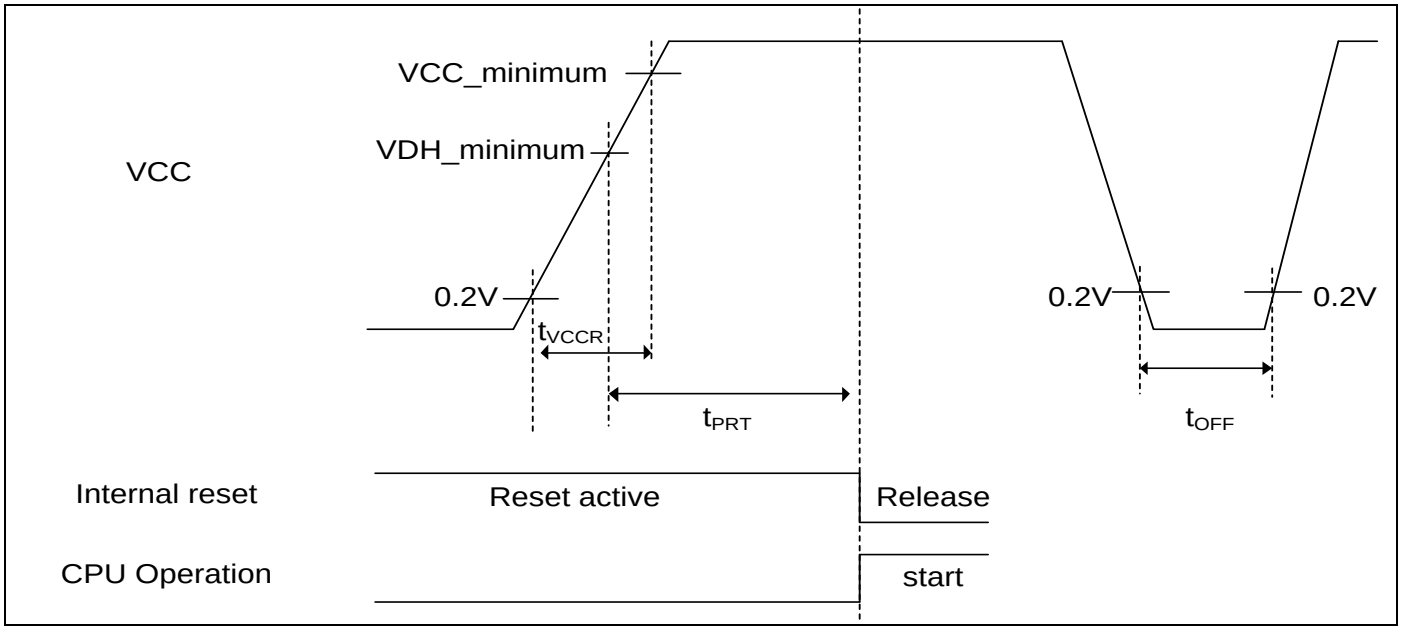
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Reset input time	t_{INITX}	INITX	-	500	-	ns	

12.4.7 Power-on Reset Timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
Power supply rising time	t_{VCCR}	VCC-	0	-	ms	
Power supply shut down time	t_{OFF}		1	-	ms	
Time until releasing Power-on reset	t_{PRT}		1.34	18.6	ms	



Glossary

- VCC_minimum: Minimum V_{CC} of recommended operating conditions
- VDH_minimum: Minimum detection voltage (when SVHR=00000) of Low-Voltage detection reset
  See "12.8. Low-Voltage Detection Characteristics"

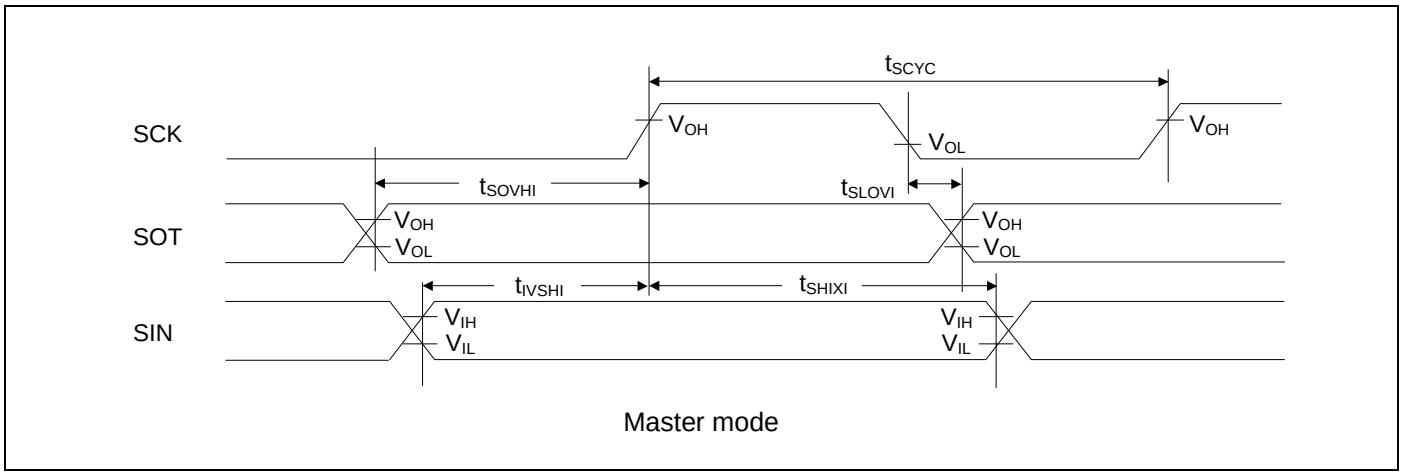
CSIO (SPI = 1, SCINV = 1)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

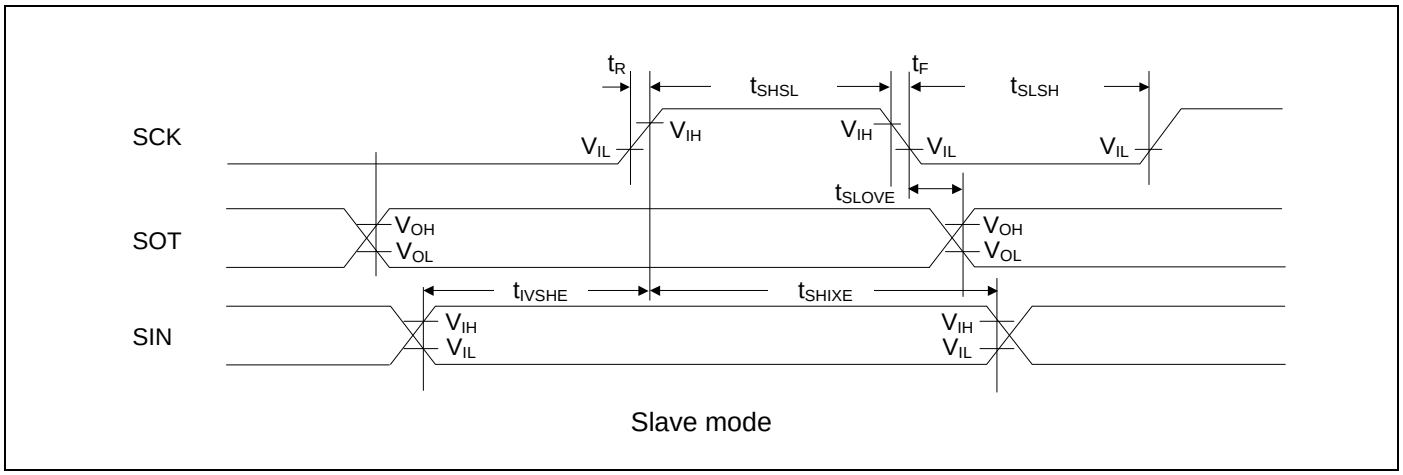
Parameter	Symbol	Pin name	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Master mode	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN → SCK ↑ setup time	t_{IVSHI}	SCKx, SINx		50	-	30	-	ns
SCK ↑ → SIN hold time	t_{SHIXI}	SCKx, SINx		0	-	0	-	ns
SOT → SCK ↑ delay time	t_{SOVHI}	SCKx, SOTx		$2t_{CYCP}$ - 30	-	$2t_{CYCP}$ - 30	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	Slave mode	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCKx, SOTx		-	50	-	30	ns
SIN → SCK ↑ setup time	t_{IVSHE}	SCKx, SINx		10	-	10	-	ns
SCK ↑ → SIN hold time	t_{SHIXE}	SCKx, SINx		20	-	20	-	ns
SCK falling time	t_F	SCKx		-	5	-	5	ns
SCK rising time	t_R	SCKx		-	5	-	5	ns

Notes:

- The above characteristics apply to CLK synchronous mode.
- t_{CYCP} indicates the APB bus clock cycle time.
  About the APB bus number which Multi-function serial is connected to, see “Block Diagram” in this data sheet.
- These characteristics only guarantee the same relocate port number.
  For example, the combination of SCKx_0 and SOTx_1 is not guaranteed.
- When the external load capacitance C_L = 30 pF.



Master mode

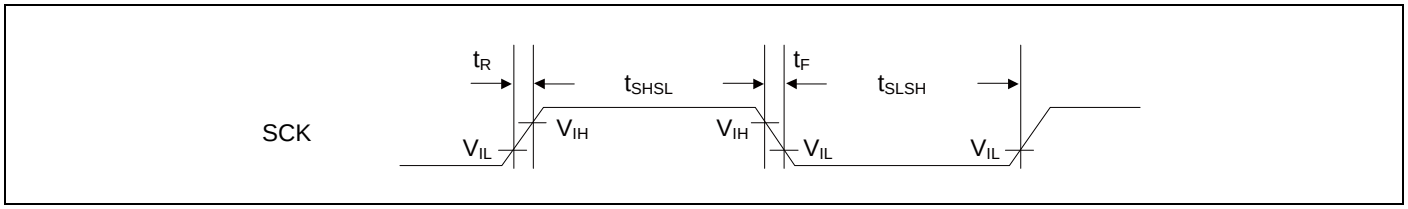


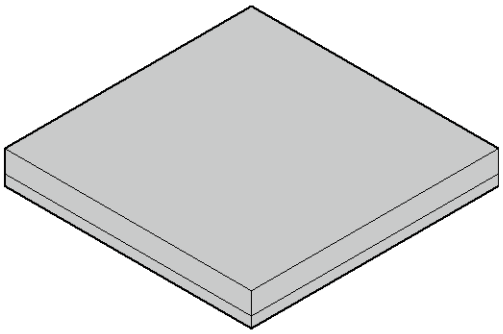
Slave mode

UART external clock input (EXT = 1)

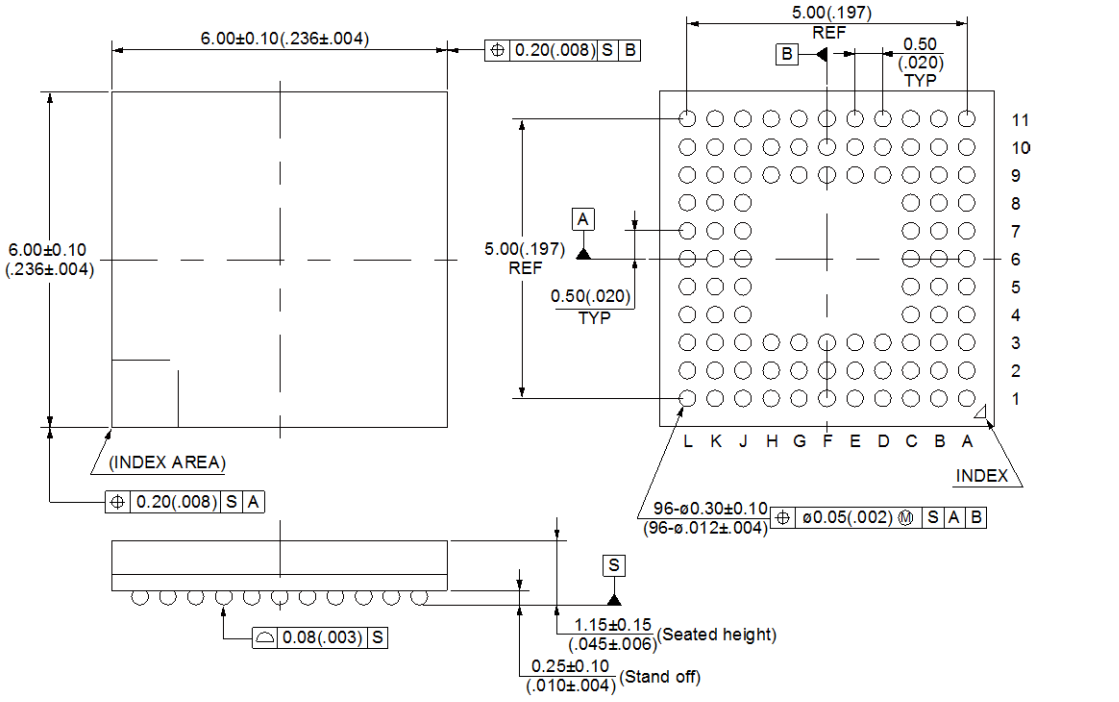
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Conditions	Min	Max	Unit	Remarks
Serial clock L pulse width	t_{SLSH}	C_L = 30 pF	t_{CYCP} + 10	-	ns	
Serial clock H pulse width	t_{SHSL}		t_{CYCP} + 10	-	ns	
SCK falling time	t_F		-	5	ns	
SCK rising time	t_R		-	5	ns	



96-pin plastic FBGA		
 (BGA-96P-M07)	Lead pitch	0.5 mm
	Package width × package length	6.00 mm × 6.00 mm
	Lead shape	Ball
	Sealing method	Plastic mold
	Mounting height	1.30 mm MAX
	Weight	0.08 g

96-pin plastic FBGA
(BGA-96P-M07)



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Page	Section	Change Results
7	Product Lineup Function	Corrected the number of A/D activating compare channels. 3ch. → 2ch. Revised Built-in CR . High-speed: 4MHz(± 2%) → 4MHz Low-speed: 100kHz(Typ) → 100kHz
8		Revised the footnote.
21	List Of Pin Functions List Of Pin Numbers	Corrected the pin number of ZIN1_1.
24	List Of Pin Functions	Corrected the pin number of ADTG_2.
29		Corrected pin numbers of SIN0_1 and SOT0_1.
31		Corrected the pin number of DTTI0X_2.
37	I/O Circuit Type	Corrested the I/O circuit figure. TYPE H : GPIO Digital input → GPIO Digital output
44	Handling Devices Sub Crystal Oscillator	Added the descriptions.
47	Block Diagram	Corrected the figure. -A/D Activation Compare: 3ch → 2ch
49	Memory Map Memory Map (2)	Added the explanatory note.
54	Pin Status In Each Cpu State List Of Pin Status	Added the pin function of selected Analog output about type L.
55		Corrected the footnote. Sub CR timer→ Low-speed CR tim
58	Electrical Characteristics 2. Recommended Operating Conditions	Added the note and footnote. Corrected the value of Analog reference voltage “AVRH”. Min.: AVss → 2.7
59	3. Dc Characteristics (1) Current Rating	Added notes and footnotes. Added the remarks of Icc. Added the frequency of main clock crystal oscillator in remarks.
63	4. Ac Characteristics (2) Sub Clock Input Characteristics	Added the footnote.
64	(3) Built-In CR Oscillation Characteristics Built-In High-Speed CR	Added "Frequency stabilization time" Added notes and footnotes.
66	(6) Power-On Reset Timing	Added "Timing until releaseing Power-on reset" Added the timing chart
68	(8) Csio Timing	Corrected the title. UART Timing → CSIO Timing Corrected the notefoot. UART → Multi-function serial
70,72,74		Corrected the notefoot. UART → Multi-function serial
79	(11) I^2c Timing	Revised the Condition. Revised the footnote.
81	5. 12-Bit A/D Converter Electrical Characteristics For The A/D Converter	Changed the name of parameter. •Non Linearity error → Integral Nonlinearity •Differential linearity error → Differential Nonlinearity Changed the Symbol. Of Zero transition voltage. $Vo_T \rightarrow V_{ZT}$ Changed the pin name. AN00 to AN26 → ANxx Corrected the value of V_{0T}, V_{FST}, Ts, Tstt, and reference voltage. Revides footnotes.
82		Change the figure. AN00 to AN26 → ANxx
83	Difinition Of 12-Bit A/D Converter Terms	•Linearity error → Integral Nonlinearity •Differential linearity error → Differential Nonlinearity $V_{0T} \rightarrow V_{ZT}$
84	6. 10-Bit D/A Converter Electrical Characteristics For The D/A Converter	•Revised the remark of IDDA. D/A operation → D/A 1unit operation Changed the name of parameter. •Linearity error → Integral Nonlinearity •Differential linearity error → Differential Nonlinearity