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What is "Embedded - Microcontrollers"?

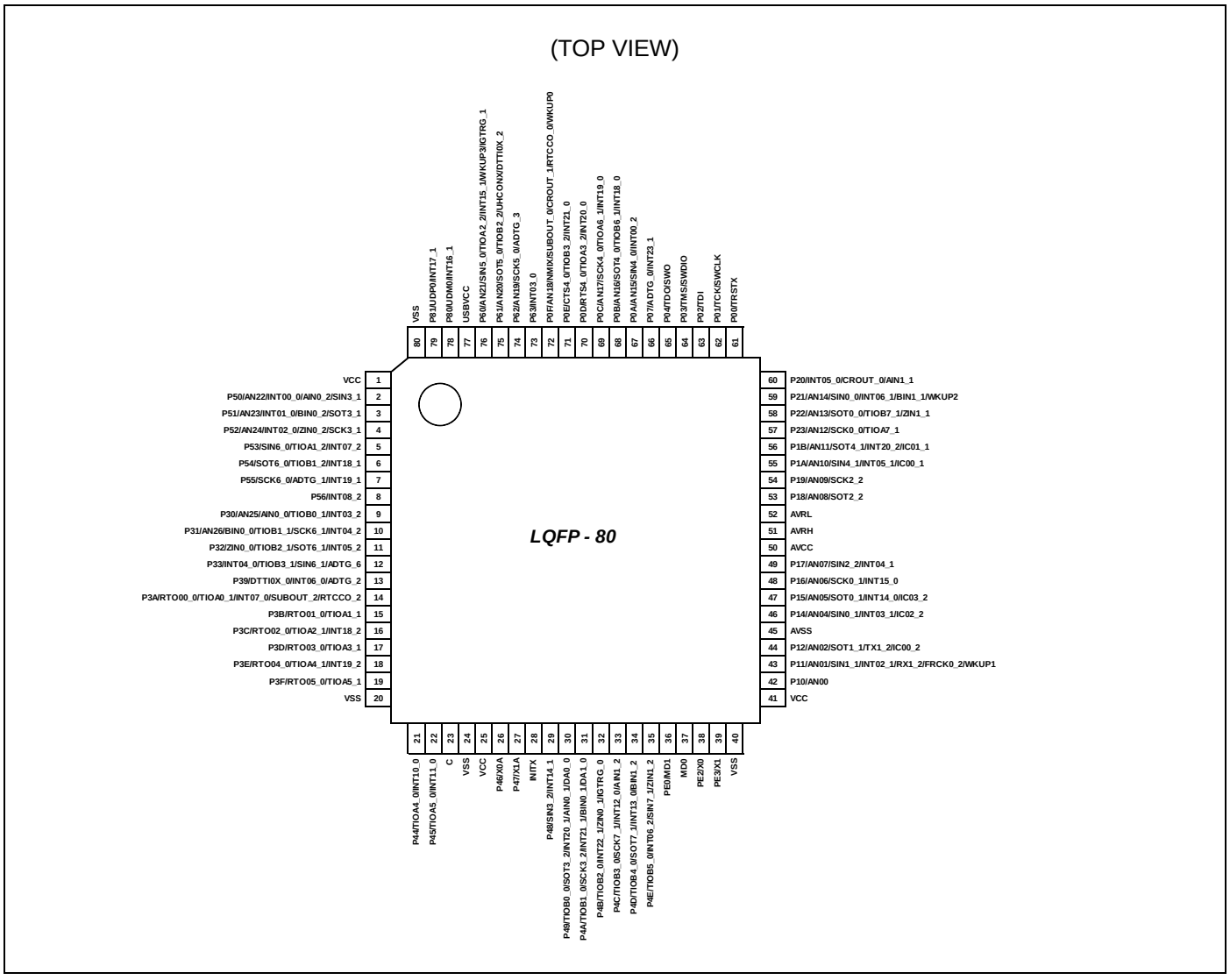
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, CSIO, I²C, LINbus, UART/USART, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	65
Program Memory Size	288KB (288K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 26x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb9bf524mpmc-g-jne2

3. Pin Assignment

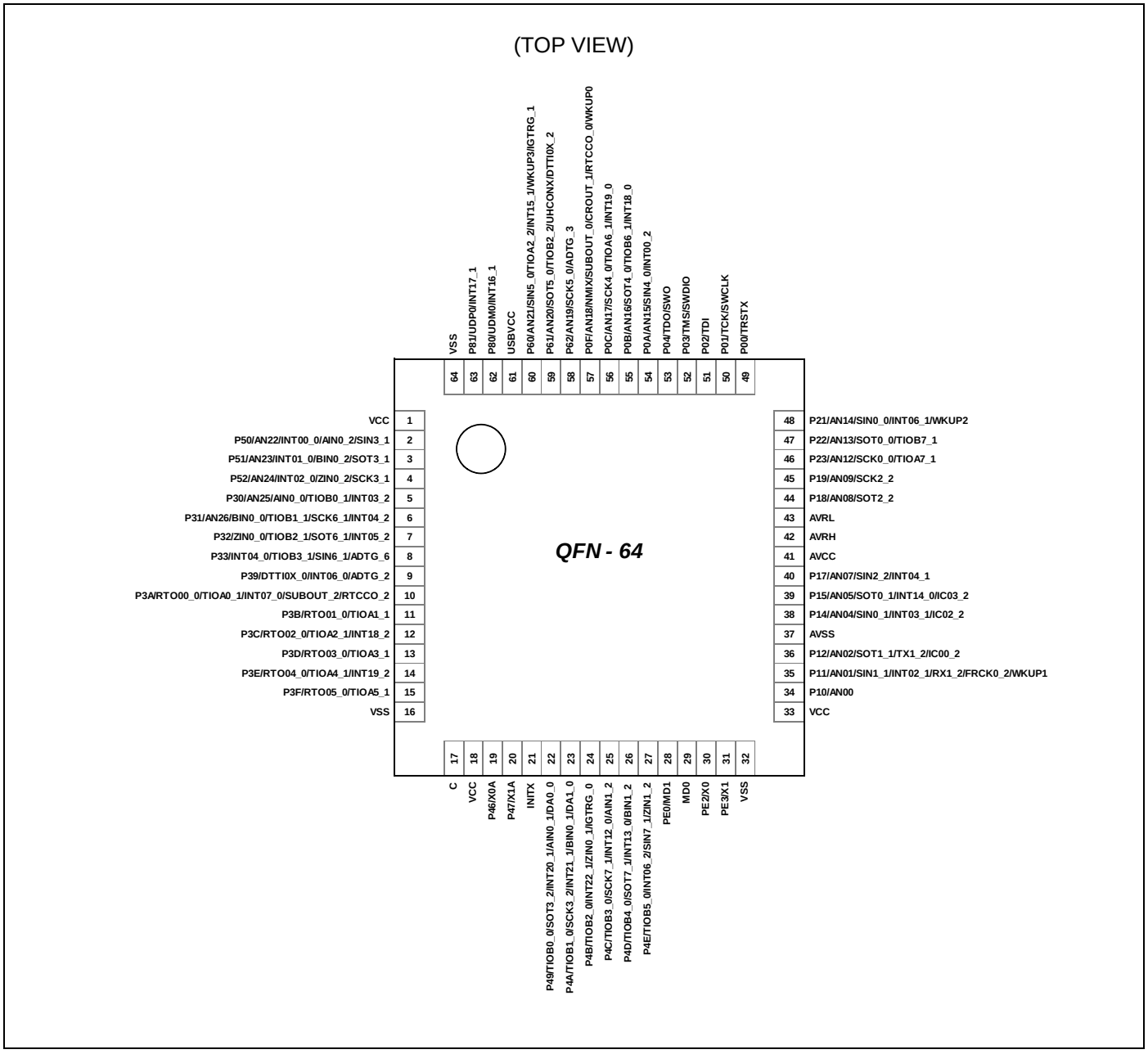
FPT-80P-M37/M40



Note:

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

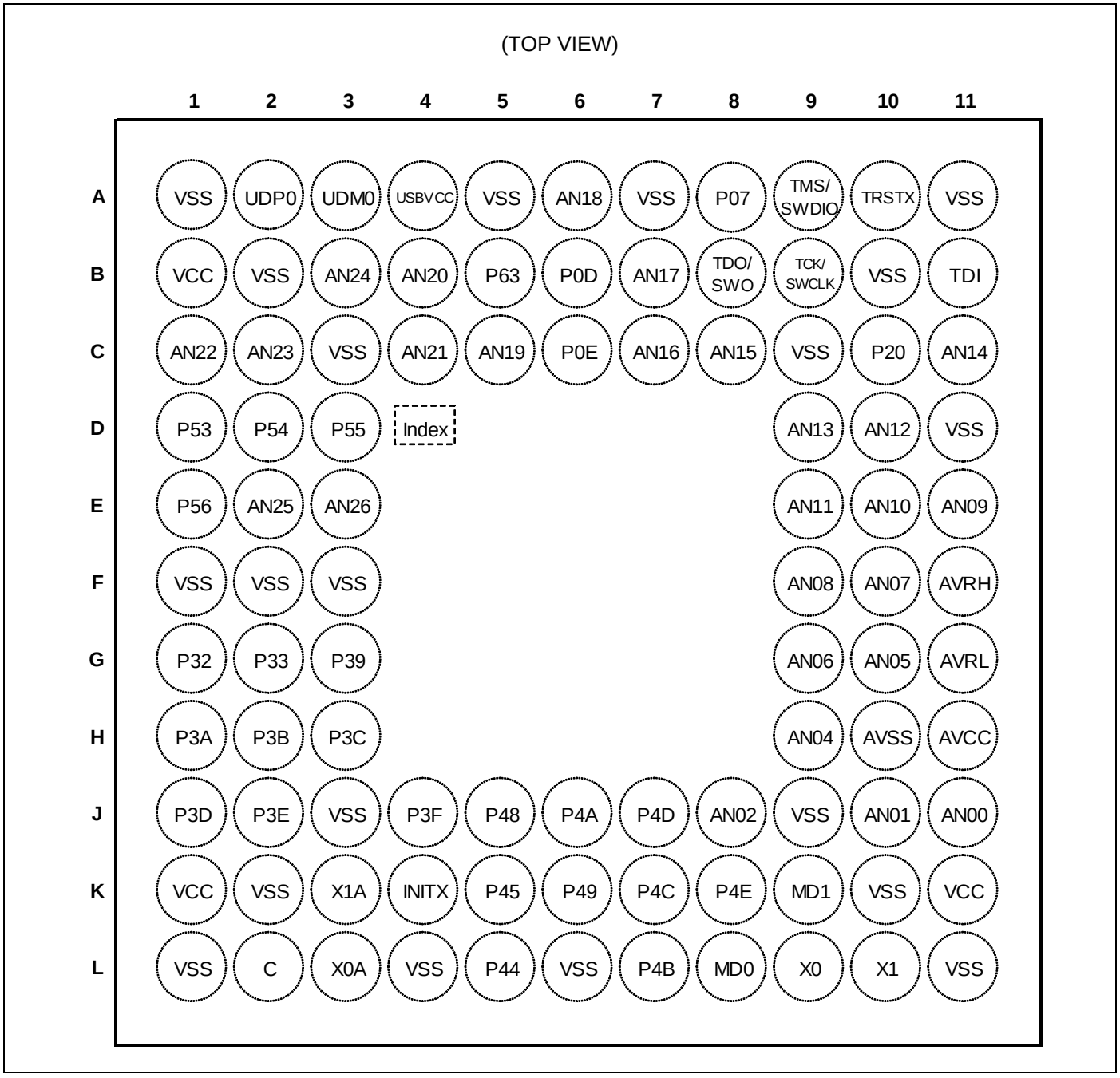
LCC-64P-M24



Note:

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

BGA-96P-M07

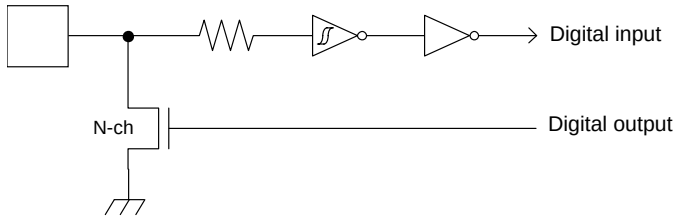
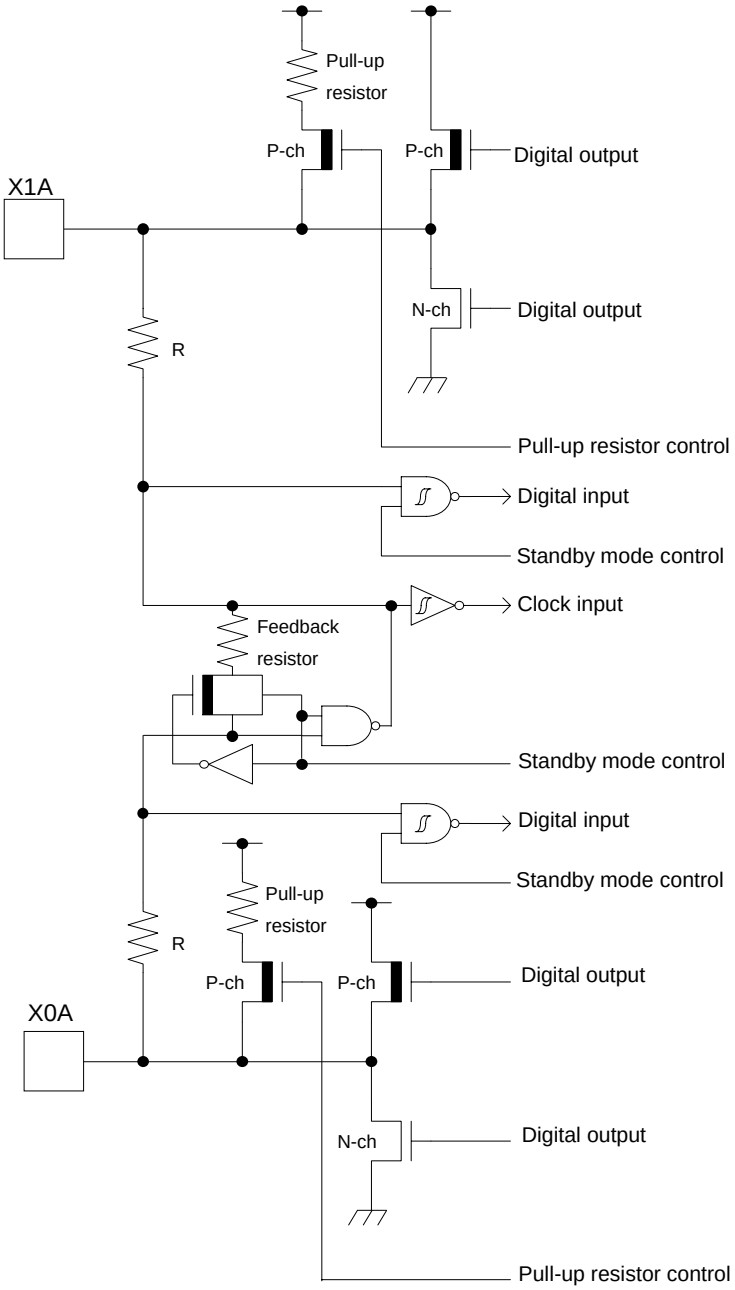


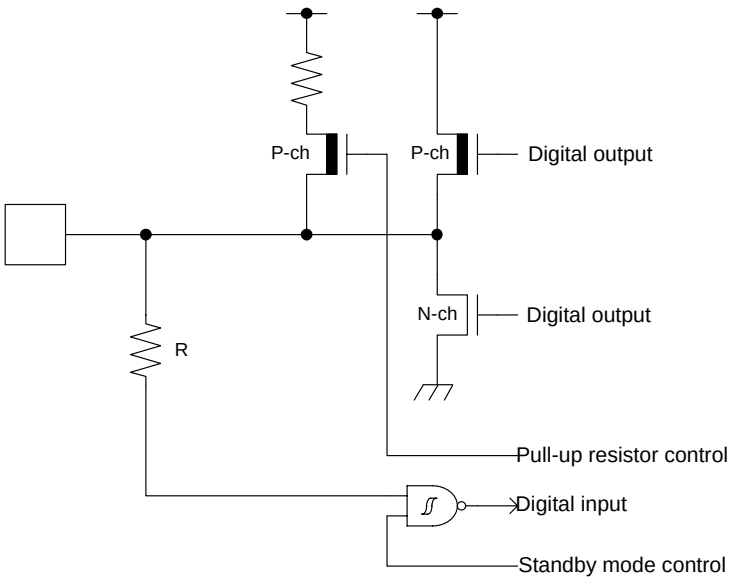
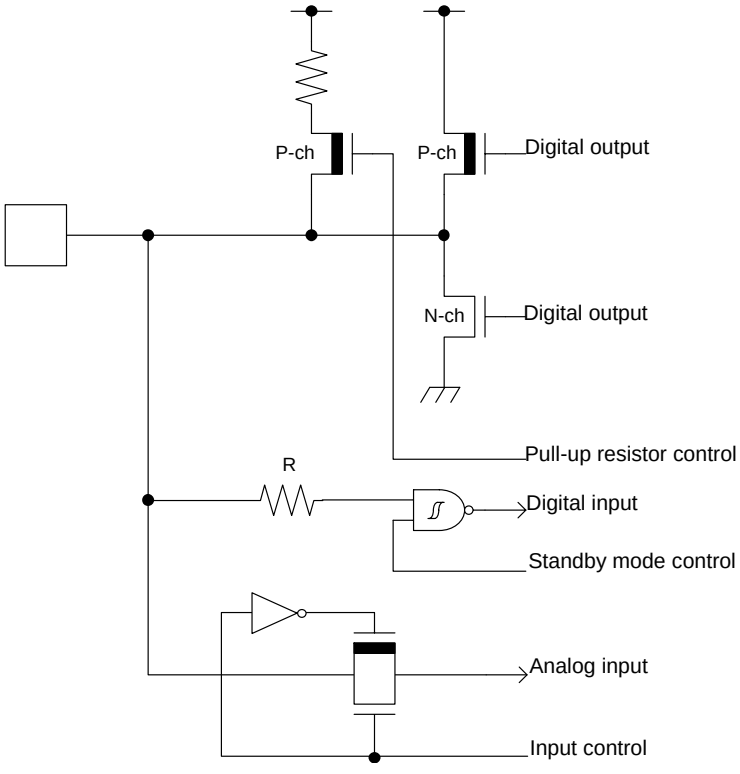
Note:

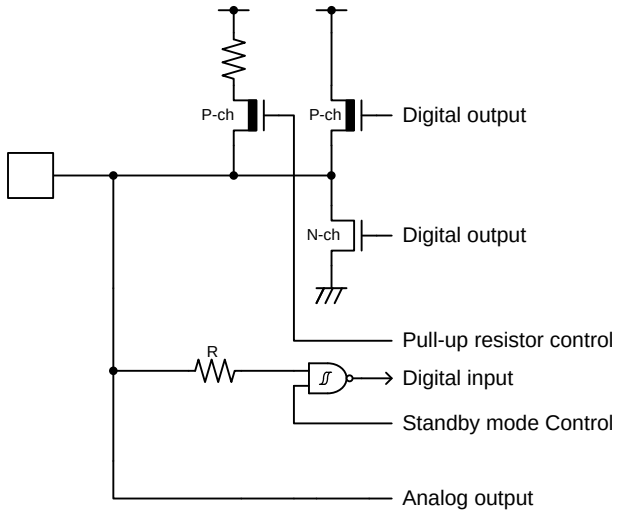
The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Pin No				Pin Name	I/O circuit type	Pin state type
LQFP-80	BGA-96	LQFP-64 QFN-64	LQFP-48 QFN-48			
18	J2	14	10	P3E RTO04_0 (PPG04_0) TIOA4_1 INT19_2	G	L
19	J4	15	11	P3F RTO05_0 (PPG04_0) TIOA5_1	G	K
20	L1	16	12	VSS	-	
21	L5	-	-	P44 TIOA4_0 INT10_0	G	L
22	K5	-	-	P45 TIOA5_0 INT11_0	G	L
23	L2	17	13	C	-	
24	L4	-	-	VSS	-	
25	K1	18	14	VCC	-	
26	L3	19	15	P46 X0A	D	F
27	K3	20	16	P47 X1A	D	G
28	K4	21	17	INITX	B	C
29	J5	-	-	P48 INT14_1 SIN3_2	E	L
30	K6	22	18	P49 TIOB0_0 INT20_1 DA0_0	L	L
			-	SOT3_2 (SDA3_2) AIN0_1		
31	J6	23	19	P4A TIOB1_0 INT21_1 DA1_0	L	L
			-	SCK3_2 (SCL3_2) BIN0_1		

Pin function	Pin name	Function description	Pin No			
			LQFP-80	BGA-96	LQFP-64 QFN-64	LQFP-48 QFN-48
External Interrupt	INT00_0	External interrupt request 00 input pin	2	C1	2	2
	INT00_2		67	C8	54	-
	INT01_0	External interrupt request 01 input pin	3	C2	3	3
	INT02_0	External interrupt request 02 input pin	4	B3	4	4
	INT02_1		43	J10	35	26
	INT03_0	External interrupt request 03 input pin	73	B5	-	-
	INT03_1		46	H9	38	29
	INT03_2		9	E2	5	-
	INT04_0	External interrupt request 04 input pin	12	G2	8	-
	INT04_1		49	F10	40	-
	INT04_2		10	E3	6	-
	INT05_0	External interrupt request 05 input pin	60	P20	-	-
	INT05_1		55	E10	-	-
	INT05_2		11	G1	7	-
	INT06_0	External interrupt request 06 input pin	13	G3	9	5
	INT06_1		59	C11	48	36
	INT06_2		35	K8	27	-
	INT07_0	External interrupt request 07 input pin	14	H1	10	6
	INT07_2		5	D1	-	-
	INT08_2	External interrupt request 08 input pin	8	E1	-	-
	INT10_0	External interrupt request 10 input pin	21	L5	-	-
	INT11_0	External interrupt request 11 input pin	22	K5	-	-
	INT12_0	External interrupt request 12 input pin	33	K7	25	-
	INT13_0	External interrupt request 13 input pin	34	J7	26	-
	INT14_0	External interrupt request 14 input pin	47	G10	39	30
	INT14_1		29	J5	-	-
	INT15_0	External interrupt request 15 input pin	48	G9	-	-
	INT15_1		76	C4	60	44
	INT16_1	External interrupt request 16 input pin	78	A3	62	46
	INT17_1	External interrupt request 17 input pin	79	A2	63	47
	INT18_0	External interrupt request 18 input pin	68	C7	55	-
	INT18_1		6	D2	-	-
	INT18_2		16	H3	12	8
	INT19_0	External interrupt request 19 input pin	59	C11	56	-
	INT19_1		7	D3	-	-
	INT19_2		18	J2	14	10

Type	Circuit	Remarks
C		• Open drain output • CMOS level hysteresis input
D		It is possible to select the sub oscillation / GPIO function When the sub oscillation is selected. • Oscillation feedback resistor : Approximately 5 MΩ • With Standby mode control When the GPIO is selected. • CMOS level output. • CMOS level hysteresis input • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50 kΩ • I_{OH}= -4 mA, I_{OL}= 4 mA

Type	Circuit	Remarks
E		• CMOS level output • CMOS level hysteresis input • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50 kΩ • I_{OH}= -4 mA, I_{OL}= 4 mA • When this pin is used as an I^2C pin, the digital output P-ch transistor is always off • +B input is available
F		• CMOS level output • CMOS level hysteresis input • With input control • Analog input • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50 kΩ • I_{OH}= -4 mA, I_{OL}= 4 mA • When this pin is used as an I^2C pin, the digital output P-ch transistor is always off • +B input is available

Type	Circuit	Remarks
L		• CMOS level output • CMOS level hysteresis input • With input control • Analog output • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50 kΩ • I_{OH} = -4 mA, I_{OL} = 4 mA

6. Handling Precautions

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Cypress semiconductor devices.

6.1 Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

Recommended Operating Conditions

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

Processing and Protection of Pins

These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

1. Preventing Over-Voltage and Over-Current Conditions

   Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.
2. Protection of Output Pins

   Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device.
   Therefore, avoid this type of connection.
3. Handling of Unused Input Pins

   Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

Latch-up

Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNPN junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

1. Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.
2. Be sure that abnormal current flows do not occur during the power-on sequence.

Observance of Safety Regulations and Standards

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

Fail-Safe Design

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

Static Electricity

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

1. Maintain relative humidity in the working environment between 40% and 70%. Use of an apparatus for ion generation may be needed to remove electricity.
2. Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.
3. Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ).
   Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.
4. Ground all fixtures and instruments, or protect with anti-static measures.
5. Avoid the use of styrofoam or other highly static-prone materials for storage of completed board assemblies.

6.3 Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

1. Humidity

   Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.
2. Discharge of Static Electricity

   When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.
3. Corrosive Gases, Dust, or Oil

   Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.
4. Radiation, Including Cosmic Radiation

   Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.
5. Smoke, Flame

   CAUTION: Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of Cypress products in other special environmental conditions should consult with sales representatives.

7. Handling Devices

Power supply pins

In products with multiple VCC and VSS pins, respective pins at the same potential are interconnected within the device in order to prevent malfunctions such as latch-up. However, all of these pins should be connected externally to the power supply or ground lines in order to reduce electromagnetic emission levels, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating.

Moreover, connect the current supply source with each Power supply pin and GND pin of this device at low impedance. It is also advisable that a ceramic capacitor of approximately 0.1 µF be connected as a bypass capacitor between each Power supply pin and GND pin, between AVCC pin and AVSS pin, between AVRH pin and AVRL pin near this device.

Stabilizing power supply voltage

A malfunction may occur when the power supply voltage fluctuates rapidly even though the fluctuation is within the recommended operating conditions of the VCC power supply voltage. As a rule, with voltage stabilization, suppress the voltage fluctuation so that the fluctuation in VCC ripple (peak-to-peak value) at the commercial frequency (50 Hz/60 Hz) does not exceed 10% of the VCC value in the recommended operating conditions, and the transient fluctuation rate does not exceed 0.1 V/µs when there is a momentary fluctuation on switching the power supply.

Crystal oscillator circuit

Noise near the X0/X1 and X0A/X1A pins may cause the device to malfunction. Design the printed circuit board so that X0/X1, X0A/X1A pins, the crystal oscillator, and the bypass capacitor to ground are located as close to the device as possible.

It is strongly recommended that the PC board artwork be designed such that the X0/X1 and X0A/X1A pins are surrounded by ground plane as this is expected to produce stable operation.

Evaluate oscillation of your using crystal oscillator by your mount board.

Sub crystal oscillator

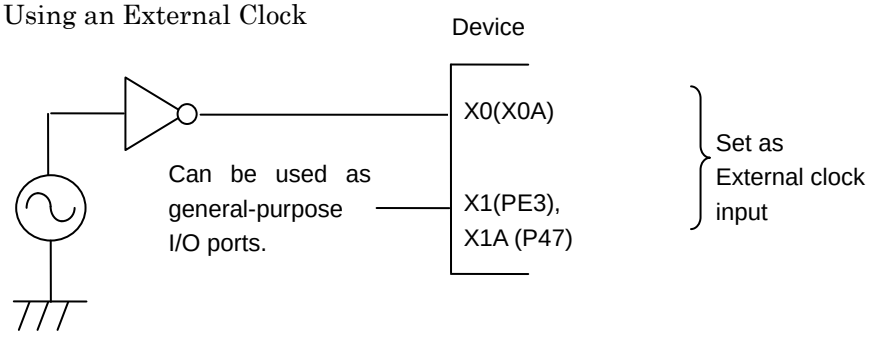
This series sub oscillator circuit is low gain to keep the low current consumption. The crystal oscillator to fill the following conditions is recommended for sub crystal oscillator to stabilize the oscillation.

- Surface mount type
  Size : More than 3.2 mm × 1.5 mm
  Load capacitance : Approximately 6 pF to 7 pF
- Lead type
  Load capacitance : Approximately 6 pF to 7 pF

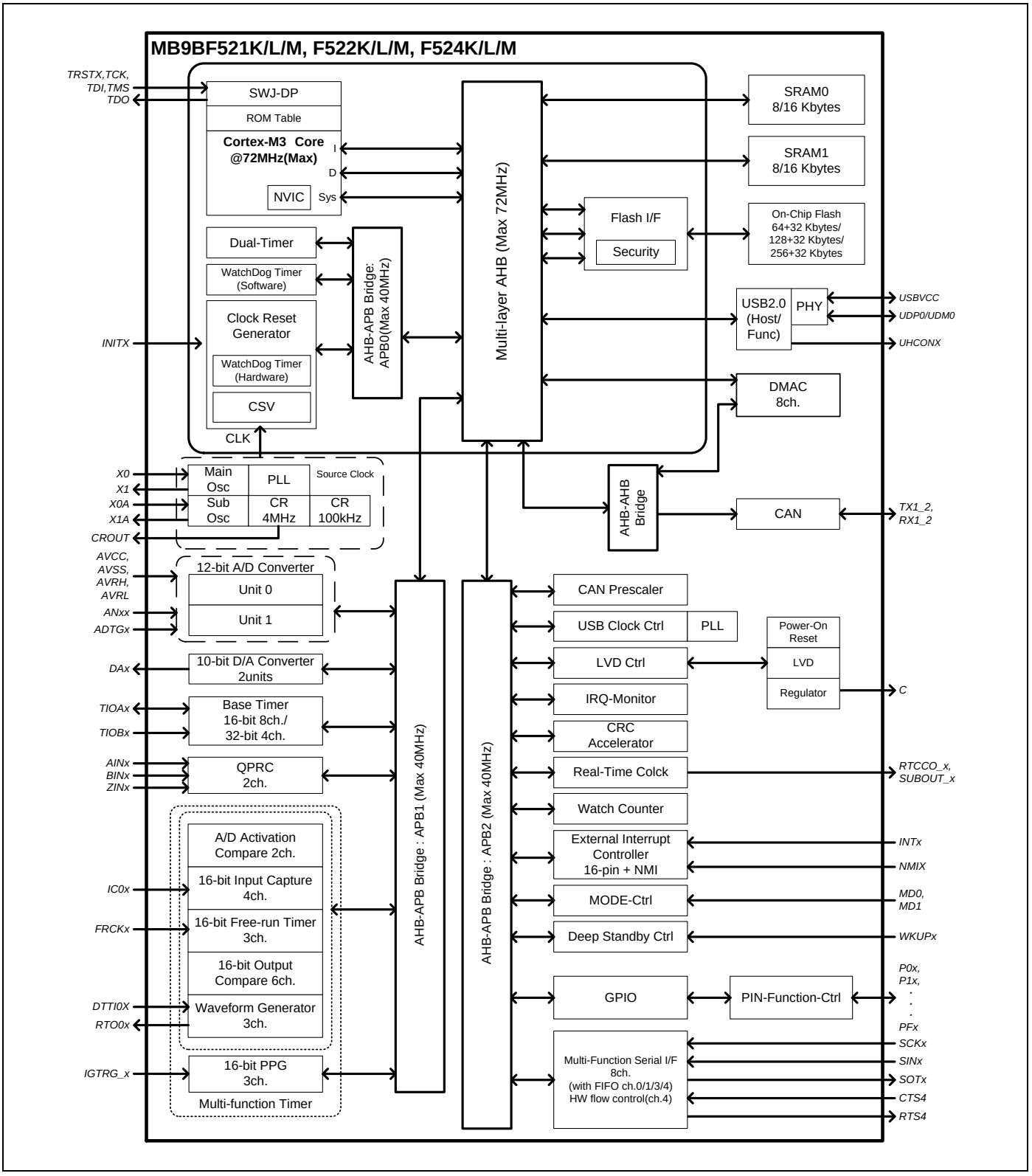
Using an external clock

When using an external clock as an input of the main clock, set X0/X1 to the external clock input, and input the clock to X0. X1(PE3) can be used as a general-purpose I/O port.
Similarly, when using an external clock as an input of the sub clock, set X0A/X1A to the external clock input, and input the clock to X0A. X1A (P47) can be used as a general-purpose I/O port.

- Example of Using an External Clock



8. Block Diagram



12. Electrical Characteristics

12.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1, *2	V_{CC}	V_{SS} - 0.5	V_{SS} + 6.5	V	
Power supply voltage (for USB)*1, *3	$USBV_{CC}$	V_{SS} - 0.5	V_{SS} + 6.5	V	
Analog power supply voltage*1, *4	AV_{CC}	V_{SS} - 0.5	V_{SS} + 6.5	V	
Analog reference voltage*1, *4	AVRH	V_{SS} - 0.5	V_{SS} + 6.5	V	
Input voltage*1	V_I	V_{SS} - 0.5	V_{CC} + 0.5 (≤ 6.5V)	V	Except for USB pin
		V_{SS} - 0.5	$USBV_{CC}$ + 0.5 (≤ 6.5 V)	V	USB pin
		V_{SS} - 0.5	V_{SS} + 6.5	V	5 V tolerant
Analog pin input voltage*1	V_{IA}	V_{SS} - 0.5	AV_{CC} + 0.5 (≤ 6.5 V)	V	
Output voltage*1	V_O	V_{SS} - 0.5	V_{CC} + 0.5 (≤ 6.5 V)	V	
Clamp maximum current	I_{CLAMP}	-2	+2	mA	*8
Clamp total maximum current	$\Sigma [I_{CLAMP}]$		+20	mA	*8
L level maximum output current*5	I_{OL}	-	10	mA	4 mA type
			20	mA	12 mA type
			39	mA	The pin doubled as USB I/O
L level average output current*6	I_{OLAV}	-	4	mA	4 mA type
			12	mA	12 mA type
			16.5	mA	The pin doubled as USB I/O
L level total maximum output current	$\sum I_{OL}$	-	100	mA	
L level total average output current*7	$\sum I_{OLAV}$	-	50	mA	
H level maximum output current*5	I_{OH}	-	- 10	mA	4 mA type
			- 20	mA	12 mA type
			- 39	mA	The pin doubled as USB I/O
H level average output current*6	I_{OHAV}	-	- 4	mA	4 mA type
			- 12	mA	12 mA type
			- 18	mA	The pin doubled as USB I/O
H level total maximum output current	$\sum I_{OH}$	-	- 100	mA	
H level total average output current*7	$\sum I_{OHAV}$	-	- 50	mA	
Power consumption	P_D	-	300	mW	
Storage temperature	T_{STG}	- 55	+ 150	°C	

*1: These parameters are based on the condition that $V_{SS} = AV_{SS} = 0$ V.

*2: V_{CC} must not drop below V_{SS} - 0.5 V.

*3: $USBV_{CC}$ must not drop below V_{SS} - 0.5 V.

*4: Ensure that the voltage does not exceed V_{CC} + 0.5 V, for example, when the power is turned on.

*5: The maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.

*6: The average output current is defined as the average current value flowing through any one of the corresponding pins for a 100 ms period.

*7: The total average output current is defined as the average current value flowing through all of corresponding pins for a 100 ms.

Low-Voltage Detection Current

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Typ	Max		
Low-voltage detection circuit (LVD) power supply current	I_{CCLVD}	VCC	At operation for reset Vcc = 5.5 V	0.13	0.3	µA	At not detect
			At operation for interrupt Vcc = 5.5 V	0.13	0.3	µA	At not detect

Flash Memory Current

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Typ	Max		
Flash memory write/erase current	$I_{CCFLASH}$	VCC	At Write/Erase	9.5	11.2	mA	*

*: The current at which to write or erase Flash memory, "$I_{CCFLASH}$" is added to "I_{CC}".

A/D Converter Current

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = AVRL = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Typ	Max		
Power supply current	I_{CCAD}	AVCC	At 1unit operation	0.69	0.90	mA	
			At stop	0.25	25.84	µA	
Reference power supply current	I_{CCAVRH}	AVRH	At 1unit operation AVRH=5.5 V	1.1	1.97	mA	
			At stop	0.2	3.4	µA	

D/A Converter Current

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current*1	IDDA*2	AVCC	At 1unit operation AV_{CC}=3.3 V	250	315	380	µA	
			At 1unit operation AV_{CC}=5.0 V	380	475	580	µA	
	IDSA		At stop	-	-	16	µA	

*1: No-load

*2: Generates the max current by the CODE about 0x200

12.4 AC Characteristics

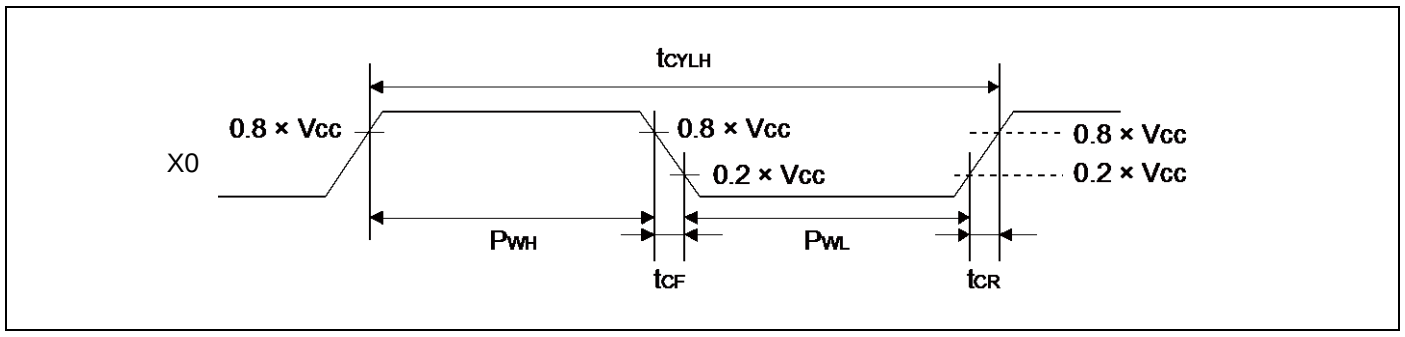
12.4.1 Main Clock Input Characteristics

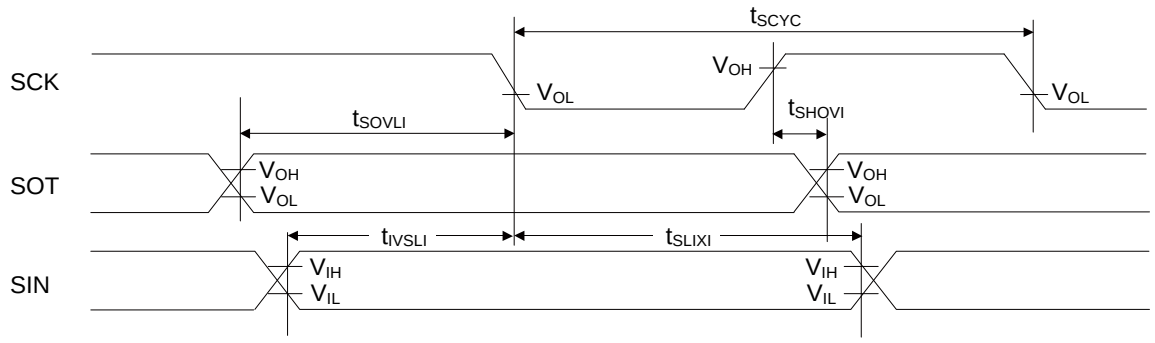
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input frequency	f_{CH}	X0, X1	$V_{CC} \geq 4.5$ V	4	48	MHz	When crystal oscillator is connected
			$V_{CC} < 4.5$ V	4	20		
			$V_{CC} \geq 4.5$ V	4	48	MHz	When using external Clock
			$V_{CC} < 4.5$ V	4	20		
Input clock cycle	t_{CYLH}		$V_{CC} \geq 4.5$ V	20.83	250	ns	When using external Clock
			$V_{CC} < 4.5$ V	50	250		
Input clock pulse width	-		P_{WH}/t_{CYLH}, P_{WL}/t_{CYLH}	45	55	%	When using external Clock
Input clock rising time and falling time	t_{CF}, t_{CR}		-	-	5	ns	When using external Clock
Internal operating clock frequency*1	f_{CM}	-	-	-	72	MHz	Master clock
	f_{CC}	-	-	-	72	MHz	Base clock (HCLK/FCLK)
	f_{CP0}	-	-	-	40	MHz	APB0 bus clock*2
	f_{CP1}	-	-	-	40	MHz	APB1 bus clock*2
	f_{CP2}	-	-	-	40	MHz	APB2 bus clock*2
Internal operating clock cycle time*1	t_{CYCC}	-	-	13.8	-	ns	Base clock (HCLK/FCLK)
	t_{CYCP0}	-	-	25	-	ns	APB0 bus clock*2
	t_{CYCP1}	-	-	25	-	ns	APB1 bus clock*2
	t_{CYCP2}	-	-	25	-	ns	APB2 bus clock*2

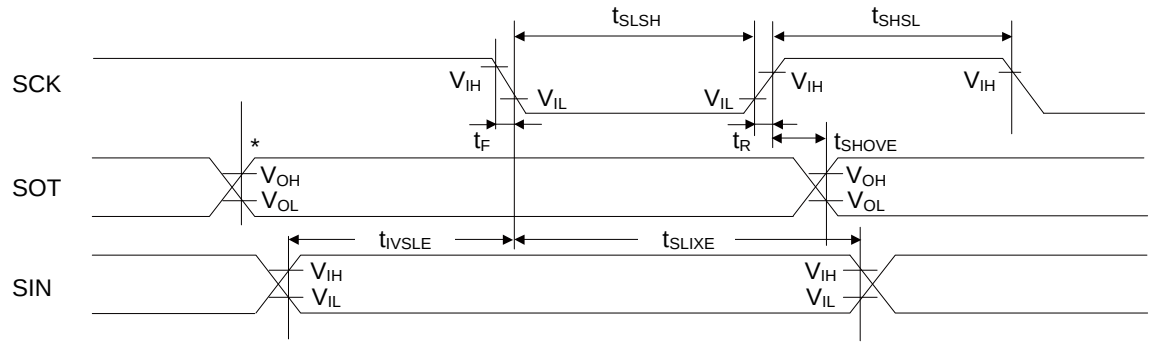
*1: For more information about each internal operating clock, see “Chapter: Clock” in “FM3 Family Peripheral Manual”.

*2: For about each APB bus which each peripheral is connected to, see “Block Diagram” in this datasheet.



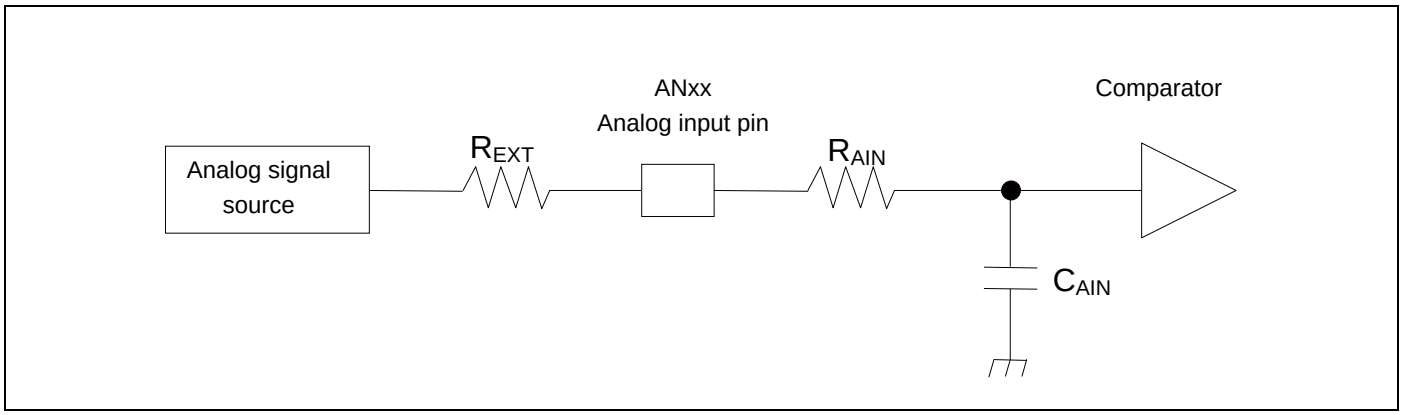


Master mode



Slave mode

*: Changes when writing to TDR register



(Equation 1) $t_S \geq (R_{AIN} + R_{EXT}) \times C_{AIN} \times 9$

t_S: Sampling time

R_{AIN}: input resistor of A/D = 1.5 kΩ at 4.5 V ≤ AV_{CC} ≤ 5.5 V ch.0 to ch.7
input resistor of A/D = 1.6 kΩ at 4.5 V ≤ AV_{CC} ≤ 5.5 V ch.8 to ch.15
input resistor of A/D = 1.7 kΩ at 4.5 V ≤ AV_{CC} ≤ 5.5 V ch.16 to ch.26
input resistor of A/D = 2.2 kΩ at 2.7 V ≤ AV_{CC} < 4.5 V ch.0 to ch.7
input resistor of A/D = 2.3 kΩ at 2.7 V ≤ AV_{CC} < 4.5 V ch.8 to ch.15
input resistor of A/D = 2.4 kΩ at 2.7 V ≤ AV_{CC} < 4.5 V ch.16 to ch.26

C_{AIN}: input capacity of A/D = 9.7 pF at 2.7 V ≤ AV_{CC} ≤ 5.5 V

R_{EXT}: Output impedance of external circuit

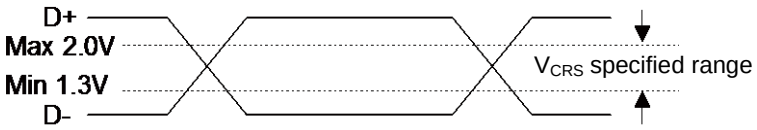
(Equation 2) $t_C = t_{CCK} \times 14$

t_C: Compare time

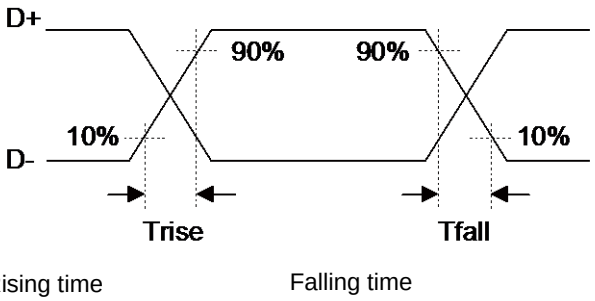
t_{CCK}: Compare clock cycle

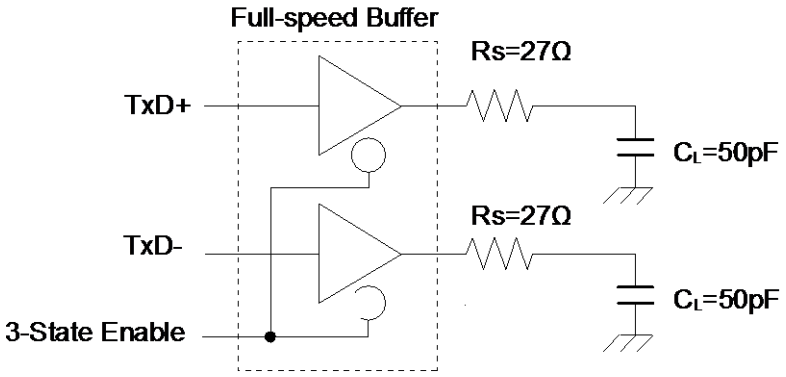
*3: The output drive capability of the driver is below 0.3 V at Low-State (V_{OL}) (to 3.6 V and 1.5 kΩ load), and 2.8 V or above (to ground and 15 kΩ load) at High-State (V_{OH}).

*4: The cross voltage of the external differential output signal (D + /D −) of USB I/O buffer is within 1.3 V to 2.0 V.



*5: They indicate rising time (Trise) and falling time (Tfall) of the full-speed differential data signal.
They are defined by the time between 10% and 90% of the output signal voltage.
For full-speed buffer, Tr/Tf ratio is regulated as within ± 10% to minimize RFI emission.





12.9 Flash Memory Write/Erase Characteristics

12.9.1 Write / Erase time

(V_{CC} = 2.7V to 5.5V, T_A = - 40°C to + 105°C)

Parameter		Value		Unit	Remarks
		Typ	Max		
Sector erase time	Large Sector	1.1	2.7	s	Includes write time prior to internal erase
	Small Sector	0.3	0.9		
Half word (16-bit) write time		16	310	µs	Not including system-level overhead time
Chip erase time		6.8	18	s	Includes write time prior to internal erase

*: The typical value is immediately after shipment, the maximam value is guarantee value under 10,000 cycle of erase/write.

12.9.2 Write cycles and data hold time

Erase/write cycles (cycle)	Data hold time (year)	Remarks
1,000	20*	
10,000	10*	

*: At average + 85°C

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