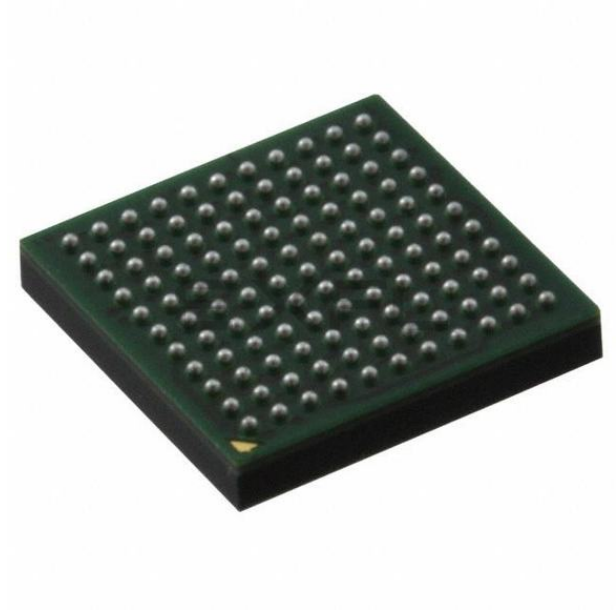

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB, USB OTG
Peripherals	DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	81
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 38x16b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	121-XFBGA
Supplier Device Package	121-XFBGA (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mk22fn512vdc12

Symbol	Description	Min.	Max.	Unit
V_{DD}	Digital supply voltage	–0.3	3.8	V
I_{DD}	Digital supply current	—	169	mA
V_{DIO}	Digital input voltage	–0.3	V_{DD} + 0.3	V
V_{AIO}	Analog[1]	–0.3	V_{DD} + 0.3	V
I_D	Maximum current single pin limit (applies to all digital pins)	–25	25	mA
V_{DDA}	Analog supply voltage	V_{DD} – 0.3	V_{DD} + 0.3	V
V_{USB0_DP}	USB0_DP input voltage	–0.3	3.63	V
V_{USB0_DM}	USB0_DM input voltage	–0.3	3.63	V
VREGIN	USB regulator input	–0.3	6.0	V
V_{BAT}	RTC battery supply voltage	–0.3	3.8	V

1. Analog pins are defined as pins that do not have an associated general purpose I/O port function.

2 General

2.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

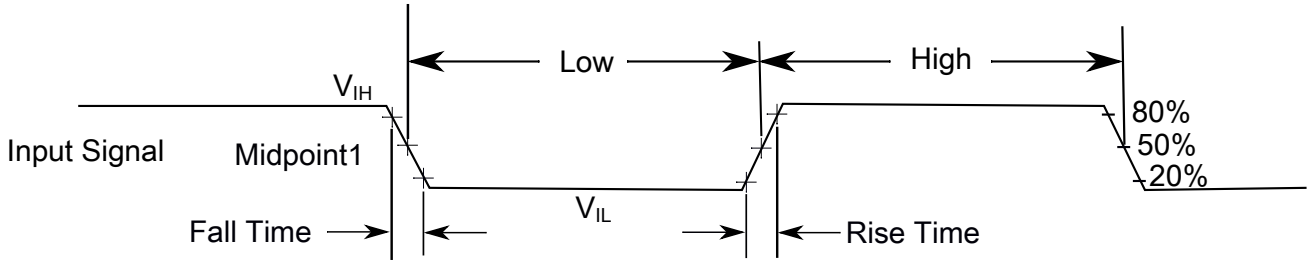

Figure 2. Input signal measurement reference

2.2 Nonswitching electrical specifications

Table 6. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	@ 70°C	—	9.5	21.25	µA	
	@ 85°C	—	15.3	34.65	µA	
	@ 105°C	—	30.1	66.05	µA	
I_{DD_VLLS2}	Very low-leakage stop mode 2 current at 3.0 V					
	@ -40°C to 25°C	—	1.9	2.45	µA	
	@ 70°C	—	4.5	8.50	µA	
	@ 85°C	—	6.8	12.15	µA	
	@ 105°C	—	13.0	25.50	µA	
I_{DD_VLLS1}	Very low-leakage stop mode 1 current at 3.0 V					
	@ -40°C to 25°C	—	0.73	1.42	µA	
	@ 70°C	—	1.8	3.90	µA	
	@ 85°C	—	3.0	5.25	µA	
	@ 105°C	—	5.9	10.80	µA	
I_{DD_VLLS0}	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit enabled					
	@ -40°C to 25°C	—	0.43	0.55	µA	
	@ 70°C	—	1.4	2.45	µA	
	@ 85°C	—	2.6	4.00	µA	
	@ 105°C	—	5.4	9.30	µA	
I_{DD_VLLS0}	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit disabled					
	@ -40°C to 25°C	—	0.14	0.24	µA	
	@ 70°C	—	1.1	2.15	µA	
	@ 85°C	—	2.3	3.85	µA	
	@ 105°C	—	5.1	9.00	µA	
I_{DD_VBAT}	Average current with RTC and 32kHz disabled at 3.0 V					
	@ -40°C to 25°C	—	0.18	0.21	µA	
	@ 70°C	—	0.66	0.86	µA	
	@ 85°C	—	1.52	2.24	µA	
	@ 105°C	—	2.92	4.30	µA	
I_{DD_VBAT}	Average current when CPU is not accessing RTC registers					
	@ 1.8V					
	• @ -40°C to 25°C	—	0.59	0.70	µA	15
	• @ 70°C	—	1.00	1.3	µA	
	• @ 85°C	—	1.76	2.59	µA	
	• @ 105°C	—	3.00	4.42	µA	
	@ 3.0V					

Table continues on the next page...

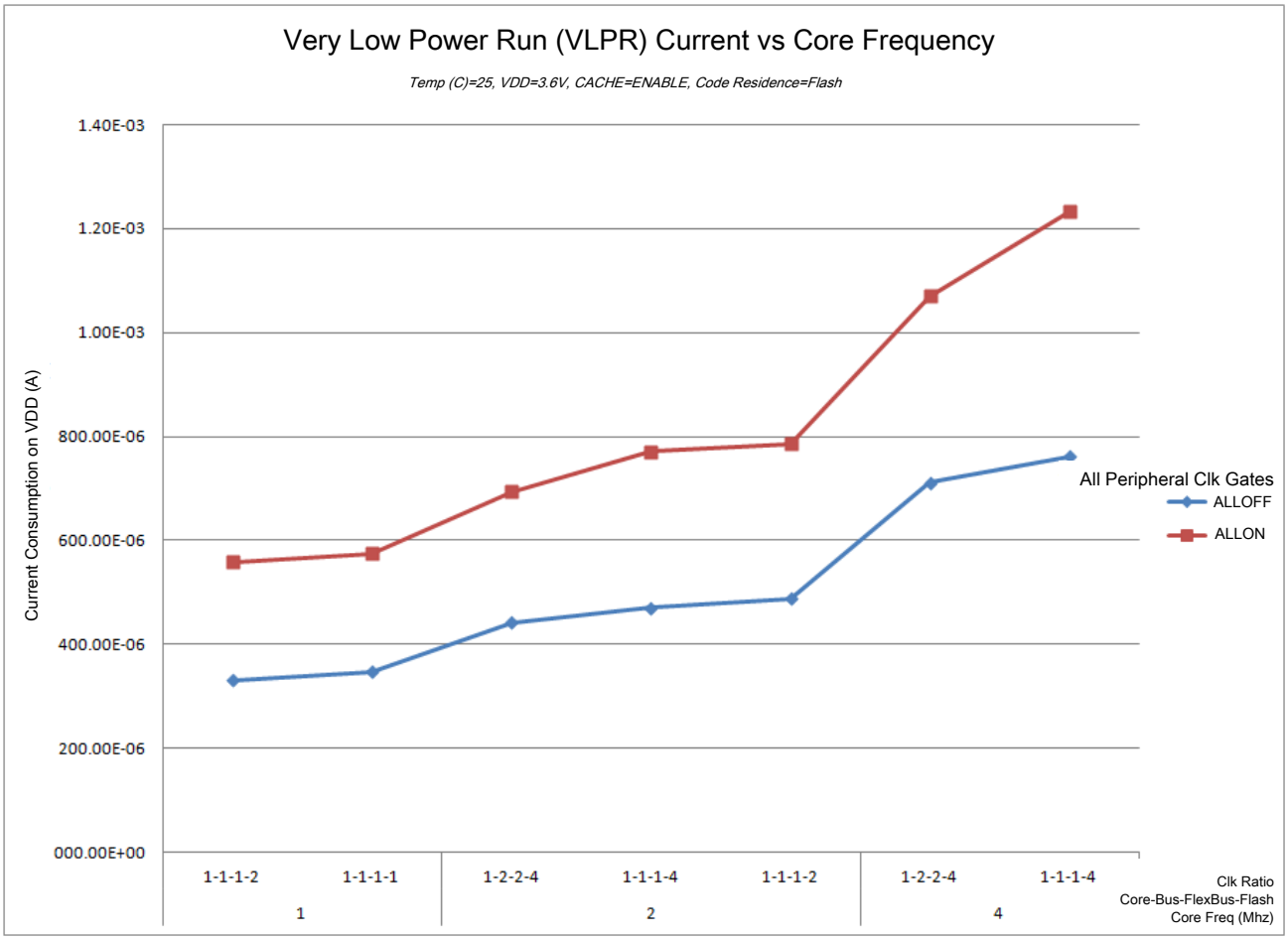

Figure 4. VLPR mode supply current vs. core frequency

2.2.6 EMC radiated emissions operating behaviors

Table 8. EMC radiated emissions operating behaviors for 64 LQFP package

Parameter	Conditions	Clocks	Frequency range	Level (Typ.)	Unit	Notes
V_{EME}	Device configuration, test conditions and EM testing per standard IEC 61967-2. Supply voltages: • VREGIN (USB) = 5.0 V • VDD = 3.3 V Temp = 25°C	FSYS = 120 MHz FBUS = 60 MHz External crystal = 8 MHz	150 kHz–50 MHz	14	dBuV	1, 2, 3
			50 MHz–150 MHz	23		
			150 MHz–500 MHz	23		
			500 MHz–1000 MHz	9		
			IEC level	L		4

1. Measurements were made per IEC 61967-2 while the device was running typical application code.
2. Measurements were performed on the 64LQFP device, MK22FN512VLH12 .

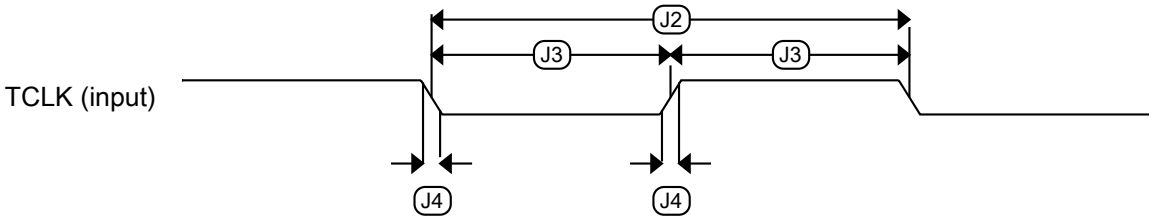

Figure 7. Test clock input timing

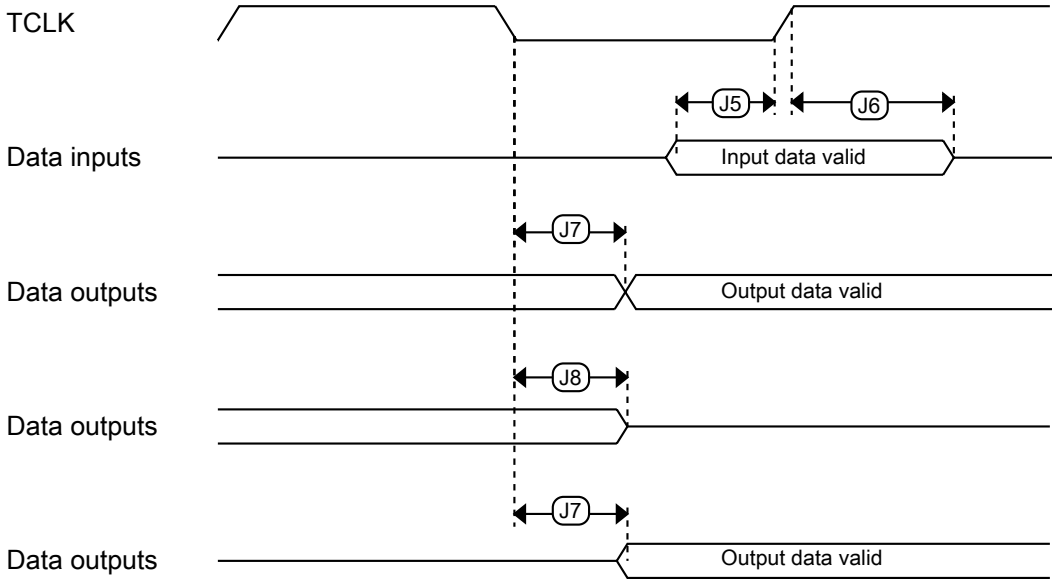

Figure 8. Boundary scan (JTAG) timing

3.3.1 MCG specifications

Table 16. MCG specifications

Symbol	Description		Min.	Typ.	Max.	Unit	Notes
f_{ints_ft}	Internal reference frequency (slow clock) — factory trimmed at nominal VDD and 25 °C		—	32.768	—	kHz	
Δf_{ints_t}	Total deviation of internal reference frequency (slow clock) over voltage and temperature		—	+0.5/-0.7	± 2	%	
f_{ints_t}	Internal reference frequency (slow clock) — user trimmed		31.25	—	39.0625	kHz	
$\Delta_{fdco\_res\_t}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM and SCFTRIM		—	± 0.3	± 0.6	$\%f_{dco}$	1
Δf_{dco_t}	Total deviation of trimmed average DCO output frequency over voltage and temperature		—	+0.5/-0.7	± 2	$\%f_{dco}$	1, 2
Δf_{dco_t}	Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0–70°C		—	± 0.3	± 1.5	$\%f_{dco}$	1
f_{intf_ft}	Internal reference frequency (fast clock) — factory trimmed at nominal VDD and 25°C		—	4	—	MHz	
Δf_{intf_ft}	Frequency deviation of internal reference clock (fast clock) over temperature and voltage — factory trimmed at nominal VDD and 25 °C		—	+1/-2	± 5	$\%f_{intf\_ft}$	
f_{intf_t}	Internal reference frequency (fast clock) — user trimmed at nominal VDD and 25 °C		3	—	5	MHz	
f_{loc_low}	Loss of external clock minimum frequency — RANGE = 00		(3/5) x f_{ints_t}	—	—	kHz	
f_{loc_high}	Loss of external clock minimum frequency — RANGE = 01, 10, or 11		(16/5) x f_{ints_t}	—	—	kHz	
FLL							
f_{fll_ref}	FLL reference frequency range		31.25	—	39.0625	kHz	
f_{dco}	DCO output frequency range	Low range (DRS=00) 640 × f_{fll_ref}	20	20.97	25	MHz	3, 4
		Mid range (DRS=01) 1280 × f_{fll_ref}	40	41.94	50	MHz	
		Mid-high range (DRS=10) 1920 × f_{fll_ref}	60	62.91	75	MHz	
		High range (DRS=11) 2560 × f_{fll_ref}	80	83.89	100	MHz	
$f_{dco\_t\_DMX32}$	DCO output frequency	Low range (DRS=00) 732 × f_{fll_ref}	—	23.99	—	MHz	5, 6
		Mid range (DRS=01) 1464 × f_{fll_ref}	—	47.97	—	MHz	
		Mid-high range (DRS=10)	—	71.99	—	MHz	

Table continues on the next page...

3.3.2 IRC48M specifications

Table 17. IRC48M specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	—	3.6	V	
I_{DD48M}	Supply current	—	400	500	µA	
f_{irc48m}	Internal reference frequency	—	48	—	MHz	
$\Delta f_{irc48m\_ol\_hv}$	Open loop total deviation of IRC48M frequency at high voltage (VDD=1.89V-3.6V) over 0°C to 70°C	—				
	Regulator enable (USB_CLK_RECOVER_IRC_EN[REG_EN]=1)	—	± 0.2	± 0.5	$\%f_{irc48m}$	1
$\Delta f_{irc48m\_ol\_hv}$	Open loop total deviation of IRC48M frequency at high voltage (VDD=1.89V-3.6V) over full temperature					
	Regulator enable (USB_CLK_RECOVER_IRC_EN[REG_EN]=1)	—	± 0.4	± 1.0	$\%f_{irc48m}$	1
$\Delta f_{irc48m\_ol\_lv}$	Open loop total deviation of IRC48M frequency at low voltage (VDD=1.71V-1.89V) over full temperature					1
	Regulator disable (USB_CLK_RECOVER_IRC_EN[REG_EN]=0)	—	± 0.4	± 1.0	$\%f_{irc48m}$	
	Regulator enable (USB_CLK_RECOVER_IRC_EN[REG_EN]=1)	—	± 0.5	± 1.5		
Δf_{irc48m_cl}	Closed loop total deviation of IRC48M frequency over voltage and temperature	—	—	± 0.1	$\%f_{host}$	2
J_{cyc_irc48m}	Period Jitter (RMS)	—	35	150	ps	
$t_{irc48mst}$	Startup time	—	2	3	µs	3

1. The maximum value represents characterized results equivalent to the mean plus or minus three times the standard deviation (mean ± 3 sigma).
2. Closed loop operation of the IRC48M is only feasible for USB device operation; it is not usable for USB host operation. It is enabled by configuring for USB Device, selecting IRC48M as USB clock source, and enabling the clock recover function (USB_CLK_RECOVER_IRC_CTRL[CLOCK_RECOVER_EN]=1, USB_CLK_RECOVER_IRC_EN[IRC_EN]=1).
3. IRC48M startup time is defined as the time between clock enablement and clock availability for system use. Enable the clock by one of the following settings:
   - USB_CLK_RECOVER_IRC_EN[IRC_EN]=1 or
   - MCG operating in an external clocking mode and MCG_C7[OSCSEL]=10 or MCG_C5[PLLCLKEN0]=1, or
   - SIM_SOPT2[PLLFLLSEL]=11

3.3.3 Oscillator electrical specifications

2. Specification is valid for all FB_AD[31:0] and FB_TA.

Table 28. Flexbus full voltage range switching specifications

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	1.71	3.6	V	
	Frequency of operation	—	30	MHz	
FB1	Clock period	33.3	—	ns	
FB2	Address, data, and control output valid	—	21.5	ns	
FB3	Address, data, and control output hold	–1.0	—	ns	1
FB4	Data and FB_TA input setup	20.0	—	ns	
FB5	Data and FB_TA input hold	0.5	—	ns	2

1. Specification is valid for all FB_AD[31:0], FB_BE/BWE*n*, FB_CS*n*, FB_OE, FB_R/W,FB_TBST, FB_TSIZ[1:0], FB_ALE, and FB_TS.
2. Specification is valid for all FB_AD[31:0] and FB_TA.

3.8.1 USB electrical specifications

The USB electricals for the USB On-the-Go module conform to the standards documented by the Universal Serial Bus Implementers Forum. For the most up-to-date standards, visit **usb.org**.

NOTE

The MCGPLLCLK meets the USB jitter and signaling rate specifications for certification with the use of an external clock/crystal for both Device and Host modes.

The MCGFLLCLK does not meet the USB jitter or signaling rate specifications for certification.

The IRC48M meets the USB jitter and signaling rate specifications for certification in Device mode when the USB clock recovery mode is enabled. It does not meet the USB signaling rate specifications for certification in Host mode operation.

3.8.2 USB VREG electrical specifications

Table 38. USB VREG electrical specifications

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
VREGIN	Input supply voltage	2.7	—	5.5	V	
I_{DDon}	Quiescent current — Run mode, load current equal zero, input supply (VREGIN) > 3.6 V	—	125	186	µA	
I_{DDstby}	Quiescent current — Standby mode, load current equal zero	—	1.1	10	µA	
I_{DDoff}	Quiescent current — Shutdown mode • VREGIN = 5.0 V and temperature=25 °C • Across operating voltage and temperature	— —	650 —	— 4	nA µA	
$I_{LOADrun}$	Maximum load current — Run mode	—	—	120	mA	
$I_{LOADstby}$	Maximum load current — Standby mode	—	—	1	mA	
$V_{Reg33out}$	Regulator output voltage — Input supply (VREGIN) > 3.6 V • Run mode • Standby mode	 3 2.1	 3.3 2.8	 3.6 3.6	 V V	

Table continues on the next page...

Table 38. USB VREG electrical specifications (continued)

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
$V_{Reg33out}$	Regulator output voltage — Input supply (VREGIN) < 3.6 V, pass-through mode	2.1	—	3.6	V	2
C_{OUT}	External output capacitor	1.76	2.2	8.16	µF	
ESR	External output capacitor equivalent series resistance	1	—	100	mΩ	
I_{LIM}	Short circuit current	—	290	—	mA	

1. Typical values assume VREGIN = 5.0 V, Temp = 25 °C unless otherwise stated.
2. Operating in pass-through mode: regulator output voltage equal to the input voltage minus a drop proportional to I_{Load}.

3.8.3 DSPI switching specifications (limited voltage range)

The Deserial Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provide DSPI timing characteristics for classic SPI timing modes. Refer to the SPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

Table 39. Master mode DSPI timing (limited voltage range)

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	2.7	3.6	V	
	Frequency of operation	—	30	MHz	
DS1	DSPI_SCK output cycle time	2 x t_{BUS}	—	ns	
DS2	DSPI_SCK output high/low time	(t_{SCK}/2) – 2	(t_{SCK}/2) + 2	ns	
DS3	DSPI_PCS*n* valid to DSPI_SCK delay	(t_{BUS} x 2) – 2	—	ns	1
DS4	DSPI_SCK to DSPI_PCS*n* invalid delay	(t_{BUS} x 2) – 2	—	ns	2
DS5	DSPI_SCK to DSPI_SOUT valid	—	8.5	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	-2	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	16.2	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns	

1. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].
2. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].

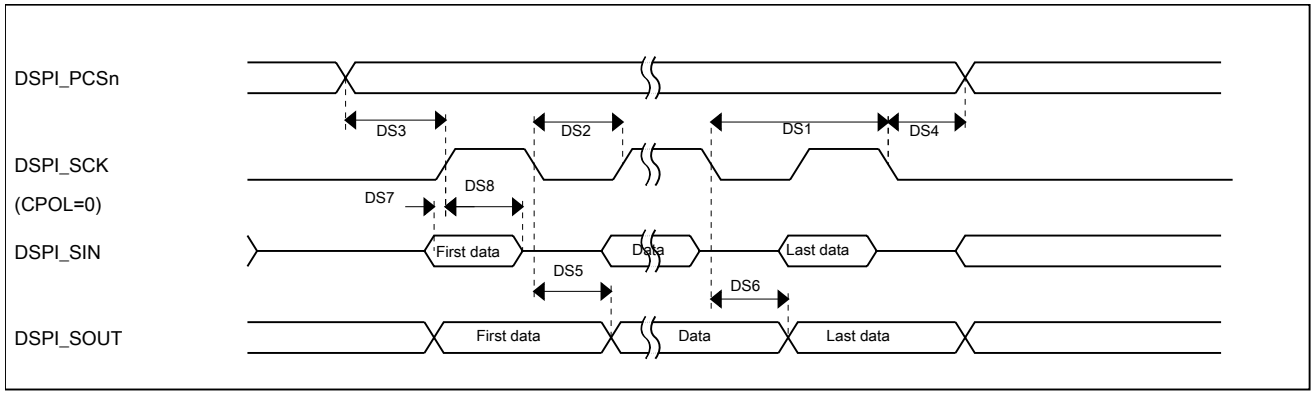

Figure 21. DSPI classic SPI timing — master mode

Table 40. Slave mode DSPI timing (limited voltage range)

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	2.7	3.6	V	
	Frequency of operation	—	15	MHz	1
DS9	DSPI_SCK input cycle time	4 x t_{BUS}	—	ns	
DS10	DSPI_SCK input high/low time	(t_{SCK}/2) – 2	(t_{SCK}/2) + 2	ns	
DS11	DSPI_SCK to DSPI_SOUT valid	—	21.4	ns	
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns	
DS13	DSPI_SIN to DSPI_SCK input setup	2.6	—	ns	
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns	
DS15	$\overline{\text{DSPI\_SS}}$ active to DSPI_SOUT driven	—	17	ns	
DS16	$\overline{\text{DSPI\_SS}}$ inactive to DSPI_SOUT not driven	—	17	ns	

1. The maximum operating frequency is measured with noncontinuous CS and SCK. When DSPI is configured with continuous CS and SCK, the SPI clock must not be greater than 1/6 of the bus clock. For example, when the bus clock is 60 MHz, the SPI clock must not be greater than 10 MHz.

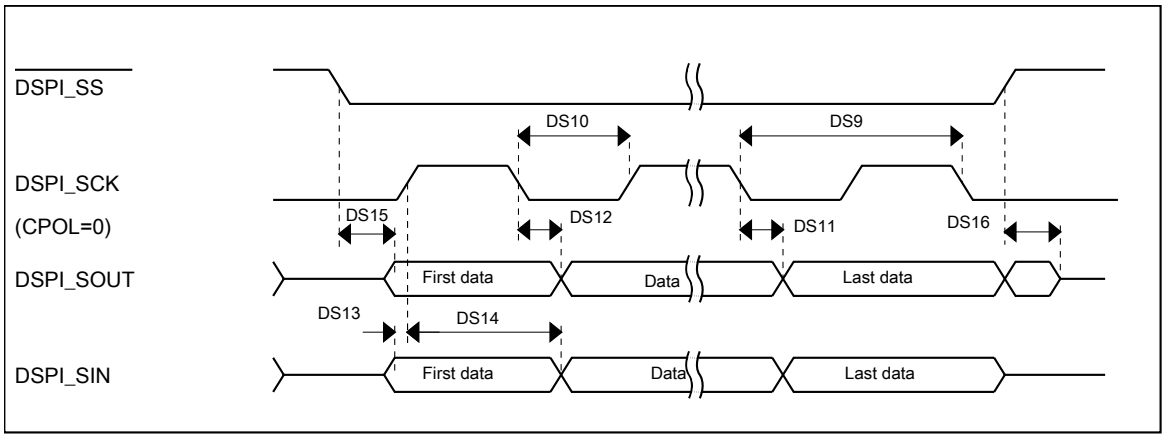

Figure 22. DSPI classic SPI timing — slave mode

Table 46. I2S/SAI slave mode timing in Normal Run, Wait and Stop modes (limited voltage range) (continued)

Num.	Characteristic	Min.	Max.	Unit
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	2	—	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid	—	20	ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	4.5	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK	2	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid[1]	—	25	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

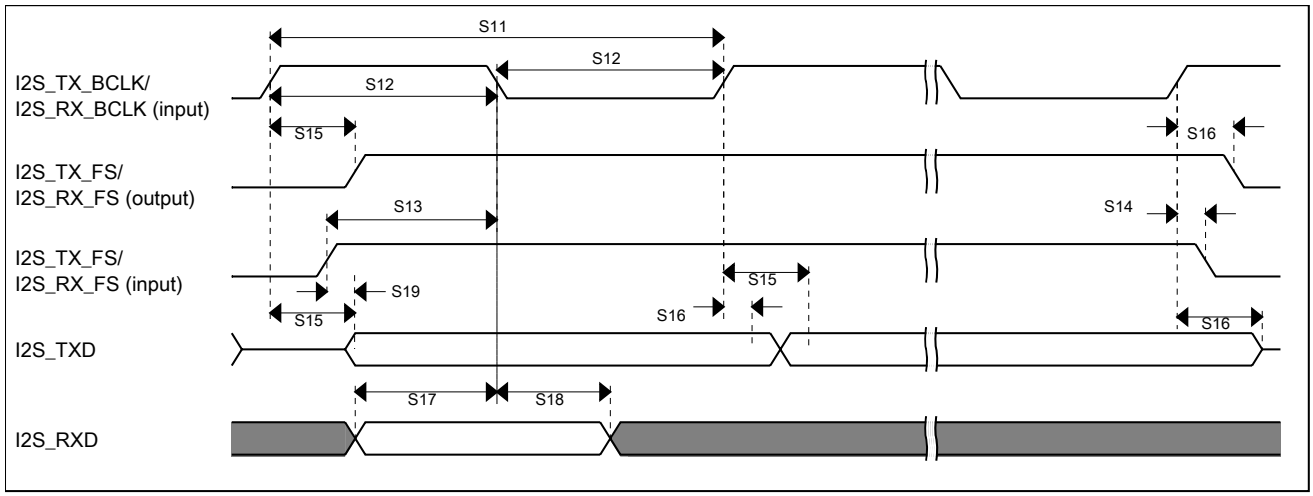

Figure 27. I2S/SAI timing — slave modes

3.8.7.2 Normal Run, Wait and Stop mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in Normal Run, Wait and Stop modes.

Table 47. I2S/SAI master mode timing in Normal Run, Wait and Stop modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	I2S_MCLK cycle time	40	—	ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period

Table continues on the next page...

64 MAP BGA	64 LQFP	88 QFN	100 LQFP	121 MAP BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EZPORT
—	—	—	14	H1	ADC0_ DP1	ADC0_ DP1	ADC0_ DP1								
—	—	—	15	H2	ADC0_ DM1	ADC0_ DM1	ADC0_ DM1								
—	—	14	16	J1	ADC1_ DP1/ ADC0_ DP2	ADC1_ DP1/ ADC0_ DP2	ADC1_ DP1/ ADC0_ DP2								
—	—	15	17	J2	ADC1_ DM1/ ADC0_ DM2	ADC1_ DM1/ ADC0_ DM2	ADC1_ DM1/ ADC0_ DM2								
G1	9	16	18	K1	ADC0_ DP0/ ADC1_ DP3	ADC0_ DP0/ ADC1_ DP3	ADC0_ DP0/ ADC1_ DP3								
F1	10	17	19	K2	ADC0_ DM0/ ADC1_ DM3	ADC0_ DM0/ ADC1_ DM3	ADC0_ DM0/ ADC1_ DM3								
G2	11	—	20	L1	ADC1_ DP0/ ADC0_ DP3	ADC1_ DP0/ ADC0_ DP3	ADC1_ DP0/ ADC0_ DP3								
F2	12	—	21	L2	ADC1_ DM0/ ADC0_ DM3	ADC1_ DM0/ ADC0_ DM3	ADC1_ DM0/ ADC0_ DM3								
F4	13	18	22	F5	VDDA	VDDA	VDDA								
G4	14	19	23	G5	VREFH	VREFH	VREFH								
G3	15	20	24	G6	VREFL	VREFL	VREFL								
F3	16	21	25	F6	VSSA	VSSA	VSSA								
—	—	—	—	J3	ADC1_ SE16/ ADC0_ SE22	ADC1_ SE16/ ADC0_ SE22	ADC1_ SE16/ ADC0_ SE22								
—	—	—	—	H3	ADC0_ SE16/ CMP1_ IN2/ ADC0_ SE21	ADC0_ SE16/ CMP1_ IN2/ ADC0_ SE21	ADC0_ SE16/ CMP1_ IN2/ ADC0_ SE21								
H1	17	22	26	L3	VREF_ OUT/ CMP1_ IN5/ CMP0_ IN5/	VREF_ OUT/ CMP1_ IN5/ CMP0_ IN5/	VREF_ OUT/ CMP1_ IN5/ CMP0_ IN5/								

64 MAP BGA	64 LQFP	88 QFN	100 LQFP	121 MAP BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EZPORT
—	—	33	40	E5	VDD	VDD	VDD								
—	—	34	41	G3	VSS	VSS	VSS								
—	—	—	—	J9	PTA10	DISABLED		PTA10		FTM2_ CH0			FTM2_ QD_PHA		
—	—	—	—	J4	PTA11	DISABLED		PTA11		FTM2_ CH1			FTM2_ QD_PHB		
H6	28	35	42	K8	PTA12	DISABLED		PTA12		FTM1_ CH0			I2S0_ TXD0	FTM1_ QD_PHA	
G6	29	36	43	L8	PTA13/ LLWU_P4	DISABLED		PTA13/ LLWU_P4		FTM1_ CH1			I2S0_TX_ FS	FTM1_ QD_PHB	
—	—	37	44	K9	PTA14	DISABLED		PTA14	SPI0_ PCS0	UART0_ TX			I2S0_RX_ BCLK		
—	—	38	45	L9	PTA15	DISABLED		PTA15	SPI0_SCK	UART0_ RX			I2S0_ RXD0		
—	—	39	46	J10	PTA16	DISABLED		PTA16	SPI0_ SOUT	UART0_ CTS_b			I2S0_RX_ FS		
—	—	40	47	H10	PTA17	ADC1_ SE17	ADC1_ SE17	PTA17	SPI0_SIN	UART0_ RTS_b			I2S0_ MCLK		
G7	30	41	48	L10	VDD	VDD	VDD								
H7	31	42	49	K10	VSS	VSS	VSS								
H8	32	43	50	L11	PTA18	EXTAL0	EXTAL0	PTA18		FTM0_ FLT2	FTM_ CLKIN0				
G8	33	44	51	K11	PTA19	XTAL0	XTAL0	PTA19		FTM1_ FLT0	FTM_ CLKIN1		LPTMR0_ ALT1		
F8	34	45	52	J11	RESET_b	RESET_b	RESET_b								
—	—	—	—	H11	PTA29	DISABLED		PTA29					FB_A24		
F7	35	46	53	G11	PTB0/ LLWU_P5	ADC0_ SE8/ ADC1_ SE8	ADC0_ SE8/ ADC1_ SE8	PTB0/ LLWU_P5	I2C0_SCL	FTM1_ CH0			FTM1_ QD_PHA		
F6	36	47	54	G10	PTB1	ADC0_ SE9/ ADC1_ SE9	ADC0_ SE9/ ADC1_ SE9	PTB1	I2C0_SDA	FTM1_ CH1			FTM1_ QD_PHB		
E7	37	48	55	G9	PTB2	ADC0_ SE12	ADC0_ SE12	PTB2	I2C0_SCL	UART0_ RTS_b			FTM0_ FLT3		
E8	38	49	56	G8	PTB3	ADC0_ SE13	ADC0_ SE13	PTB3	I2C0_SDA	UART0_ CTS_b			FTM0_ FLT0		
—	—	50	—	F11	PTB6	ADC1_ SE12	ADC1_ SE12	PTB6				FB_AD23			
—	—	51	—	E11	PTB7	ADC1_ SE13	ADC1_ SE13	PTB7				FB_AD22			
—	—	52	—	D11	PTB8	DISABLED		PTB8		LPUART0 _RTS_b		FB_AD21			

64 MAP BGA	64 LQFP	88 QFN	100 LQFP	121 MAP BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EZPORT
—	—	53	57	E10	PTB9	DISABLED		PTB9	SPI1_ PCS1	LPUART0 _CTS_b		FB_AD20			
—	—	54	58	D10	PTB10	ADC1_ SE14	ADC1_ SE14	PTB10	SPI1_ PCS0	LPUART0 _RX		FB_AD19	FTM0_ FLT1		
—	—	55	59	C10	PTB11	ADC1_ SE15	ADC1_ SE15	PTB11	SPI1_SCK	LPUART0 _TX		FB_AD18	FTM0_ FLT2		
—	—	—	60	—	VSS	VSS	VSS								
—	—	—	61	—	VDD	VDD	VDD								
E6	39	56	62	B10	PTB16	DISABLED		PTB16	SPI1_ SOUT	UART0_ RX	FTM_ CLKIN0	FB_AD17	EWM_IN		
D7	40	57	63	E9	PTB17	DISABLED		PTB17	SPI1_SIN	UART0_ TX	FTM_ CLKIN1	FB_AD16	EWM_ OUT_b		
D6	41	58	64	D9	PTB18	DISABLED		PTB18		FTM2_ CH0	I2S0_TX_ BCLK	FB_AD15	FTM2_ QD_PHA		
C7	42	59	65	C9	PTB19	DISABLED		PTB19		FTM2_ CH1	I2S0_TX_ FS	FB_OE_b	FTM2_ QD_PHB		
—	—	—	66	F10	PTB20	DISABLED		PTB20				FB_AD31	CMP0_ OUT		
—	—	—	67	F9	PTB21	DISABLED		PTB21				FB_AD30	CMP1_ OUT		
—	—	—	68	F8	PTB22	DISABLED		PTB22				FB_AD29			
—	—	—	69	E8	PTB23	DISABLED		PTB23		SPI0_ PCS5		FB_AD28			
D8	43	60	70	B9	PTC0	ADC0_ SE14	ADC0_ SE14	PTC0	SPI0_ PCS4	PDB0_ EXTRG	USB_ SOF_OUT	FB_AD14			
C6	44	61	71	D8	PTC1/ LLWU_P6	ADC0_ SE15	ADC0_ SE15	PTC1/ LLWU_P6	SPI0_ PCS3	UART1_ RTS_b	FTM0_ CH0	FB_AD13	I2S0_ TXD0	LPUART0 _RTS_b	
B7	45	62	72	C8	PTC2	ADC0_ SE4b/ CMP1_IN0	ADC0_ SE4b/ CMP1_IN0	PTC2	SPI0_ PCS2	UART1_ CTS_b	FTM0_ CH1	FB_AD12	I2S0_TX_ FS	LPUART0 _CTS_b	
C8	46	63	73	B8	PTC3/ LLWU_P7	CMP1_IN1	CMP1_IN1	PTC3/ LLWU_P7	SPI0_ PCS1	UART1_ RX	FTM0_ CH2	CLKOUT	I2S0_TX_ BCLK	LPUART0 _RX	
E3	47	64	74	—	VSS	VSS	VSS								
E4	48	65	75	—	VDD	VDD	VDD								
B8	49	66	76	A8	PTC4/ LLWU_P8	DISABLED		PTC4/ LLWU_P8	SPI0_ PCS0	UART1_ TX	FTM0_ CH3	FB_AD11	CMP1_ OUT	LPUART0 _TX	
A8	50	67	77	D7	PTC5/ LLWU_P9	DISABLED		PTC5/ LLWU_P9	SPI0_SCK	LPTMR0_ ALT2	I2S0_ RXD0	FB_AD10	CMP0_ OUT	FTM0_ CH2	
A7	51	68	78	C7	PTC6/ LLWU_ P10	CMP0_IN0	CMP0_IN0	PTC6/ LLWU_ P10	SPI0_ SOUT	PDB0_ EXTRG	I2S0_RX_ BCLK	FB_AD9	I2S0_ MCLK		
B6	52	69	79	B7	PTC7	CMP0_IN1	CMP0_IN1	PTC7	SPI0_SIN	USB_ SOF_OUT	I2S0_RX_ FS	FB_AD8			

64 MAP BGA	64 LQFP	88 QFN	100 LQFP	121 MAP BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EZPORT
A4	58	80	94	D3	PTD1	ADC0_ SE5b	ADC0_ SE5b	PTD1	SPI0_SCK	UART2_ CTS_b	FTM3_ CH1	FB_CS0_b	LPUART0 _CTS_b		
C2	59	81	95	C3	PTD2/ LLWU_ P13	DISABLED		PTD2/ LLWU_ P13	SPI0_ SOUT	UART2_ RX	FTM3_ CH2	FB_AD4	LPUART0 _RX	I2C0_SCL	
B3	60	82	96	B3	PTD3	DISABLED		PTD3	SPI0_SIN	UART2_ TX	FTM3_ CH3	FB_AD3	LPUART0 _TX	I2C0_SDA	
A3	61	83	97	A3	PTD4/ LLWU_ P14	DISABLED		PTD4/ LLWU_ P14	SPI0_ PCS1	UART0_ RTS_b	FTM0_ CH4	FB_AD2	EWM_IN	SPI1_ PCS0	
C1	62	84	98	A2	PTD5	ADC0_ SE6b	ADC0_ SE6b	PTD5	SPI0_ PCS2	UART0_ CTS_b	FTM0_ CH5	FB_AD1	EWM_ OUT_b	SPI1_SCK	
—	—	85	—	F7	VSS	VSS	VSS								
—	—	86	—	E7	VDD	VDD	VDD								
B2	63	87	99	B2	PTD6/ LLWU_ P15	ADC0_ SE7b	ADC0_ SE7b	PTD6/ LLWU_ P15	SPI0_ PCS3	UART0_ RX	FTM0_ CH6	FB_AD0	FTM0_ FLT0	SPI1_ SOUT	
A2	64	88	100	A1	PTD7	DISABLED		PTD7		UART0_ TX	FTM0_ CH7		FTM0_ FLT1	SPI1_SIN	
—	—	—	—	A10	PTD8	DISABLED		PTD8	I2C0_SCL			LPUART0 _RX	FB_A16		
—	—	—	—	A9	PTD9	DISABLED		PTD9	I2C0_SDA			LPUART0 _TX	FB_A17		
—	—	—	—	B1	PTD10	DISABLED		PTD10				LPUART0 _RTS_b	FB_A18		
—	—	—	—	C2	PTD11	DISABLED		PTD11				LPUART0 _CTS_b	FB_A19		
—	—	—	—	C1	PTD12	DISABLED		PTD12		FTM3_ FLT0			FB_A20		
—	—	—	—	D2	PTD13	DISABLED		PTD13					FB_A21		
—	—	—	—	D1	PTD14	DISABLED		PTD14					FB_A22		
—	—	—	—	E1	PTD15	DISABLED		PTD15					FB_A23		
—	—	—	—	A11	NC	NC	NC								
—	—	—	—	K3	NC	NC	NC								
—	—	—	—	H4	NC	NC	NC								
—	—	—	—	B11	NC	NC	NC								
—	—	—	—	C11	NC	NC	NC								

5.2 Recommended connection for unused analog and digital pins

The following table shows the recommended connections for analog interface pins if those analog interfaces are not used in the customer's application.

Table 51. Recommended connection for unused analog interfaces

Pin Type		Short recommendation	Detailed recommendation
Analog/non GPIO	PGAx/ADCx	Float	Analog input - Float
Analog/non GPIO	ADCx/CMPx	Float	Analog input - Float
Analog/non GPIO	VREF_OUT	Float	Analog output - Float
Analog/non GPIO	DACx_OUT	Float	Analog output - Float
Analog/non GPIO	RTC_WAKEUP_B	Float	Analog output - Float
Analog/non GPIO	XTAL32	Float	Analog output - Float
Analog/non GPIO	EXTAL32	Float	Analog input - Float
GPIO/Analog	PTA18/EXTAL0	Float	Analog input - Float
GPIO/Analog	PTA19/XTAL0	Float	Analog output - Float
GPIO/Analog	PTx/ADCx	Float	Float (default is analog input)
GPIO/Analog	PTx/CMPx	Float	Float (default is analog input)
GPIO/Digital	PTA0/JTAG_TCLK	Float	Float (default is JTAG with pulldown)
GPIO/Digital	PTA1/JTAG_TDI	Float	Float (default is JTAG with pullup)
GPIO/Digital	PTA2/JTAG_TDO	Float	Float (default is JTAG with pullup)
GPIO/Digital	PTA3/JTAG_TMS	Float	Float (default is JTAG with pullup)
GPIO/Digital	PTA4/NMI_b	10kΩ pullup or disable and float	Pull high or disable in PCR & FOPT and float
GPIO/Digital	PTx	Float	Float (default is disabled)
USB	USB0_DP	Float	Float
USB	USB0_DM	Float	Float
USB	VOUT33	Tie to input and ground through 10kΩ	Tie to input and ground through 10kΩ
USB	VREGIN	Tie to output and ground through 10kΩ	Tie to output and ground through 10kΩ
VBAT	VBAT	Float	Float
VDDA	VDDA	Always connect to VDD potential	Always connect to VDD potential
VREFH	VREFH	Always connect to VDD potential	Always connect to VDD potential
VREFL	VREFL	Always connect to VSS potential	Always connect to VSS potential
VSSA	VSSA	Always connect to VSS potential	Always connect to VSS potential

5.3 K22 Pinouts

The following figure shows the pinout diagram for the devices supported by this document. Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, see the previous section.

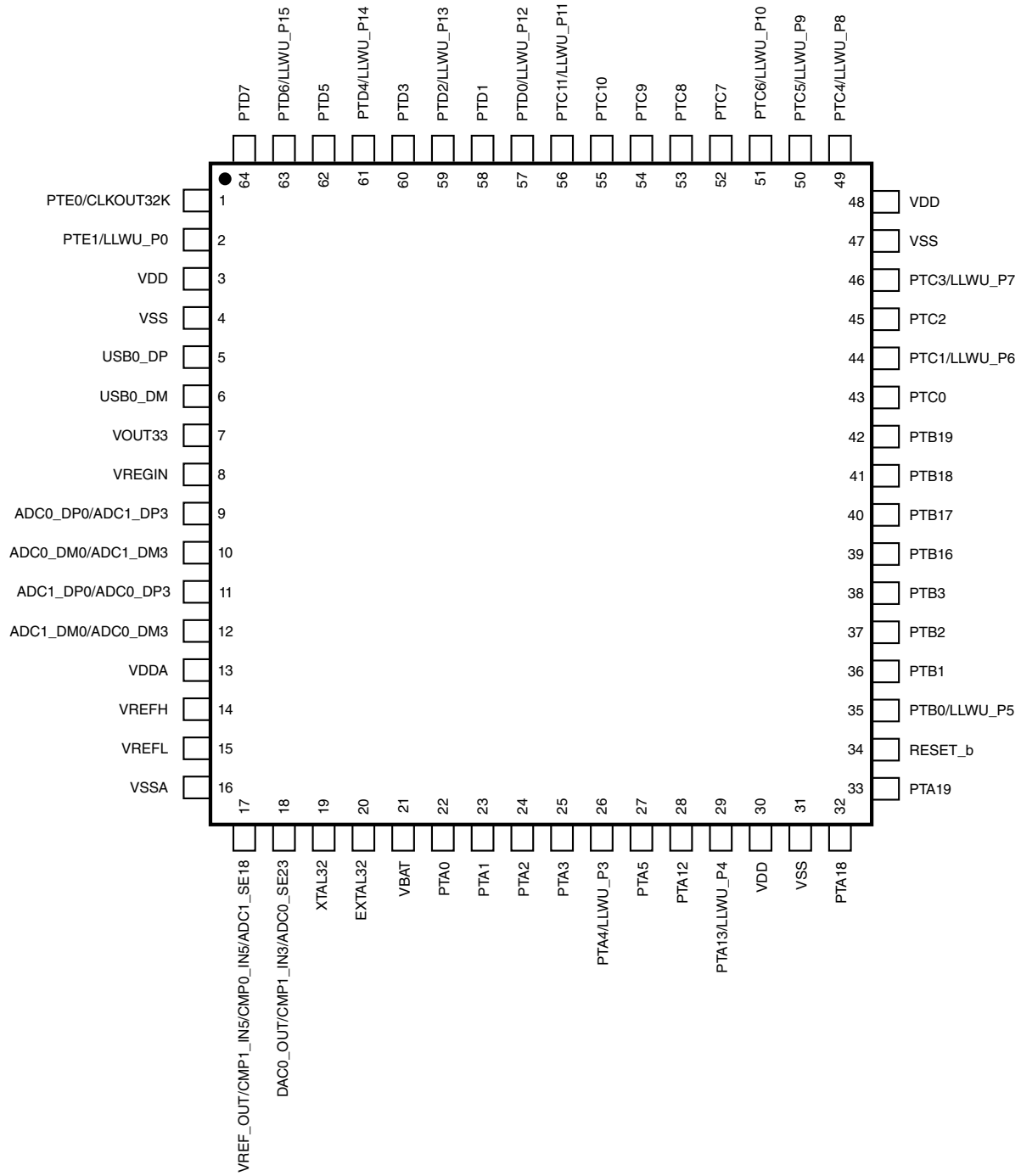

Figure 32. K22F 64 LQFP pinout diagram (top view)

6.4 Example

This is an example part number:

MK22FN512VDC12

6.5 121-pin XFBGA part marking

The 121-pin XFBGA package parts follow the part-marking scheme in the following table.

Table 52. 121-pin XFBGA part marking

MK Partnumber	MK Part Marking
MK22FN512VDC12	M22J9VDC

6.6 64-pin MAPBGA part marking

The 64-pin MAPBGA package parts follow the part-marking scheme in the following table.

Table 53. 64-pin MAPBGA part marking

MK Partnumber	MK Part Marking
MK22FN512VMP12	M22J9V

7 Terminology and guidelines

7.1 Definitions

Key terms are defined in the following table:

Term	Definition
Rating	A minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure: • *Operating ratings* apply during operation of the chip. • *Handling ratings* apply when the chip is not powered.

Table continues on the next page...

Term	Definition
	NOTE: The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.
Operating requirement	A specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip
Operating behavior	A specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions
Typical value	A specified value for a technical characteristic that: • Lies within the range of values specified by the operating behavior • Is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions **NOTE:** Typical values are provided as design guidelines and are neither tested nor guaranteed.

7.2 Examples

Operating rating:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	–0.3	1.2	V

Operating requirement:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	0.9	1.1	V

Operating behavior that includes a *typical value*:

Symbol	Description	Min.	Typ.	Max.	Unit
I_{WP}	Digital I/O weak pullup/pulldown current	10	70	130	µA

7.3 Typical-value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Table 54. Revision History (continued)

Rev. No.	Date	Substantial Changes
		• Added the following footnote on maximum Fast mode value for SCL Clock Frequency: "The maximum SCL Clock Frequency in Fast mode with maximum bus loading can only be achieved when using the High drive pins across the full voltage range and when using the Normal drive pins and VDD ≥ 2.7 V." • Updated minimum Fast mode value for LOW period of the SCL clock to 1.25 µ • Added "I^2C 1 Mbps timing" table • Removed Section 6, "Ordering parts." • Specified that the figure, "K22F 64 LQFP Pinout Diagram" is a top view • Specified that the figure, "K22F 64 MAPBGA Pinout Diagram" is a transparent top view • Specified that the figure, "K22F 100 LQFP Pinout Diagram" is a top view • Corrected part marking shown in "64-pin MAPBGA part marking" table
4	7/2014	• In "Power consumption operating behaviors table": • Updated existing typical power measurements • Added new typical power measurements for the following: • IDD_HSRUN (High Speed Run mode current executing CoreMark code) • IDD_RUNCO (Run mode current in Compute operation, executing CoreMark code) • IDD_RUN (Run mode current in Compute operation, executing while(1) loop) • IDD_VLPR (Very Low Power mode current executing CoreMark code) • IDD_VLPR (Very Low Power Run mode current in Compute operation, executing while(1) loop) • In "Thermal attributes" table, added values for 64 MAPBGA package
3	5/2014	• In "Voltage and current operating ratings" table, updated maximum digital supply current • Updated "Voltage and current operating behaviors" table • Updated "Power mode transition operating behaviors" table • Updated "Power consumption operating behaviors" table • Updated "EMC radiated emissions operating behaviors for 64 LQFP package" table • Updated "Thermal attributes" table • Updated "MCG specifications" table • Updated "IRC48M specifications" table • Updated "16-bit ADC operating conditions" table • Updated "Voltage reference electrical specifications" section • Added "64-pin MAPBGA part marking" table
2	3/2014	Initial public release