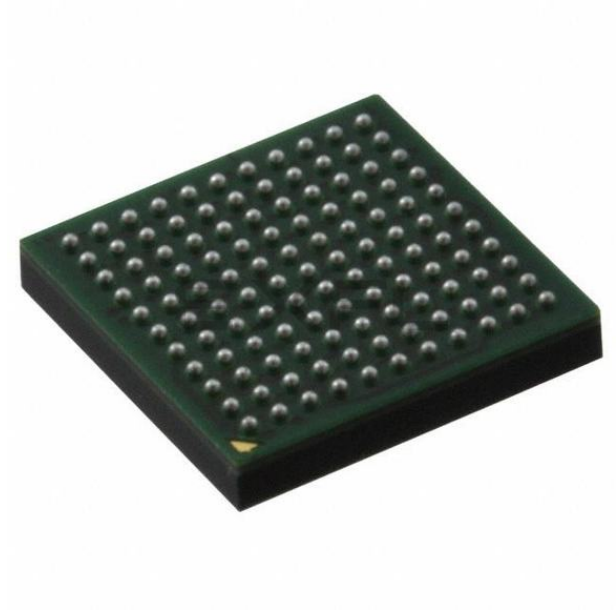

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB, USB OTG
Peripherals	DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	81
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 38x16b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	121-XFBGA
Supplier Device Package	121-XFBGA (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mk22fn512vdc12r

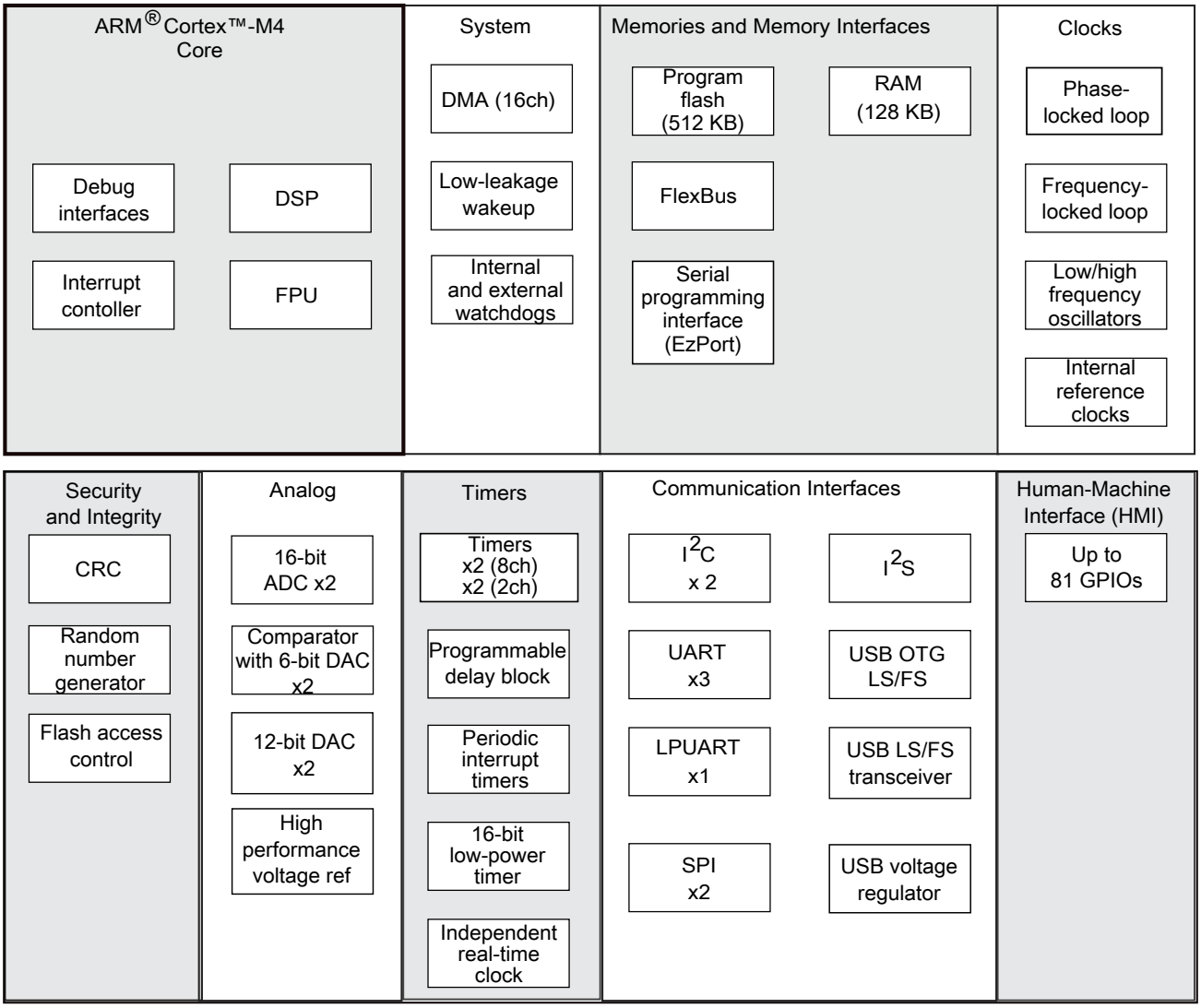

Figure 1. Functional block diagram

Table 4. Voltage and current operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{OL}	Output low voltage — Normal drive pad except RESET_B					
	2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 5 mA	—	—	0.5	V	1
	1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 2.5 mA	—	—	0.5	V	
V_{OL}	Output low voltage — High drive pad except RESET_B					
	2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 20 mA	—	—	0.5	V	1
	1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 10 mA	—	—	0.5	V	
V_{OL}	Output low voltage — RESET_B					
	2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 3 mA	—	—	0.5	V	
	1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 1.5 mA	—	—	0.5	V	
I_{OLT}	Output low current total for all ports	—	—	100	mA	
I_{IN}	Input leakage current (per pin) for full temperature range					
	All pins other than high drive port pins	—	0.002	0.5	µA	1, 2
	High drive port pins	—	0.004	0.5	µA	
I_{IN}	Input leakage current (total all pins) for full temperature range	—	—	1.0	µA	2
R_{PU}	Internal pullup resistors	20	—	50	kΩ	3
R_{PD}	Internal pulldown resistors	20	—	50	kΩ	4

1. PTB0, PTB1, PTC3, PTC4, PTD4, PTD5, PTD6, and PTD7 I/O have both high drive and normal drive capability selected by the associated PTx_PCRn[DSE] control bit. All other GPIOs are normal drive only.
2. Measured at VDD=3.6V
3. Measured at V_{DD} supply voltage = V_{DD} min and Vinput = V_{SS}
4. Measured at V_{DD} supply voltage = V_{DD} min and Vinput = V_{DD}

2.2.4 Power mode transition operating behaviors

All specifications except t_{POR}, and VLLSx→RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 80 MHz
- Bus clock = 40 MHz
- FlexBus clock = 20 MHz
- Flash clock = 20 MHz
- MCG mode: FEI

Table 5. Power mode transition operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{POR}	After a POR event, amount of time from the point V_{DD} reaches 1.71 V to execution of the first instruction across the operating temperature range of the chip.	—	—	300	µs	1
	• VLLS0 → RUN	—	—	140	µs	
	• VLLS1 → RUN	—	—	140	µs	
	• VLLS2 → RUN	—	—	80	µs	
	• VLLS3 → RUN	—	—	80	µs	
	• LLS2 → RUN	—	—	6	µs	
	• LLS3 → RUN	—	—	6	µs	
	• VLPS → RUN	—	—	5.7	µs	
	• STOP → RUN	—	—	5.7	µs	

1. Normal boot (FTFA_OPT[LPBOOT]=1)

2.2.5 Power consumption operating behaviors

The current parameters in the table below are derived from code executing a while(1) loop from flash, unless otherwise noted.

The IDD typical values represent the statistical mean at 25°C, and the IDD maximum values for RUN, WAIT, VLPR, and VLPW represent data collected at 125°C junction temperature unless otherwise noted. The maximum values represent characterized results equivalent to the mean plus three times the standard deviation (mean + 3 sigma).

Table 6. Power consumption operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA}	Analog supply current	—	—	See note	mA	1
I_{DD_HSRUN}	High Speed Run mode current - all peripheral clocks disabled, CoreMark benchmark code executing from flash					

Table continues on the next page...

Table 7. Low power mode peripheral adders—typical value (continued)

Symbol	Description	Temperature (°C)						Unit
		-40	25	50	70	85	105	
	and EREFSTEN] bits. Measured by entering all modes with the crystal enabled.							
	VLLS1	440	490	540	560	570	580	nA
	VLLS3	440	490	540	560	570	580	
	LLS	490	490	540	560	570	680	
	VLPS	510	560	560	560	610	680	
	STOP	510	560	560	560	610	680	
I_{48MIRC}	48 Mhz internal reference clock	350	350	350	350	350	350	µA
I_{CMP}	CMP peripheral adder measured by placing the device in VLLS1 mode with CMP enabled using the 6-bit DAC and a single external input for compare. Includes 6-bit DAC power consumption.	22	22	22	22	22	22	µA
I_{RTC}	RTC peripheral adder measured by placing the device in VLLS1 mode with external 32 kHz crystal enabled by means of the RTC_CR[OSCE] bit and the RTC ALARM set for 1 minute. Includes ERCLK32K (32 kHz external crystal) power consumption.	432	357	388	475	532	810	nA
I_{UART}	UART peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source waiting for RX data at 115200 baud rate. Includes selected clock source power consumption.							
	MCGIRCLK (4 MHz internal reference clock)	66	66	66	66	66	66	µA
	>OSCERCLK (4 MHz external crystal)	214	237	246	254	260	268	
I_{BG}	Bandgap adder when BGEN bit is set and device is placed in VLPx, LLS, or VLLSx mode.	45	45	45	45	45	45	µA
I_{ADC}	ADC peripheral adder combining the measured values at V_{DD} and V_{DDA} by placing the device in STOP or VLPS mode. ADC is configured for low power mode using the internal clock and continuous conversions.	42	42	42	42	42	42	µA

2.2.5.1 Diagram: Typical IDD_RUN operating behavior

The following data was measured under these conditions:

- MCG in FBE mode for 50 MHz and lower frequencies. MCG in FEE mode at frequencies between 50 MHz and 100MHz. MCG in PEE mode at frequencies greater than 100 MHz.
- USB regulator disabled
- No GPIOs toggled
- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFA

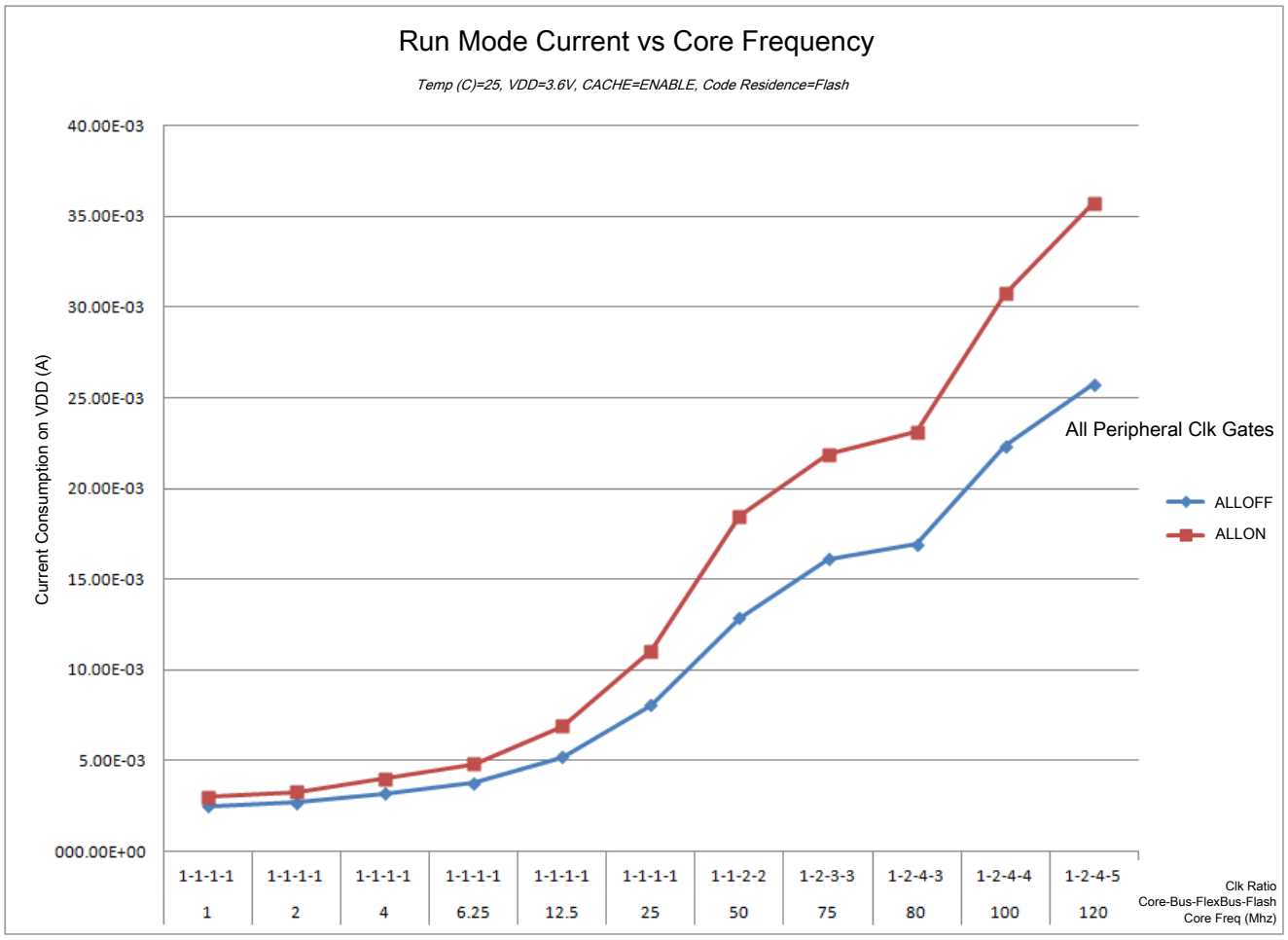

Figure 3. Run mode supply current vs. core frequency

3. The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.
4. IEC Level Maximums: M ≤ 18dBmV, L ≤ 24dBmV, K ≤ 30dBmV, I ≤ 36dBmV, H ≤ 42dBmV .

2.2.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

- Go to nxp.com
- Perform a keyword search for "EMC design."

2.2.8 Capacitance attributes

Table 9. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C_{IN_A}	Input capacitance: analog pins	—	7	pF
C_{IN_D}	Input capacitance: digital pins	—	7	pF

2.3 Switching specifications

2.3.1 Device clock specifications

Table 10. Device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes
High Speed run mode					
f_{SYS}	System and core clock	—	120	MHz	
f_{BUS}	Bus clock	—	60	MHz	
Normal run mode (and High Speed run mode unless otherwise specified above)					
f_{SYS}	System and core clock	—	80	MHz	
f_{SYS_USB}	System and core clock when Full Speed USB in operation	20	—	MHz	
f_{BUS}	Bus clock	—	50	MHz	
FB_CLK	FlexBus clock	—	30	MHz	
f_{FLASH}	Flash clock	—	26.67	MHz	
f_{LPTMR}	LPTMR clock	—	25	MHz	
VLPR mode[1]					

Table continues on the next page...

2. The greater of synchronous and asynchronous timing must be met.
3. These pins have a passive filter enabled on the inputs. This is the shortest pulse width that is guaranteed to be recognized.
4. These pins do not have a passive filter on the inputs. This is the shortest pulse width that is guaranteed to be recognized.
5. 25 pF load

2.4 Thermal specifications

2.4.1 Thermal operating requirements

Table 12. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
T_J	Die junction temperature	–40	125	°C	
T_A	Ambient temperature	–40	105	°C	1

1. Maximum T_A can be exceeded only if the user ensures that T_J does not exceed maximum T_J. The simplest method to determine T_J is: $T_J = T_A + R_{\Theta JA} \times$ chip power dissipation.

2.4.2 Thermal attributes

Board type	Symbol	Description	121 XFBGA	100 LQFP	64 LQFP	64 MAPBGA	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	44.4	61	67	95.7	°C/W	1
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	27.0	48	48	48.8	°C/W	2
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	37.2	51	55	74.4	°C/W	3
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	23.7	42	42	44.0	°C/W	3
—	$R_{\theta JB}$	Thermal resistance, junction to board	23.5	34	31	30.3	°C/W	4
—	$R_{\theta JC}$	Thermal resistance, junction to case	17.4	16	16	28.0	°C/W	5
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside	0.2	3	3	1.0	°C/W	6

Board type	Symbol	Description	88 QFN	Unit	Notes
		parameter, junction to package top outside center (natural convection)			

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with natural convection for horizontally oriented board. Board meets JESD51-9 specification for 1s or 2s2p board, respectively.
3. Per JEDEC JESD51-6 with forced convection for horizontally oriented board. Board meets JESD51-9 specification for 1s or 2s2p board, respectively.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the solder pad on the bottom of the package. Interface resistance is ignored.
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

3 Peripheral operating requirements and behaviors

3.1 Core modules

3.1.1 SWD electricals

Table 13. SWD full voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	SWD_CLK frequency of operation • Serial wire debug	 0	 33	 MHz
S2	SWD_CLK cycle period	1/S1	—	ns
S3	SWD_CLK clock pulse width • Serial wire debug	 15	 —	 ns
S4	SWD_CLK rise and fall times	—	3	ns
S9	SWD_DIO input data setup time to SWD_CLK rise	8	—	ns
S10	SWD_DIO input data hold time after SWD_CLK rise	1.4	—	ns
S11	SWD_CLK high to SWD_DIO data valid	—	25	ns
S12	SWD_CLK high to SWD_DIO high-Z	5	—	ns

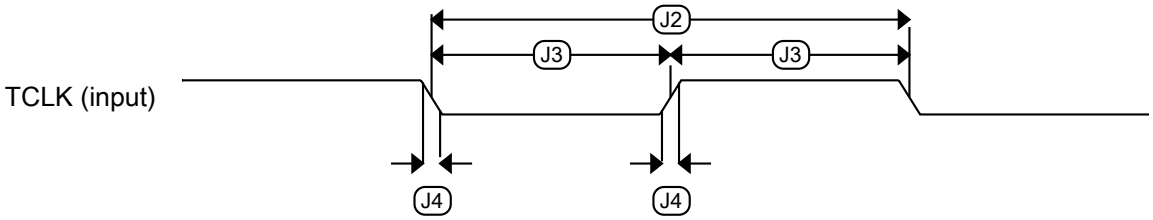

Figure 7. Test clock input timing

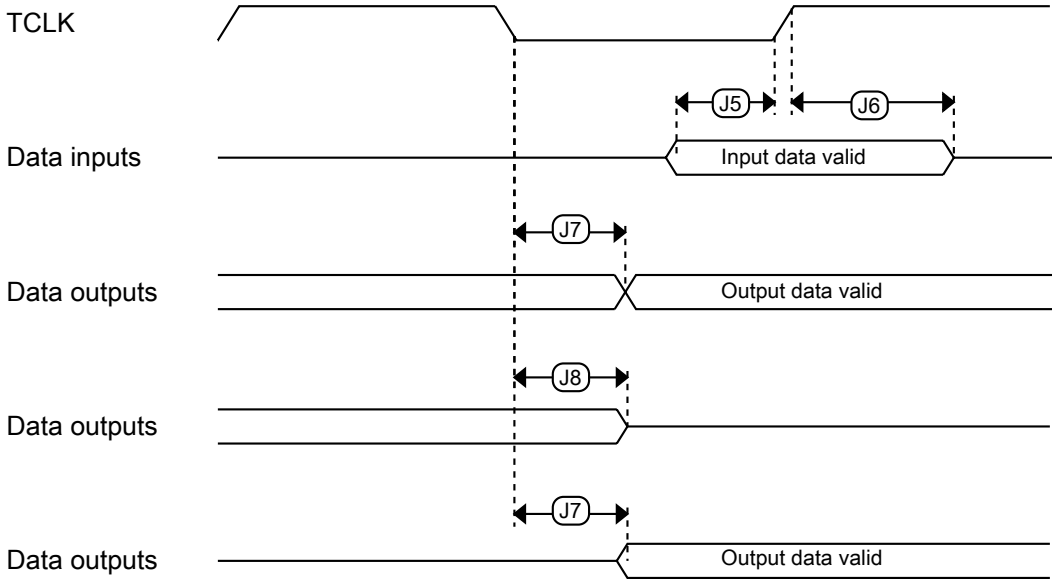

Figure 8. Boundary scan (JTAG) timing

2. Specification is valid for all FB_AD[31:0] and FB_TA.

Table 28. Flexbus full voltage range switching specifications

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	1.71	3.6	V	
	Frequency of operation	—	30	MHz	
FB1	Clock period	33.3	—	ns	
FB2	Address, data, and control output valid	—	21.5	ns	
FB3	Address, data, and control output hold	–1.0	—	ns	1
FB4	Data and FB_TA input setup	20.0	—	ns	
FB5	Data and FB_TA input hold	0.5	—	ns	2

1. Specification is valid for all FB_AD[31:0], FB_BE/BWE*n*, FB_CS*n*, FB_OE, FB_R/W,FB_TBST, FB_TSIZ[1:0], FB_ALE, and FB_TS.
2. Specification is valid for all FB_AD[31:0] and FB_TA.

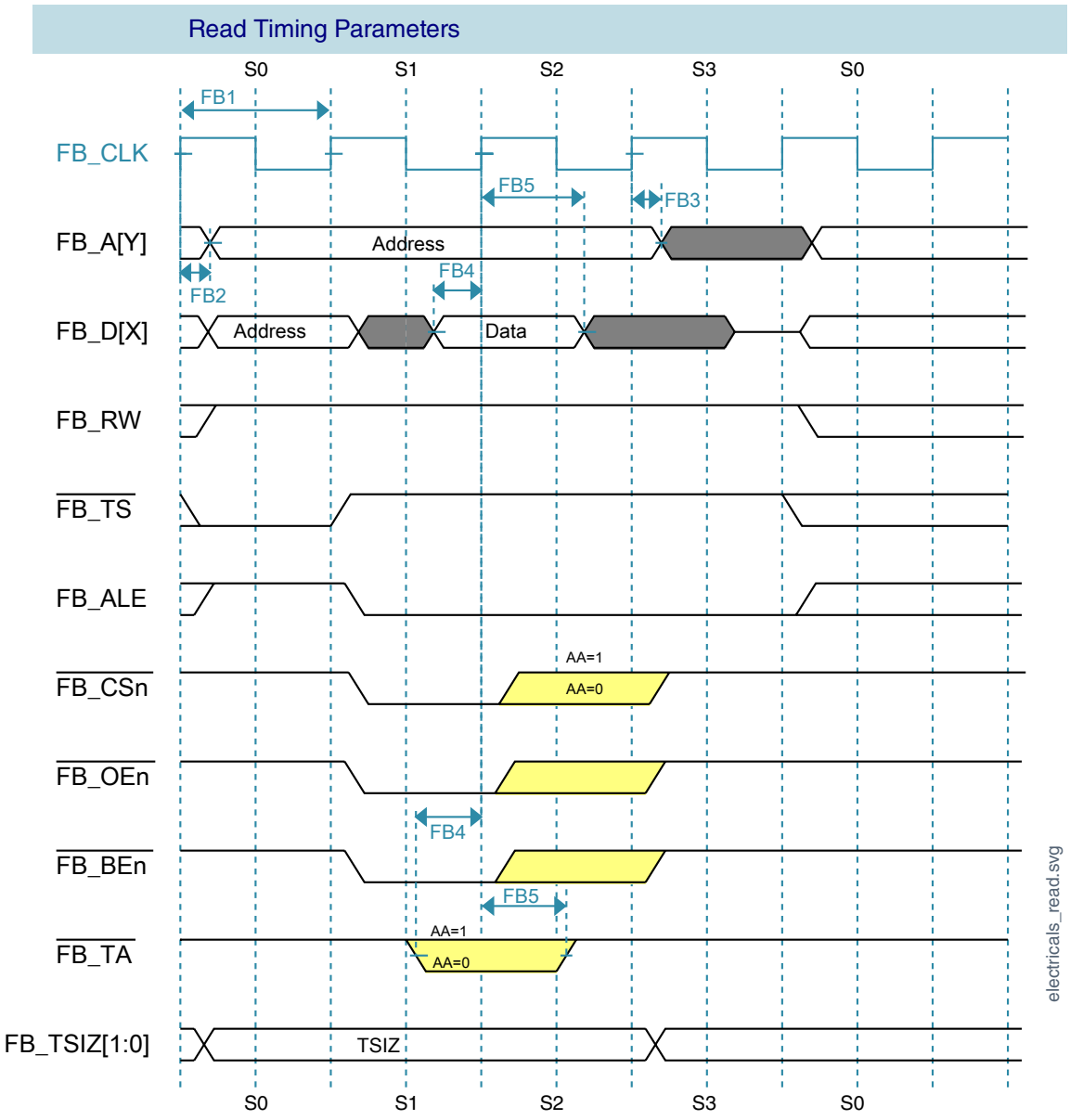

Figure 12. FlexBus read timing diagram

Table 30. 16-bit ADC characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA}) (continued)

Symbol	Description	Conditions[1]	Min.	Typ.[2]	Max.	Unit	Notes
		• Avg = 32					
E_{IL}	Input leakage error		$I_{In} \times R_{AS}$			mV	I_{In} = leakage current (refer to the MCU's voltage and current operating ratings)
	Temp sensor slope	Across the full temperature range of the device	1.55	1.62	1.69	mV/°C	8
V_{TEMP25}	Temp sensor voltage	25 °C	706	716	726	mV	8

1. All accuracy numbers assume the ADC is calibrated with V_{REFH} = V_{DDA}
2. Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 2.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
3. The ADC supply current depends on the ADC conversion clock speed, conversion rate and ADC_CFG1[ADLPC] (low power). For lowest power operation, ADC_CFG1[ADLPC] must be set, the ADC_CFG2[ADHSC] bit must be clear with 1 MHz ADC conversion clock speed.
4. 1 LSB = (V_{REFH} - V_{REFL})/2^N
5. ADC conversion clock < 16 MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
6. Input data is 100 Hz sine wave. ADC conversion clock < 12 MHz.
7. Input data is 1 kHz sine wave. ADC conversion clock < 12 MHz.
8. ADC conversion clock < 3 MHz

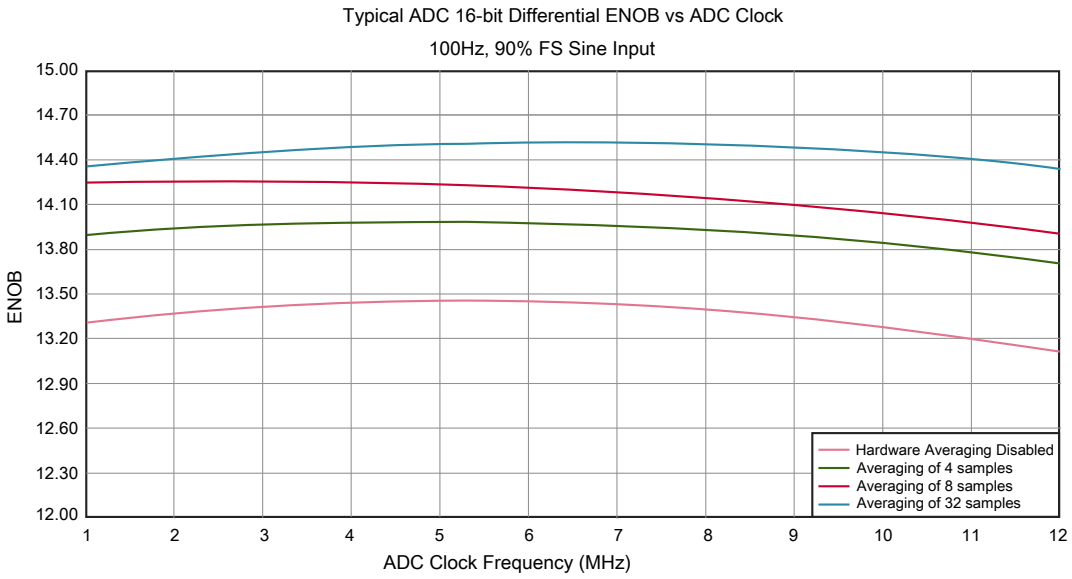

Figure 15. Typical ENOB vs. ADC_CLK for 16-bit differential mode

3.6.3.2 12-bit DAC operating behaviors

Table 33. 12-bit DAC operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA_DACLP}	Supply current — low-power mode	—	—	330	µA	
I_{DDA_DACHP}	Supply current — high-speed mode	—	—	1200	µA	
t_{DACLP}	Full-scale settling time (0x080 to 0xF7F) — low-power mode	—	100	200	µs	1
t_{DACHP}	Full-scale settling time (0x080 to 0xF7F) — high-power mode	—	15	30	µs	1
$t_{CCDACLP}$	Code-to-code settling time (0xBF8 to 0xC08) — low-power mode and high-speed mode	—	0.7	1	µs	1
$V_{dacoutl}$	DAC output voltage range low — high-speed mode, no load, DAC set to 0x000	—	—	100	mV	
$V_{dacouth}$	DAC output voltage range high — high-speed mode, no load, DAC set to 0xFFF	V_{DACR} −100	—	V_{DACR}	mV	
INL	Integral non-linearity error — high speed mode	—	—	±8	LSB	2
DNL	Differential non-linearity error — V_{DACR} > 2 V	—	—	±1	LSB	3
DNL	Differential non-linearity error — V_{DACR} = VREF_OUT	—	—	±1	LSB	4
V_{OFFSET}	Offset error	—	±0.4	±0.8	%FSR	5
E_G	Gain error	—	±0.1	±0.6	%FSR	5
PSRR	Power supply rejection ratio, V_{DDA} ≥ 2.4 V	60	—	90	dB	
T_{CO}	Temperature coefficient offset voltage	—	3.7	—	µV/C	6
T_{GE}	Temperature coefficient gain error	—	0.000421	—	%FSR/C	
Rop	Output resistance (load = 3 kΩ)	—	—	250	Ω	
SR	Slew rate -80h→ F7Fh→ 80h • High power (SP_{HP}) • Low power (SP_{LP})	 1.2 0.05	 1.7 0.12	 — —	V/µs	
BW	3dB bandwidth • High power (SP_{HP}) • Low power (SP_{LP})	 550 40	 — —	 — —	kHz	

1. Settling within ±1 LSB
2. The INL is measured for 0 + 100 mV to V_{DACR} −100 mV
3. The DNL is measured for 0 + 100 mV to V_{DACR} −100 mV
4. The DNL is measured for 0 + 100 mV to V_{DACR} −100 mV with V_{DDA} > 2.4 V
5. Calculated by a best fit curve from V_{SS} + 100 mV to V_{DACR} − 100 mV
6. V_{DDA} = 3.0 V, reference select set for V_{DDA} (DACx_CO:DACRFS = 1), high power mode (DACx_C0:LPEN = 0), DAC set to 0x800, temperature range is across the full range of the device

Table 42. Slave mode DSPI timing (full voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
	Frequency of operation	—	7.5	MHz
DS9	DSPI_SCK input cycle time	8 x t_{BUS}	—	ns
DS10	DSPI_SCK input high/low time	(t_{SCK}/2) - 4	($t_{SCK/2}$) + 4	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	29.5	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	3.2	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns
DS15	$\overline{\text{DSPI\_SS}}$ active to DSPI_SOUT driven	—	25	ns
DS16	$\overline{\text{DSPI\_SS}}$ inactive to DSPI_SOUT not driven	—	25	ns

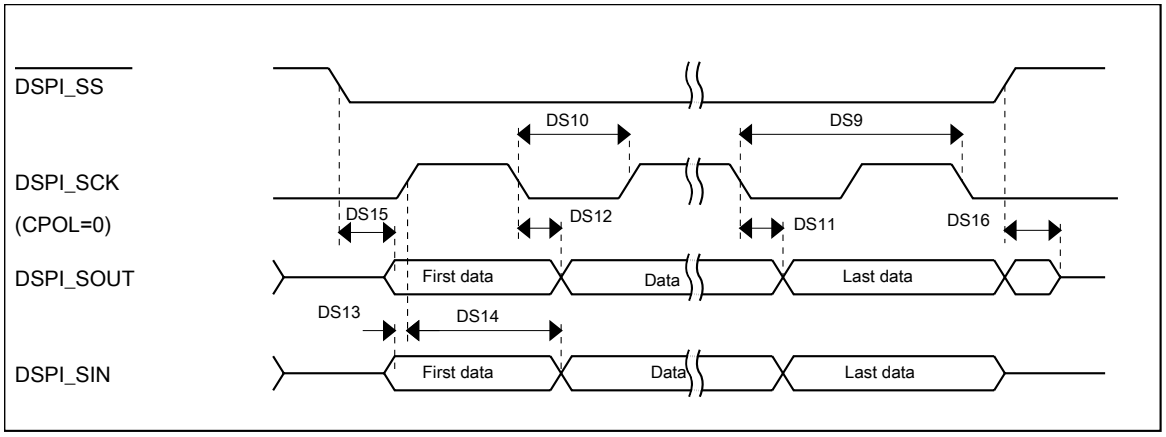

Figure 24. DSPI classic SPI timing — slave mode

3.8.5 Inter-Integrated Circuit Interface (I^2C) timing

Table 43. I^2C timing

Characteristic	Symbol	Standard Mode		Fast Mode		Unit
		Minimum	Maximum	Minimum	Maximum	
SCL Clock Frequency	f_{SCL}	0	100	0	400[1]	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	t_{HD}; STA	4	—	0.6	—	µs
LOW period of the SCL clock	t_{LOW}	4.7	—	1.25	—	µs
HIGH period of the SCL clock	t_{HIGH}	4	—	0.6	—	µs
Set-up time for a repeated START condition	t_{SU}; STA	4.7	—	0.6	—	µs

Table continues on the next page...

Table 48. I2S/SAI slave mode timing in Normal Run, Wait and Stop modes (full voltage range) (continued)

Num.	Characteristic	Min.	Max.	Unit
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	2	—	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid	—	28.5	ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	5.8	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK	2	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid[1]	—	26.3	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

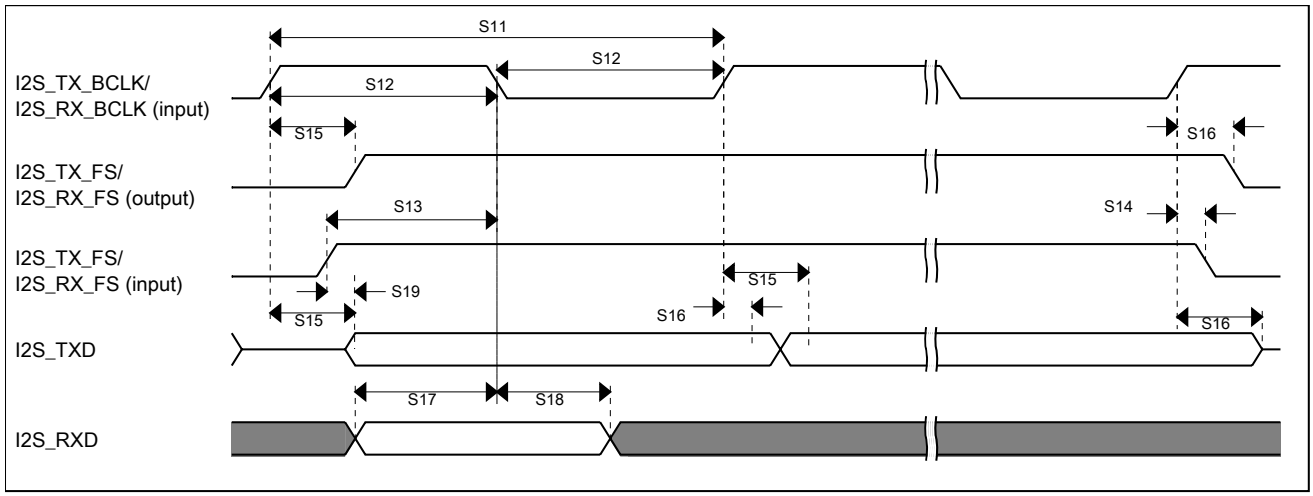

Figure 29. I2S/SAI timing — slave modes

3.8.7.3 VLPR, VLPW, and VLPS mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in VLPR, VLPW, and VLPS modes.

Table 49. I2S/SAI master mode timing in VLPR, VLPW, and VLPS modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	I2S_MCLK cycle time	62.5	—	ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	250	—	ns

Table continues on the next page...

Table 50. I2S/SAI slave mode timing in VLPR, VLPW, and VLPS modes (full voltage range) (continued)

Num.	Characteristic	Min.	Max.	Unit
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	30	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK	4	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid[1]	—	72	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

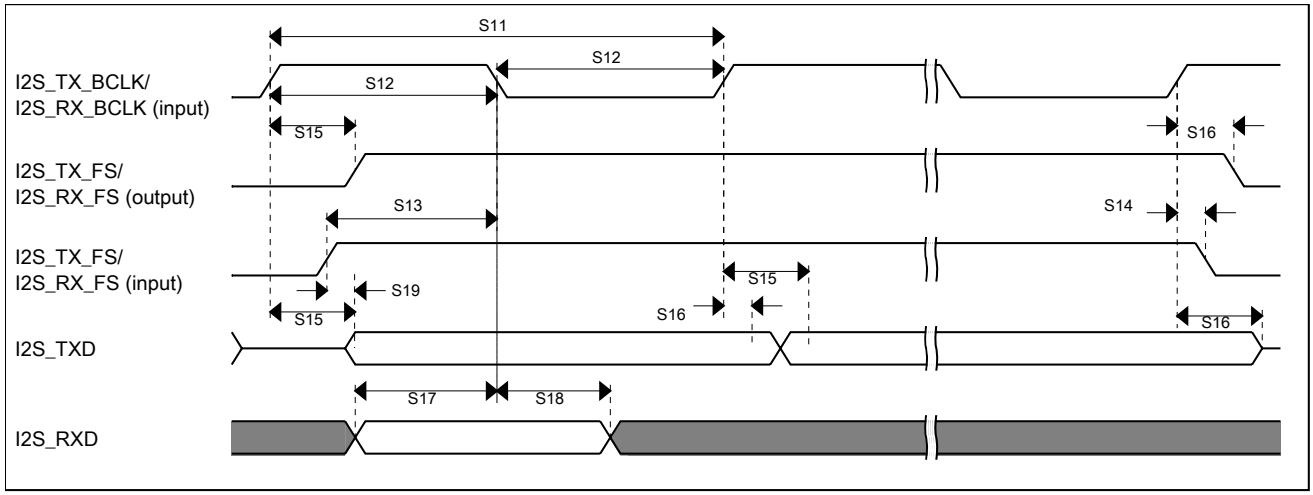

Figure 31. I2S/SAI timing — slave modes

4 Dimensions

4.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to nxp.com and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
64-pin LQFP	98ASS23234W
64-pin MAPBGA	98ASA00420D
88-pin QFN	98ASA00935D

Table continues on the next page...

64 MAP BGA	64 LQFP	88 QFN	100 LQFP	121 MAP BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EZPORT
—	—	—	14	H1	ADC0_ DP1	ADC0_ DP1	ADC0_ DP1								
—	—	—	15	H2	ADC0_ DM1	ADC0_ DM1	ADC0_ DM1								
—	—	14	16	J1	ADC1_ DP1/ ADC0_ DP2	ADC1_ DP1/ ADC0_ DP2	ADC1_ DP1/ ADC0_ DP2								
—	—	15	17	J2	ADC1_ DM1/ ADC0_ DM2	ADC1_ DM1/ ADC0_ DM2	ADC1_ DM1/ ADC0_ DM2								
G1	9	16	18	K1	ADC0_ DP0/ ADC1_ DP3	ADC0_ DP0/ ADC1_ DP3	ADC0_ DP0/ ADC1_ DP3								
F1	10	17	19	K2	ADC0_ DM0/ ADC1_ DM3	ADC0_ DM0/ ADC1_ DM3	ADC0_ DM0/ ADC1_ DM3								
G2	11	—	20	L1	ADC1_ DP0/ ADC0_ DP3	ADC1_ DP0/ ADC0_ DP3	ADC1_ DP0/ ADC0_ DP3								
F2	12	—	21	L2	ADC1_ DM0/ ADC0_ DM3	ADC1_ DM0/ ADC0_ DM3	ADC1_ DM0/ ADC0_ DM3								
F4	13	18	22	F5	VDDA	VDDA	VDDA								
G4	14	19	23	G5	VREFH	VREFH	VREFH								
G3	15	20	24	G6	VREFL	VREFL	VREFL								
F3	16	21	25	F6	VSSA	VSSA	VSSA								
—	—	—	—	J3	ADC1_ SE16/ ADC0_ SE22	ADC1_ SE16/ ADC0_ SE22	ADC1_ SE16/ ADC0_ SE22								
—	—	—	—	H3	ADC0_ SE16/ CMP1_ IN2/ ADC0_ SE21	ADC0_ SE16/ CMP1_ IN2/ ADC0_ SE21	ADC0_ SE16/ CMP1_ IN2/ ADC0_ SE21								
H1	17	22	26	L3	VREF_ OUT/ CMP1_ IN5/ CMP0_ IN5/	VREF_ OUT/ CMP1_ IN5/ CMP0_ IN5/	VREF_ OUT/ CMP1_ IN5/ CMP0_ IN5/								

64 MAP BGA	64 LQFP	88 QFN	100 LQFP	121 MAP BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EZPORT
—	—	33	40	E5	VDD	VDD	VDD								
—	—	34	41	G3	VSS	VSS	VSS								
—	—	—	—	J9	PTA10	DISABLED		PTA10		FTM2_ CH0			FTM2_ QD_PHA		
—	—	—	—	J4	PTA11	DISABLED		PTA11		FTM2_ CH1			FTM2_ QD_PHB		
H6	28	35	42	K8	PTA12	DISABLED		PTA12		FTM1_ CH0			I2S0_ TXD0	FTM1_ QD_PHA	
G6	29	36	43	L8	PTA13/ LLWU_P4	DISABLED		PTA13/ LLWU_P4		FTM1_ CH1			I2S0_TX_ FS	FTM1_ QD_PHB	
—	—	37	44	K9	PTA14	DISABLED		PTA14	SPI0_ PCS0	UART0_ TX			I2S0_RX_ BCLK		
—	—	38	45	L9	PTA15	DISABLED		PTA15	SPI0_SCK	UART0_ RX			I2S0_ RXD0		
—	—	39	46	J10	PTA16	DISABLED		PTA16	SPI0_ SOUT	UART0_ CTS_b			I2S0_RX_ FS		
—	—	40	47	H10	PTA17	ADC1_ SE17	ADC1_ SE17	PTA17	SPI0_SIN	UART0_ RTS_b			I2S0_ MCLK		
G7	30	41	48	L10	VDD	VDD	VDD								
H7	31	42	49	K10	VSS	VSS	VSS								
H8	32	43	50	L11	PTA18	EXTAL0	EXTAL0	PTA18		FTM0_ FLT2	FTM_ CLKIN0				
G8	33	44	51	K11	PTA19	XTAL0	XTAL0	PTA19		FTM1_ FLT0	FTM_ CLKIN1		LPTMR0_ ALT1		
F8	34	45	52	J11	RESET_b	RESET_b	RESET_b								
—	—	—	—	H11	PTA29	DISABLED		PTA29					FB_A24		
F7	35	46	53	G11	PTB0/ LLWU_P5	ADC0_ SE8/ ADC1_ SE8	ADC0_ SE8/ ADC1_ SE8	PTB0/ LLWU_P5	I2C0_SCL	FTM1_ CH0			FTM1_ QD_PHA		
F6	36	47	54	G10	PTB1	ADC0_ SE9/ ADC1_ SE9	ADC0_ SE9/ ADC1_ SE9	PTB1	I2C0_SDA	FTM1_ CH1			FTM1_ QD_PHB		
E7	37	48	55	G9	PTB2	ADC0_ SE12	ADC0_ SE12	PTB2	I2C0_SCL	UART0_ RTS_b			FTM0_ FLT3		
E8	38	49	56	G8	PTB3	ADC0_ SE13	ADC0_ SE13	PTB3	I2C0_SDA	UART0_ CTS_b			FTM0_ FLT0		
—	—	50	—	F11	PTB6	ADC1_ SE12	ADC1_ SE12	PTB6				FB_AD23			
—	—	51	—	E11	PTB7	ADC1_ SE13	ADC1_ SE13	PTB7				FB_AD22			
—	—	52	—	D11	PTB8	DISABLED		PTB8		LPUART0 _RTS_b		FB_AD21			

64 MAP BGA	64 LQFP	88 QFN	100 LQFP	121 MAP BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EZPORT
—	—	53	57	E10	PTB9	DISABLED		PTB9	SPI1_ PCS1	LPUART0 _CTS_b		FB_AD20			
—	—	54	58	D10	PTB10	ADC1_ SE14	ADC1_ SE14	PTB10	SPI1_ PCS0	LPUART0 _RX		FB_AD19	FTM0_ FLT1		
—	—	55	59	C10	PTB11	ADC1_ SE15	ADC1_ SE15	PTB11	SPI1_SCK	LPUART0 _TX		FB_AD18	FTM0_ FLT2		
—	—	—	60	—	VSS	VSS	VSS								
—	—	—	61	—	VDD	VDD	VDD								
E6	39	56	62	B10	PTB16	DISABLED		PTB16	SPI1_ SOUT	UART0_ RX	FTM_ CLKIN0	FB_AD17	EWM_IN		
D7	40	57	63	E9	PTB17	DISABLED		PTB17	SPI1_SIN	UART0_ TX	FTM_ CLKIN1	FB_AD16	EWM_ OUT_b		
D6	41	58	64	D9	PTB18	DISABLED		PTB18		FTM2_ CH0	I2S0_TX_ BCLK	FB_AD15	FTM2_ QD_PHA		
C7	42	59	65	C9	PTB19	DISABLED		PTB19		FTM2_ CH1	I2S0_TX_ FS	FB_OE_b	FTM2_ QD_PHB		
—	—	—	66	F10	PTB20	DISABLED		PTB20				FB_AD31	CMP0_ OUT		
—	—	—	67	F9	PTB21	DISABLED		PTB21				FB_AD30	CMP1_ OUT		
—	—	—	68	F8	PTB22	DISABLED		PTB22				FB_AD29			
—	—	—	69	E8	PTB23	DISABLED		PTB23		SPI0_ PCS5		FB_AD28			
D8	43	60	70	B9	PTC0	ADC0_ SE14	ADC0_ SE14	PTC0	SPI0_ PCS4	PDB0_ EXTRG	USB_ SOF_OUT	FB_AD14			
C6	44	61	71	D8	PTC1/ LLWU_P6	ADC0_ SE15	ADC0_ SE15	PTC1/ LLWU_P6	SPI0_ PCS3	UART1_ RTS_b	FTM0_ CH0	FB_AD13	I2S0_ TXD0	LPUART0 _RTS_b	
B7	45	62	72	C8	PTC2	ADC0_ SE4b/ CMP1_IN0	ADC0_ SE4b/ CMP1_IN0	PTC2	SPI0_ PCS2	UART1_ CTS_b	FTM0_ CH1	FB_AD12	I2S0_TX_ FS	LPUART0 _CTS_b	
C8	46	63	73	B8	PTC3/ LLWU_P7	CMP1_IN1	CMP1_IN1	PTC3/ LLWU_P7	SPI0_ PCS1	UART1_ RX	FTM0_ CH2	CLKOUT	I2S0_TX_ BCLK	LPUART0 _RX	
E3	47	64	74	—	VSS	VSS	VSS								
E4	48	65	75	—	VDD	VDD	VDD								
B8	49	66	76	A8	PTC4/ LLWU_P8	DISABLED		PTC4/ LLWU_P8	SPI0_ PCS0	UART1_ TX	FTM0_ CH3	FB_AD11	CMP1_ OUT	LPUART0 _TX	
A8	50	67	77	D7	PTC5/ LLWU_P9	DISABLED		PTC5/ LLWU_P9	SPI0_SCK	LPTMR0_ ALT2	I2S0_ RXD0	FB_AD10	CMP0_ OUT	FTM0_ CH2	
A7	51	68	78	C7	PTC6/ LLWU_ P10	CMP0_IN0	CMP0_IN0	PTC6/ LLWU_ P10	SPI0_ SOUT	PDB0_ EXTRG	I2S0_RX_ BCLK	FB_AD9	I2S0_ MCLK		
B6	52	69	79	B7	PTC7	CMP0_IN1	CMP0_IN1	PTC7	SPI0_SIN	USB_ SOF_OUT	I2S0_RX_ FS	FB_AD8			

6.4 Example

This is an example part number:

MK22FN512VDC12

6.5 121-pin XFBGA part marking

The 121-pin XFBGA package parts follow the part-marking scheme in the following table.

Table 52. 121-pin XFBGA part marking

MK Partnumber	MK Part Marking
MK22FN512VDC12	M22J9VDC

6.6 64-pin MAPBGA part marking

The 64-pin MAPBGA package parts follow the part-marking scheme in the following table.

Table 53. 64-pin MAPBGA part marking

MK Partnumber	MK Part Marking
MK22FN512VMP12	M22J9V

7 Terminology and guidelines

7.1 Definitions

Key terms are defined in the following table:

Term	Definition
Rating	A minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure: • *Operating ratings* apply during operation of the chip. • *Handling ratings* apply when the chip is not powered.

Table continues on the next page...