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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB, USB OTG
Peripherals	DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	66
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 33x16b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mk22fn512vll12

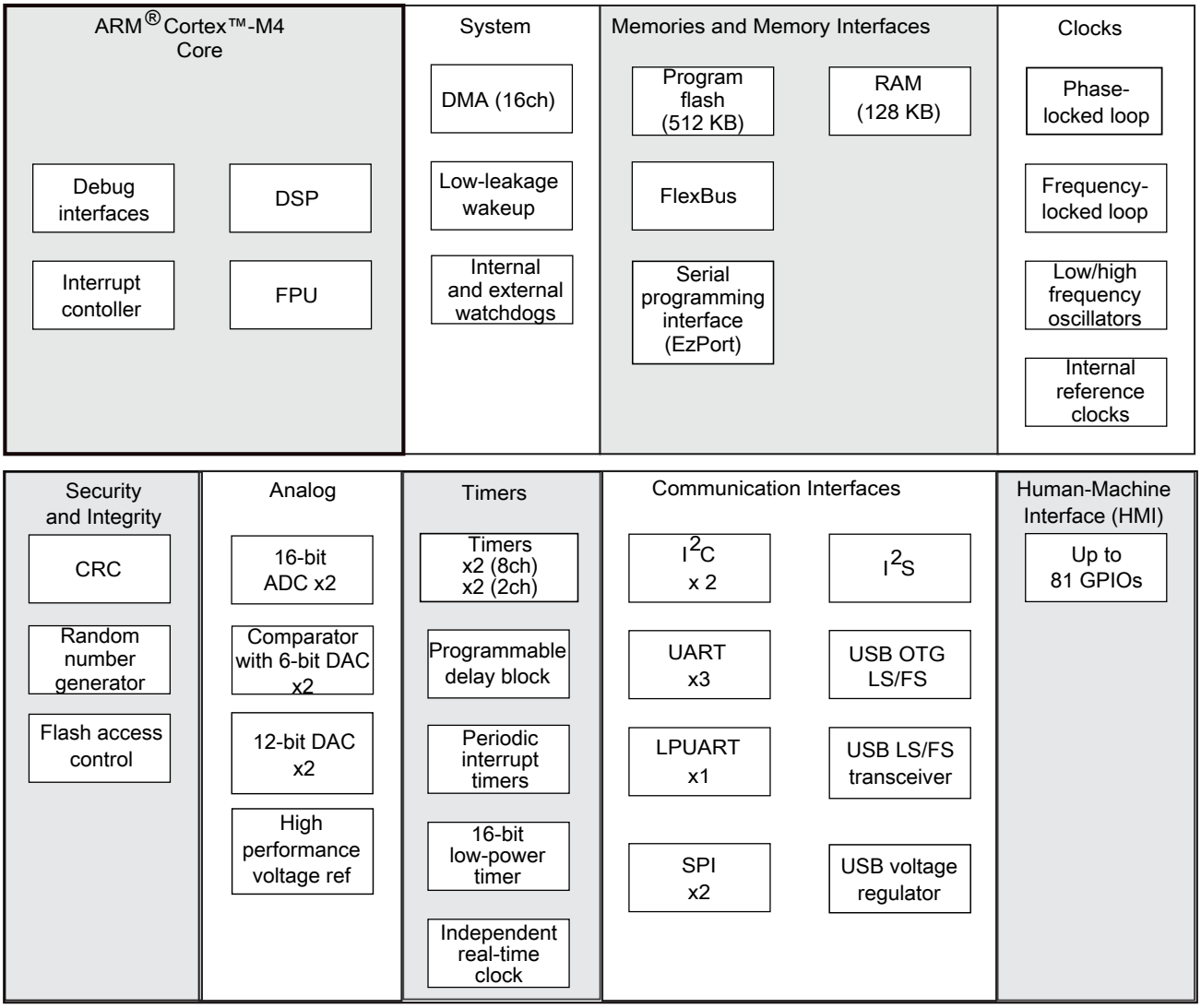


Figure 1. Functional block diagram

Table 6. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DD_WAIT}	Wait mode high frequency current at 3.0 V — all peripheral clocks disabled	—	9.3	10.63	mA	7
I_{DD_WAIT}	Wait mode reduced frequency current at 3.0 V — all peripheral clocks disabled	—	5.4	6.73	mA	10
I_{DD_VLPR}	Very-low-power run mode current in Compute operation — CoreMark benchmark code executing from flash					
	@ 1.8V	—	0.88	1.02	mA	3, 4, 11
	@ 3.0V	—	0.89	1.03	mA	
I_{DD_VLPR}	Very-low-power run mode current in Compute operation, code executing from flash					
	@ 1.8V	—	0.62	0.77	mA	11
	@ 3.0V	—	0.63	0.77	mA	
I_{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks disabled	—	0.76	0.90	mA	12
I_{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks enabled	—	1.2	1.34	mA	13
I_{DD_VLPW}	Very-low-power wait mode current at 3.0 V — all peripheral clocks disabled	—	0.45	0.59	mA	14
I_{DD_STOP}	Stop mode current at 3.0 V					
	@ -40°C to 25°C	—	0.28	0.37	mA	
	@ 70°C	—	0.34	0.51	mA	
	@ 85°C	—	0.38	0.55	mA	
	@ 105°C	—	0.50	0.80	mA	
I_{DD_VLPS}	Very-low-power stop mode current at 3.0 V					
	@ -40°C to 25°C	—	8.7	18.10	µA	
	@ 70°C	—	31.1	79.55	µA	
	@ 85°C	—	50.3	110.15	µA	
	@ 105°C	—	98.6	238.30	µA	
I_{DD_LLS3}	Low leakage stop mode 3 current at 3.0 V					
	@ -40°C to 25°C	—	3.8	5.65	µA	
	@ 70°C	—	12.5	28.75	µA	
	@ 85°C	—	20.2	47.60	µA	
	@ 105°C	—	39.5	91.25	µA	
I_{DD_LLS2}	Low leakage stop mode 2 current at 3.0 V					
	@ -40°C to 25°C	—	3.0	4.10	µA	
	@ 70°C	—	7.8	16.40	µA	
	@ 85°C	—	12.3	30.15	µA	
	@ 105°C	—	23.6	55.30	µA	
I_{DD_VLLS3}	Very low-leakage stop mode 3 current at 3.0 V					
	@ -40°C to 25°C	—	2.8	3.95	µA	

Table continues on the next page...

Table 6. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	@ 70°C	—	9.5	21.25	µA	
	@ 85°C	—	15.3	34.65	µA	
	@ 105°C	—	30.1	66.05	µA	
I_{DD_VLLS2}	Very low-leakage stop mode 2 current at 3.0 V					
	@ -40°C to 25°C	—	1.9	2.45	µA	
	@ 70°C	—	4.5	8.50	µA	
	@ 85°C	—	6.8	12.15	µA	
	@ 105°C	—	13.0	25.50	µA	
I_{DD_VLLS1}	Very low-leakage stop mode 1 current at 3.0 V					
	@ -40°C to 25°C	—	0.73	1.42	µA	
	@ 70°C	—	1.8	3.90	µA	
	@ 85°C	—	3.0	5.25	µA	
	@ 105°C	—	5.9	10.80	µA	
I_{DD_VLLS0}	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit enabled					
	@ -40°C to 25°C	—	0.43	0.55	µA	
	@ 70°C	—	1.4	2.45	µA	
	@ 85°C	—	2.6	4.00	µA	
	@ 105°C	—	5.4	9.30	µA	
I_{DD_VLLS0}	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit disabled					
	@ -40°C to 25°C	—	0.14	0.24	µA	
	@ 70°C	—	1.1	2.15	µA	
	@ 85°C	—	2.3	3.85	µA	
	@ 105°C	—	5.1	9.00	µA	
I_{DD_VBAT}	Average current with RTC and 32kHz disabled at 3.0 V					
	@ -40°C to 25°C	—	0.18	0.21	µA	
	@ 70°C	—	0.66	0.86	µA	
	@ 85°C	—	1.52	2.24	µA	
	@ 105°C	—	2.92	4.30	µA	
I_{DD_VBAT}	Average current when CPU is not accessing RTC registers					
	@ 1.8V					
	• @ -40°C to 25°C	—	0.59	0.70	µA	15
	• @ 70°C	—	1.00	1.3	µA	
	• @ 85°C	—	1.76	2.59	µA	
	• @ 105°C	—	3.00	4.42	µA	
	@ 3.0V					

Table continues on the next page...

3. The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.
4. IEC Level Maximums: M ≤ 18dBmV, L ≤ 24dBmV, K ≤ 30dBmV, I ≤ 36dBmV, H ≤ 42dBmV .

2.2.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

- Go to nxp.com
- Perform a keyword search for "EMC design."

2.2.8 Capacitance attributes

Table 9. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C_{IN_A}	Input capacitance: analog pins	—	7	pF
C_{IN_D}	Input capacitance: digital pins	—	7	pF

2.3 Switching specifications

2.3.1 Device clock specifications

Table 10. Device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes
High Speed run mode					
f_{SYS}	System and core clock	—	120	MHz	
f_{BUS}	Bus clock	—	60	MHz	
Normal run mode (and High Speed run mode unless otherwise specified above)					
f_{SYS}	System and core clock	—	80	MHz	
f_{SYS_USB}	System and core clock when Full Speed USB in operation	20	—	MHz	
f_{BUS}	Bus clock	—	50	MHz	
FB_CLK	FlexBus clock	—	30	MHz	
f_{FLASH}	Flash clock	—	26.67	MHz	
f_{LPTMR}	LPTMR clock	—	25	MHz	
VLPR mode[1]					

Table continues on the next page...

Board type	Symbol	Description	121 XFBGA	100 LQFP	64 LQFP	64 MAPBGA	Unit	Notes
		center (natural convection)						

1. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*with the single layer board horizontal. Board meets JESD51-9 specification.
2. Determined according to JEDEC Standard JESD51-2, Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air).
3. Determined according to JEDEC Standard JESD51-6, Integrated Circuits Thermal Test Method Environmental Conditions—Forced Convection (Moving Air) with the board horizontal.
4. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

2.4.3 Thermal attributes for 88 QFN

Board type	Symbol	Description	88 QFN	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	55	°C/W	1, 2
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	20	°C/W	1, 2
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./ min. air speed)	50	°C/W	1, 3
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./ min. air speed)	15	°C/W	1,3
—	$R_{\theta JB}$	Thermal resistance, junction to board	7	°C/W	4
—	$R_{\theta JC}$	Thermal resistance, junction to case	1	°C/W	5
—	Ψ_{JT}	Thermal characterization	1	°C/W	6

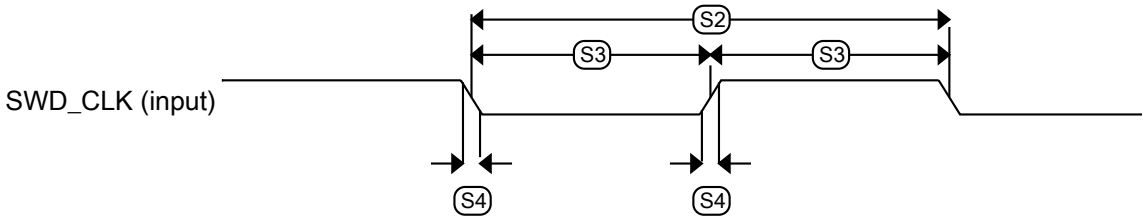


Figure 5. Serial wire clock input timing

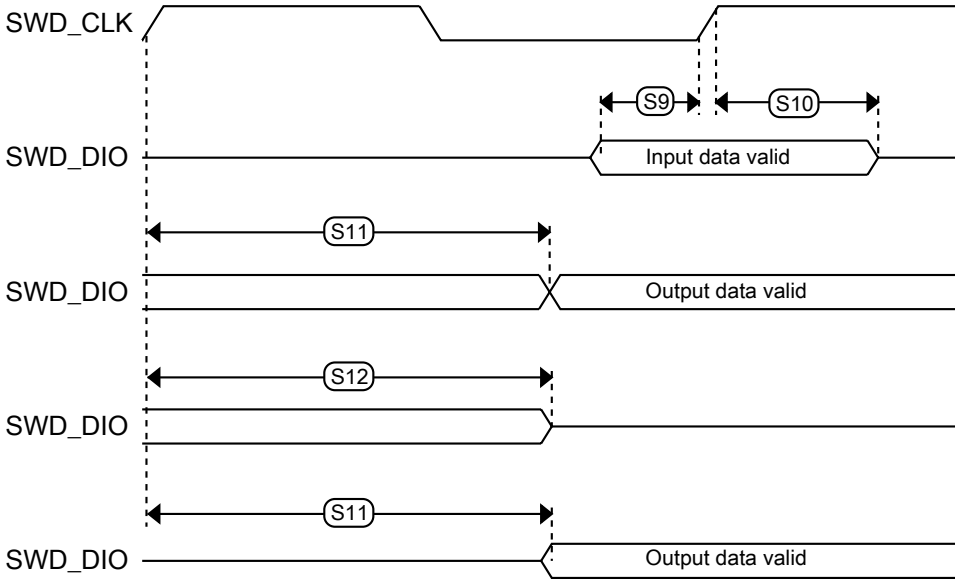


Figure 6. Serial wire data timing

3.1.2 JTAG electricals

Table 14. JTAG limited voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
J1	TCLK frequency of operation • Boundary Scan • JTAG and CJTAG	 0 0	 10 20	MHz
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width	50	—	ns

Table continues on the next page...

Table 24. Flash high voltage current behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit
I_{DD_ERS}	Average current adder during high voltage flash erase operation	—	1.5	4.0	mA

3.4.1.4 Reliability specifications

Table 25. NVM reliability specifications

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
Program Flash						
$t_{nvmretp10k}$	Data retention after up to 10 K cycles	5	50	—	years	—
$t_{nvmretp1k}$	Data retention after up to 1 K cycles	20	100	—	years	—
$n_{nvmcycp}$	Cycling endurance	10 K	50 K	—	cycles	2

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25 °C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at –40 °C ≤ T_j ≤ 125 °C.

3.4.2 EzPort switching specifications

Table 26. EzPort switching specifications

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
EP1	EZP_CK frequency of operation (all commands except READ)	—	$f_{SYS}/2$	MHz
EP1a	EZP_CK frequency of operation (READ command)	—	$f_{SYS}/8$	MHz
EP2	$\overline{\text{EZP\_CS}}$ negation to next $\overline{\text{EZP\_CS}}$ assertion	2 x t_{EZP_CK}	—	ns
EP3	$\overline{\text{EZP\_CS}}$ input valid to EZP_CK high (setup)	5	—	ns
EP4	EZP_CK high to $\overline{\text{EZP\_CS}}$ input invalid (hold)	5	—	ns
EP5	EZP_D input valid to EZP_CK high (setup)	2	—	ns
EP6	EZP_CK high to EZP_D input invalid (hold)	5	—	ns
EP7	EZP_CK low to EZP_Q output valid	—	25	ns
EP8	EZP_CK low to EZP_Q output invalid (hold)	0	—	ns
EP9	$\overline{\text{EZP\_CS}}$ negation to EZP_Q tri-state	—	12	ns

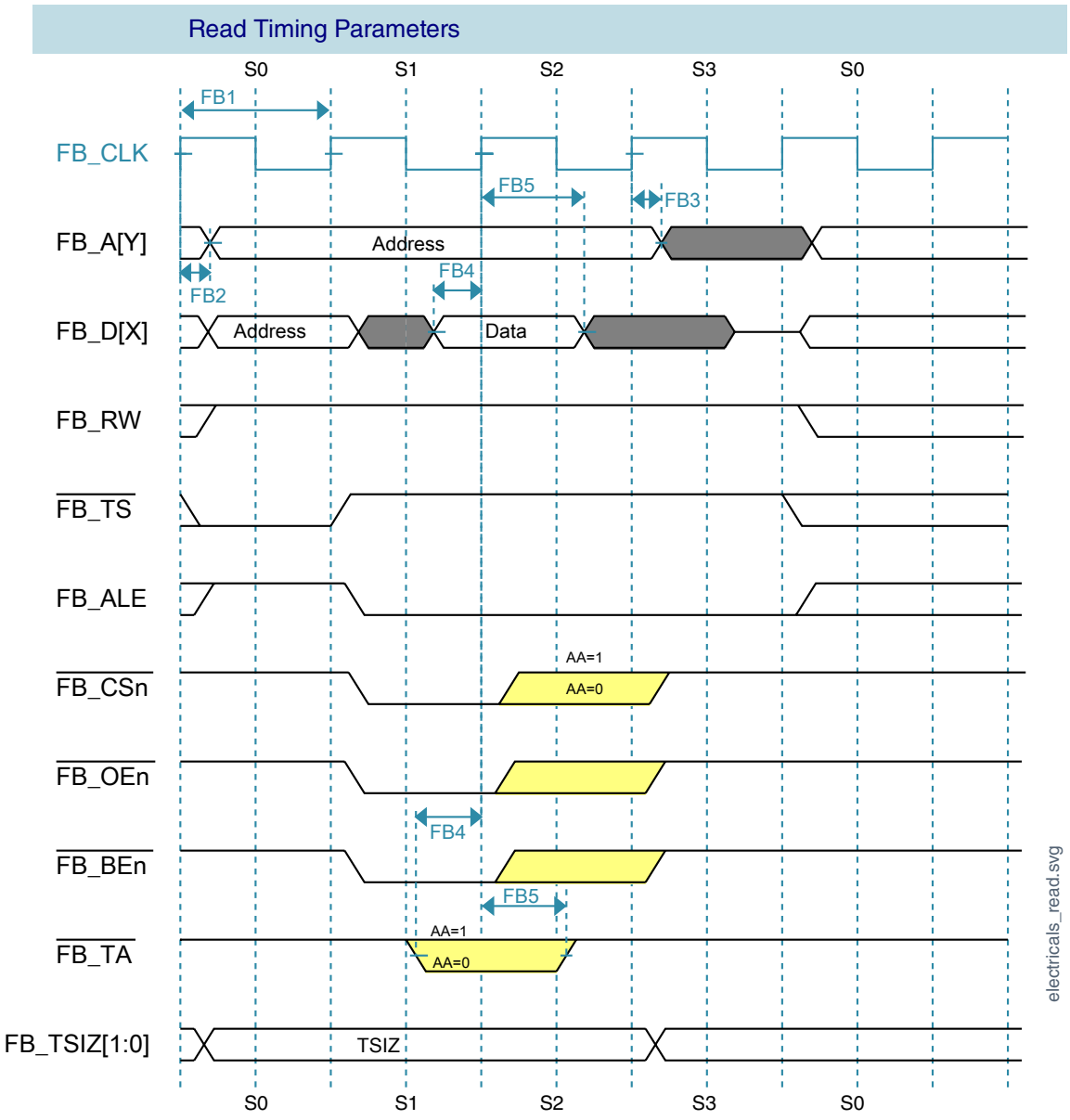


Figure 12. FlexBus read timing diagram

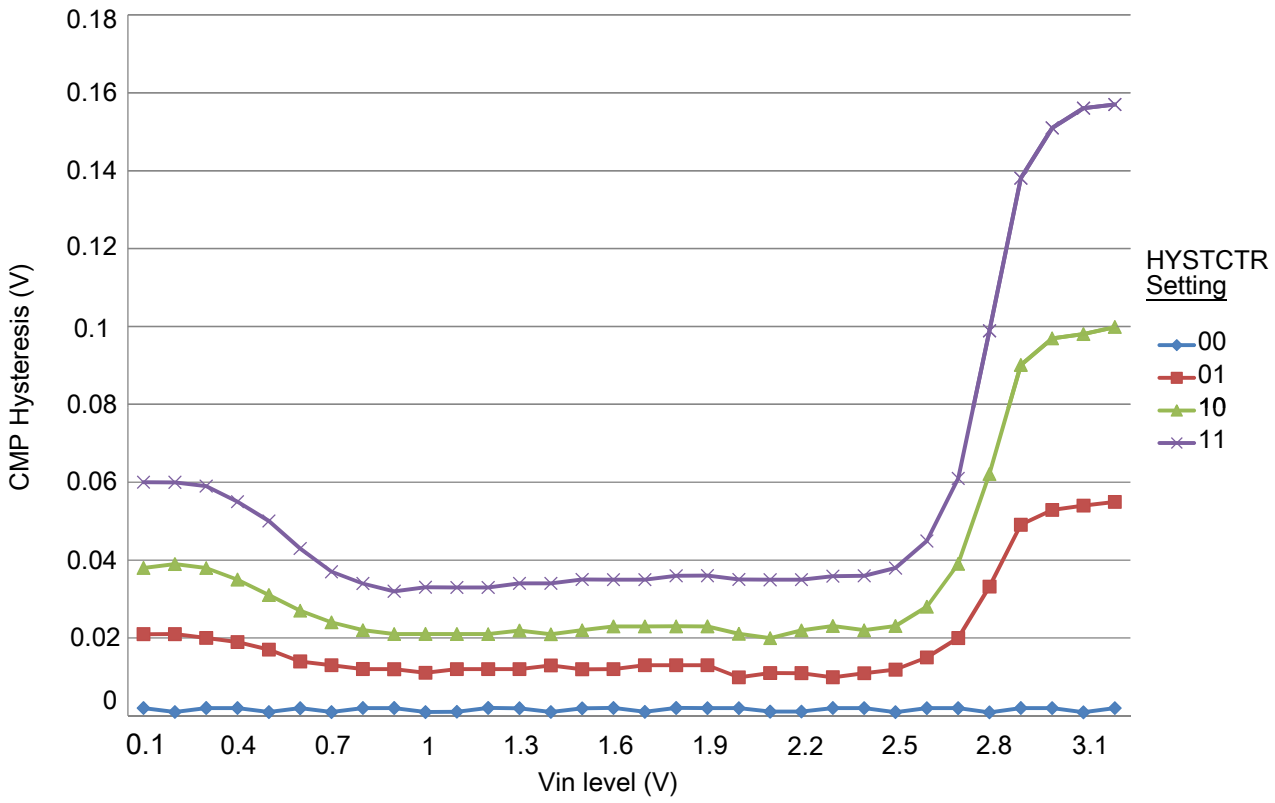


Figure 18. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 1)

3.6.3 12-bit DAC electrical characteristics

3.6.3.1 12-bit DAC operating requirements

Table 32. 12-bit DAC operating requirements

Symbol	Desciption	Min.	Max.	Unit	Notes
V_{DDA}	Supply voltage	1.71	3.6	V	
V_{DACR}	Reference voltage	1.13	3.6	V	1
C_L	Output load capacitance	—	100	pF	2
I_L	Output load current	—	1	mA	

1. The DAC reference can be selected to be V_{DDA} or V_{REFH}.
2. A small load capacitance (47 pF) can improve the bandwidth performance of the DAC.

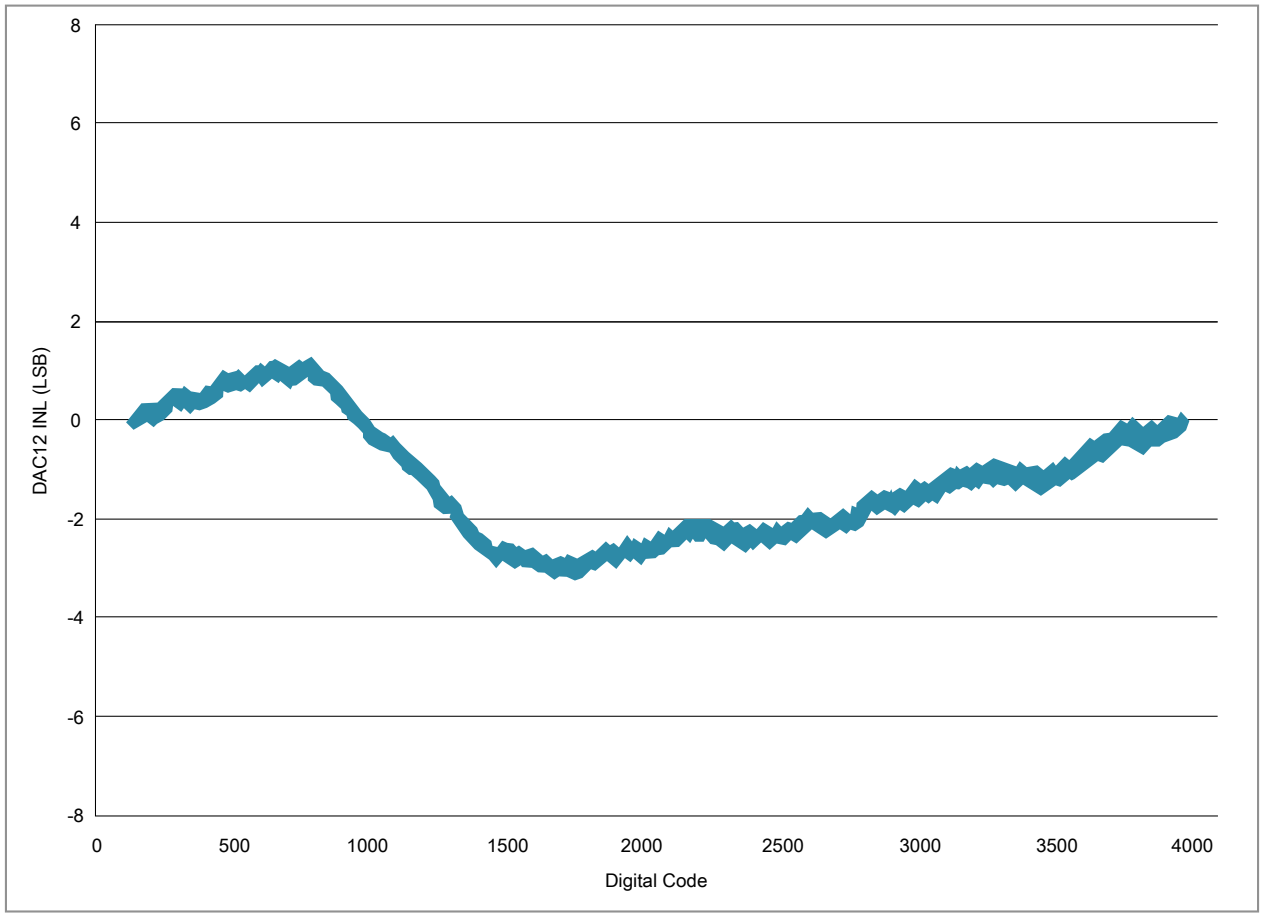


Figure 19. Typical INL error vs. digital code

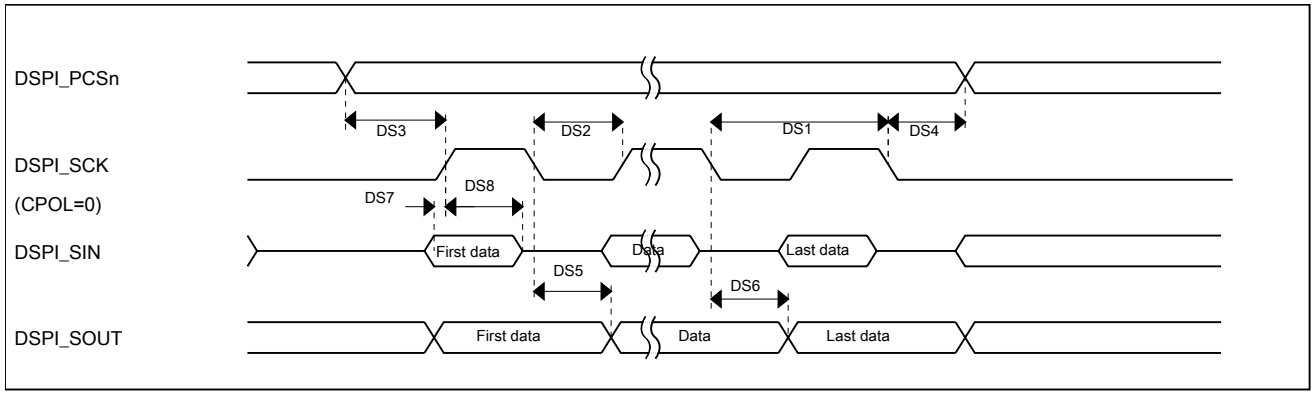


Figure 21. DSPI classic SPI timing — master mode

Table 40. Slave mode DSPI timing (limited voltage range)

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	2.7	3.6	V	
	Frequency of operation	—	15	MHz	1
DS9	DSPI_SCK input cycle time	4 x t_{BUS}	—	ns	
DS10	DSPI_SCK input high/low time	(t_{SCK}/2) – 2	(t_{SCK}/2) + 2	ns	
DS11	DSPI_SCK to DSPI_SOUT valid	—	21.4	ns	
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns	
DS13	DSPI_SIN to DSPI_SCK input setup	2.6	—	ns	
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns	
DS15	$\overline{\text{DSPI\_SS}}$ active to DSPI_SOUT driven	—	17	ns	
DS16	$\overline{\text{DSPI\_SS}}$ inactive to DSPI_SOUT not driven	—	17	ns	

1. The maximum operating frequency is measured with noncontinuous CS and SCK. When DSPI is configured with continuous CS and SCK, the SPI clock must not be greater than 1/6 of the bus clock. For example, when the bus clock is 60 MHz, the SPI clock must not be greater than 10 MHz.

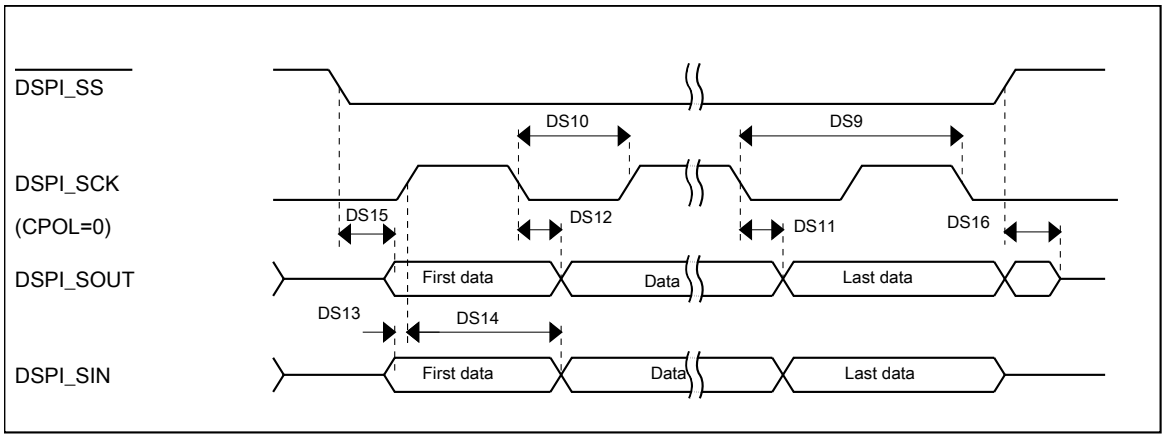


Figure 22. DSPI classic SPI timing — slave mode

1. The maximum SCL clock frequency of 1 Mbps can support maximum bus loading when using the High drive pins across the full voltage range.
2. C_b = total capacitance of the one bus line in pF.

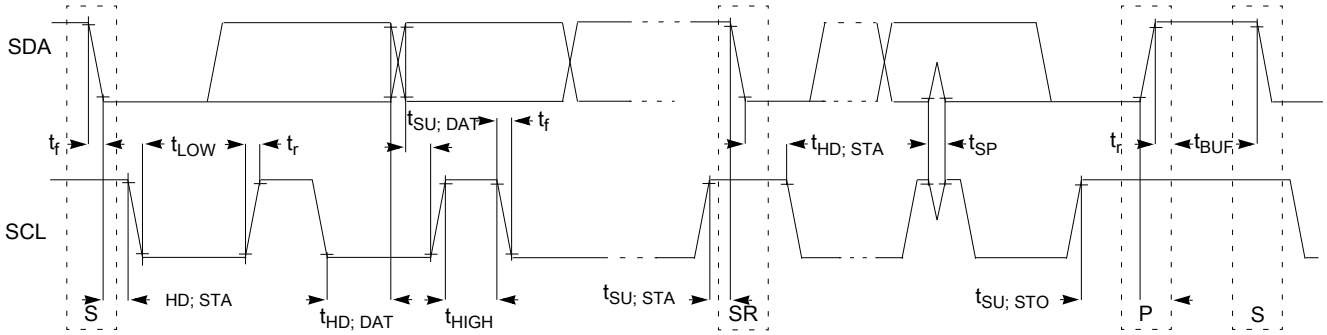


Figure 25. Timing definition for devices on the I²C bus

3.8.6 UART switching specifications

See General switching specifications.

3.8.7 I2S/SAI switching specifications

This section provides the AC timing for the I2S/SAI module in master mode (clocks are driven) and slave mode (clocks are input). All timing is given for noninverted serial clock polarity (TCR2[BCP] is 0, RCR2[BCP] is 0) and a noninverted frame sync (TCR4[FSP] is 0, RCR4[FSP] is 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the bit clock signal (BCLK) and/or the frame sync (FS) signal shown in the following figures.

3.8.7.1 Normal Run, Wait and Stop mode performance over a limited operating voltage range

This section provides the operating performance over a limited operating voltage for the device in Normal Run, Wait and Stop modes.

Table 45. I2S/SAI master mode timing in Normal Run, Wait and Stop modes (limited voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
S1	I2S_MCLK cycle time	40	—	ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period

Table continues on the next page...

Table 49. I2S/SAI master mode timing in VLPR, VLPW, and VLPS modes (full voltage range) (continued)

Num.	Characteristic	Min.	Max.	Unit
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid	—	45	ns
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid	-1	—	ns
S7	I2S_TX_BCLK to I2S_TXD valid	—	45	ns
S8	I2S_TX_BCLK to I2S_TXD invalid	0	—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	45	—	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns

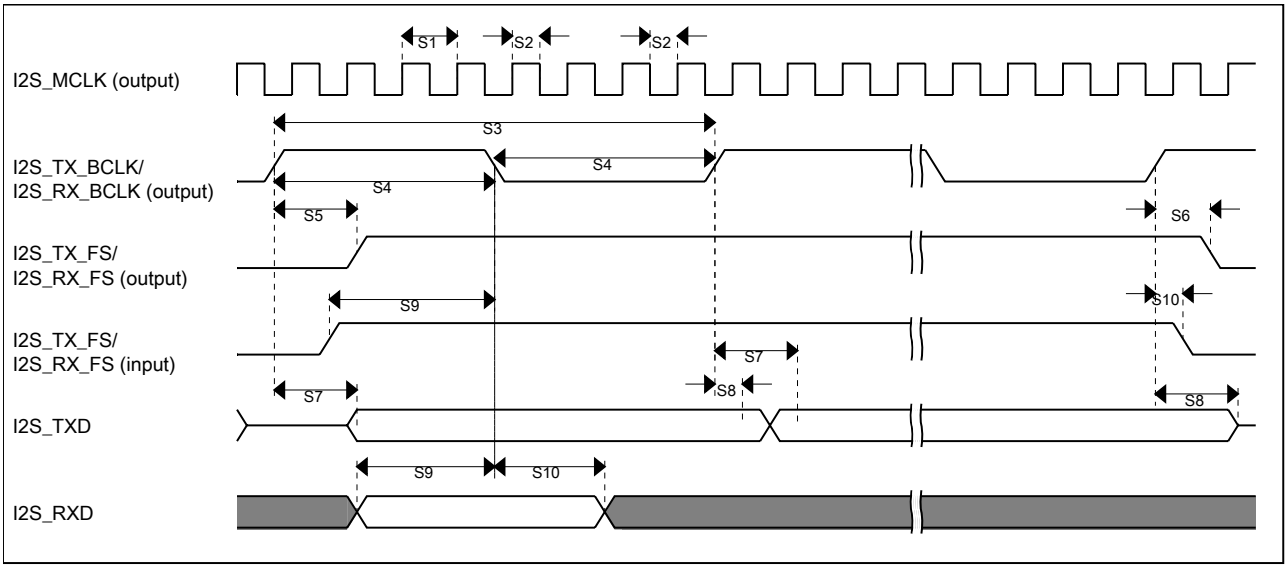


Figure 30. I2S/SAI timing — master modes

Table 50. I2S/SAI slave mode timing in VLPR, VLPW, and VLPS modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	250	—	ns
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	30	—	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	7	—	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid	—	63	ns

Table continues on the next page...

64 MAP BGA	64 LQFP	88 QFN	100 LQFP	121 MAP BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EZPORT
—	—	33	40	E5	VDD	VDD	VDD								
—	—	34	41	G3	VSS	VSS	VSS								
—	—	—	—	J9	PTA10	DISABLED		PTA10		FTM2_ CH0			FTM2_ QD_PHA		
—	—	—	—	J4	PTA11	DISABLED		PTA11		FTM2_ CH1			FTM2_ QD_PHB		
H6	28	35	42	K8	PTA12	DISABLED		PTA12		FTM1_ CH0			I2S0_ TXD0	FTM1_ QD_PHA	
G6	29	36	43	L8	PTA13/ LLWU_P4	DISABLED		PTA13/ LLWU_P4		FTM1_ CH1			I2S0_TX_ FS	FTM1_ QD_PHB	
—	—	37	44	K9	PTA14	DISABLED		PTA14	SPI0_ PCS0	UART0_ TX			I2S0_RX_ BCLK		
—	—	38	45	L9	PTA15	DISABLED		PTA15	SPI0_SCK	UART0_ RX			I2S0_ RXD0		
—	—	39	46	J10	PTA16	DISABLED		PTA16	SPI0_ SOUT	UART0_ CTS_b			I2S0_RX_ FS		
—	—	40	47	H10	PTA17	ADC1_ SE17	ADC1_ SE17	PTA17	SPI0_SIN	UART0_ RTS_b			I2S0_ MCLK		
G7	30	41	48	L10	VDD	VDD	VDD								
H7	31	42	49	K10	VSS	VSS	VSS								
H8	32	43	50	L11	PTA18	EXTAL0	EXTAL0	PTA18		FTM0_ FLT2	FTM_ CLKIN0				
G8	33	44	51	K11	PTA19	XTAL0	XTAL0	PTA19		FTM1_ FLT0	FTM_ CLKIN1		LPTMR0_ ALT1		
F8	34	45	52	J11	RESET_b	RESET_b	RESET_b								
—	—	—	—	H11	PTA29	DISABLED		PTA29					FB_A24		
F7	35	46	53	G11	PTB0/ LLWU_P5	ADC0_ SE8/ ADC1_ SE8	ADC0_ SE8/ ADC1_ SE8	PTB0/ LLWU_P5	I2C0_SCL	FTM1_ CH0			FTM1_ QD_PHA		
F6	36	47	54	G10	PTB1	ADC0_ SE9/ ADC1_ SE9	ADC0_ SE9/ ADC1_ SE9	PTB1	I2C0_SDA	FTM1_ CH1			FTM1_ QD_PHB		
E7	37	48	55	G9	PTB2	ADC0_ SE12	ADC0_ SE12	PTB2	I2C0_SCL	UART0_ RTS_b			FTM0_ FLT3		
E8	38	49	56	G8	PTB3	ADC0_ SE13	ADC0_ SE13	PTB3	I2C0_SDA	UART0_ CTS_b			FTM0_ FLT0		
—	—	50	—	F11	PTB6	ADC1_ SE12	ADC1_ SE12	PTB6				FB_AD23			
—	—	51	—	E11	PTB7	ADC1_ SE13	ADC1_ SE13	PTB7				FB_AD22			
—	—	52	—	D11	PTB8	DISABLED		PTB8		LPUART0 _RTS_b		FB_AD21			

64 MAP BGA	64 LQFP	88 QFN	100 LQFP	121 MAP BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EZPORT
—	—	53	57	E10	PTB9	DISABLED		PTB9	SPI1_ PCS1	LPUART0 _CTS_b		FB_AD20			
—	—	54	58	D10	PTB10	ADC1_ SE14	ADC1_ SE14	PTB10	SPI1_ PCS0	LPUART0 _RX		FB_AD19	FTM0_ FLT1		
—	—	55	59	C10	PTB11	ADC1_ SE15	ADC1_ SE15	PTB11	SPI1_SCK	LPUART0 _TX		FB_AD18	FTM0_ FLT2		
—	—	—	60	—	VSS	VSS	VSS								
—	—	—	61	—	VDD	VDD	VDD								
E6	39	56	62	B10	PTB16	DISABLED		PTB16	SPI1_ SOUT	UART0_ RX	FTM_ CLKIN0	FB_AD17	EWM_IN		
D7	40	57	63	E9	PTB17	DISABLED		PTB17	SPI1_SIN	UART0_ TX	FTM_ CLKIN1	FB_AD16	EWM_ OUT_b		
D6	41	58	64	D9	PTB18	DISABLED		PTB18		FTM2_ CH0	I2S0_TX_ BCLK	FB_AD15	FTM2_ QD_PHA		
C7	42	59	65	C9	PTB19	DISABLED		PTB19		FTM2_ CH1	I2S0_TX_ FS	FB_OE_b	FTM2_ QD_PHB		
—	—	—	66	F10	PTB20	DISABLED		PTB20				FB_AD31	CMP0_ OUT		
—	—	—	67	F9	PTB21	DISABLED		PTB21				FB_AD30	CMP1_ OUT		
—	—	—	68	F8	PTB22	DISABLED		PTB22				FB_AD29			
—	—	—	69	E8	PTB23	DISABLED		PTB23		SPI0_ PCS5		FB_AD28			
D8	43	60	70	B9	PTC0	ADC0_ SE14	ADC0_ SE14	PTC0	SPI0_ PCS4	PDB0_ EXTRG	USB_ SOF_OUT	FB_AD14			
C6	44	61	71	D8	PTC1/ LLWU_P6	ADC0_ SE15	ADC0_ SE15	PTC1/ LLWU_P6	SPI0_ PCS3	UART1_ RTS_b	FTM0_ CH0	FB_AD13	I2S0_ TXD0	LPUART0 _RTS_b	
B7	45	62	72	C8	PTC2	ADC0_ SE4b/ CMP1_IN0	ADC0_ SE4b/ CMP1_IN0	PTC2	SPI0_ PCS2	UART1_ CTS_b	FTM0_ CH1	FB_AD12	I2S0_TX_ FS	LPUART0 _CTS_b	
C8	46	63	73	B8	PTC3/ LLWU_P7	CMP1_IN1	CMP1_IN1	PTC3/ LLWU_P7	SPI0_ PCS1	UART1_ RX	FTM0_ CH2	CLKOUT	I2S0_TX_ BCLK	LPUART0 _RX	
E3	47	64	74	—	VSS	VSS	VSS								
E4	48	65	75	—	VDD	VDD	VDD								
B8	49	66	76	A8	PTC4/ LLWU_P8	DISABLED		PTC4/ LLWU_P8	SPI0_ PCS0	UART1_ TX	FTM0_ CH3	FB_AD11	CMP1_ OUT	LPUART0 _TX	
A8	50	67	77	D7	PTC5/ LLWU_P9	DISABLED		PTC5/ LLWU_P9	SPI0_SCK	LPTMR0_ ALT2	I2S0_ RXD0	FB_AD10	CMP0_ OUT	FTM0_ CH2	
A7	51	68	78	C7	PTC6/ LLWU_ P10	CMP0_IN0	CMP0_IN0	PTC6/ LLWU_ P10	SPI0_ SOUT	PDB0_ EXTRG	I2S0_RX_ BCLK	FB_AD9	I2S0_ MCLK		
B6	52	69	79	B7	PTC7	CMP0_IN1	CMP0_IN1	PTC7	SPI0_SIN	USB_ SOF_OUT	I2S0_RX_ FS	FB_AD8			

	1	2	3	4	5	6	7	8	
A	PTE0/ CLKOUT32K	PTD7	PTD4/ LLWU_P14	PTD1	PTC11/ LLWU_P11	PTC8	PTC6/ LLWU_P10	PTC5/ LLWU_P9	A
B	PTE1/ LLWU_P0	PTD6/ LLWU_P15	PTD3	PTC10	PTC9	PTC7	PTC2	PTC4/ LLWU_P8	B
C	PTD5	PTD2/ LLWU_P13	PTD0/ LLWU_P12	VSS	VDD	PTC1/ LLWU_P6	PTB19	PTC3/ LLWU_P7	C
D	USB0_DM	VREGIN	PTA0	PTA1	PTA3	PTB18	PTB17	PTC0	D
E	USB0_DP	VOUT33	VSS	VDD	PTA2	PTB16	PTB2	PTB3	E
F	ADC0_DM0/ ADC1_DM3	ADC1_DM0/ ADC0_DM3	VSSA	VDDA	PTA5	PTB1	PTB0/ LLWU_P5	RESET_b	F
G	ADC0_DP0/ ADC1_DP3	ADC1_DP0/ ADC0_DP3	VREFL	VREFH	PTA4/ LLWU_P3	PTA13/ LLWU_P4	VDD	PTA19	G
H	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18	DAC0_OUT/ CMP1_IN3/ ADC0_SE23	XTAL32	EXTAL32	VBAT	PTA12	VSS	PTA18	H
	1	2	3	4	5	6	7	8	

Figure 33. K22F 64 MAPBGA pinout diagram (transparent top view)

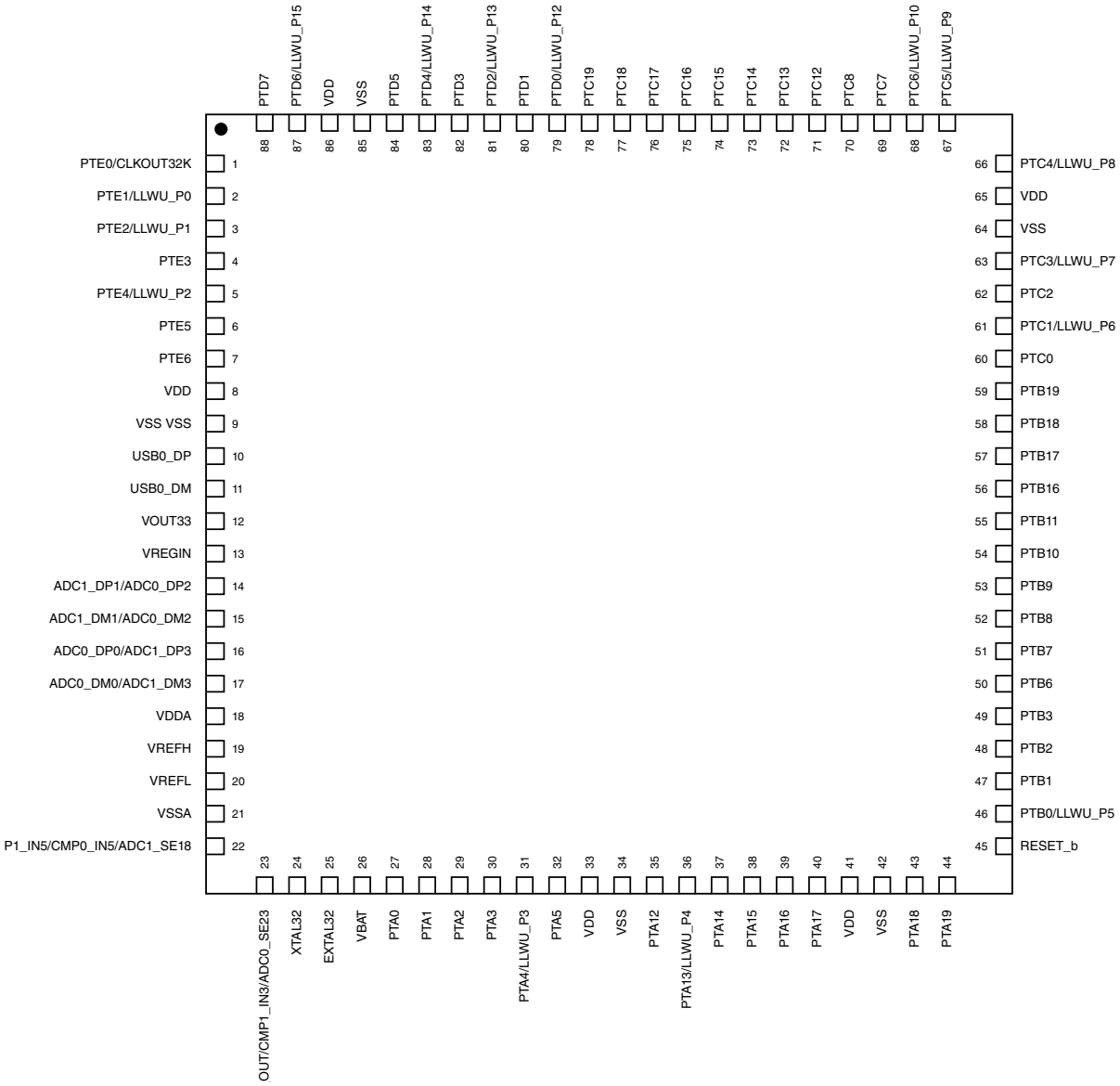


Figure 34. K22F 88 QFN pinout diagram (transparent top view)

NOTE

For more information about QFN package use, see Electrical Connection Recommendations for the Exposed Pad on QFN and DFN Packages .

	1	2	3	4	5	6	7	8	9	10	11	
A	PTD7	PTD5	PTD4/ LLWU_P14	PTC19	PTC14	PTC13	PTC8	PTC4/ LLWU_P8	PTD9	PTD8	NC	A
B	PTD10	PTD6/ LLWU_P15	PTD3	PTC18	PTC15	PTC12	PTC7	PTC3/ LLWU_P7	PTC0	PTB16	NC	B
C	PTD12	PTD11	PTD2/ LLWU_P13	PTC17	PTC11/ LLWU_P11	PTC10	PTC6/ LLWU_P10	PTC2	PTB19	PTB11	NC	C
D	PTD14	PTD13	PTD1	PTD0/ LLWU_P12	PTC16	PTC9	PTC5/ LLWU_P9	PTC1/ LLWU_P6	PTB18	PTB10	PTB8	D
E	PTD15	PTE2/ LLWU_P1	PTE1/ LLWU_P0	PTE0/ CLKOUT32K	VDD	VDD	VDD	PTB23	PTB17	PTB9	PTB7	E
F	USB0_DP	USB0_DM	PTE6	PTE3	VDDA	VSSA	VSS	PTB22	PTB21	PTB20	PTB6	F
G	VOUT33	VREGIN	VSS	PTE5	VREFH	VREFL	VSS	PTB3	PTB2	PTB1	PTB0/ LLWU_P5	G
H	ADC0_DP1	ADC0_DM1	ADC0_SE16/ CMP1_IN2/ ADC0_SE21	NC	PTE24	PTE26/ CLKOUT32K	PTE4/ LLWU_P2	PTA1	PTA3	PTA17	PTA29	H
J	ADC1_DP1/ ADC0_DP2	ADC1_DM1/ ADC0_DM2	ADC1_SE16/ ADC0_SE22	PTA11	PTE25	PTA0	PTA2	PTA4/ LLWU_P3	PTA10	PTA16	RESET_b	J
K	ADC0_DP0/ ADC1_DP3	ADC0_DM0/ ADC1_DM3	NC	DAC1_OUT/ CMP0_IN4/ ADC1_SE23	DAC0_OUT/ CMP1_IN3/ ADC0_SE23	VBAT	PTA5	PTA12	PTA14	VSS	PTA19	K
L	ADC1_DP0/ ADC0_DP3	ADC1_DM0/ ADC0_DM3	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18	XTAL32	EXTAL32	VSS	RTC_ WAKEUP_B	PTA13/ LLWU_P4	PTA15	VDD	PTA18	L
	1	2	3	4	5	6	7	8	9	10	11	

Figure 36. K22F 121 XFBGA pinout diagram (transparent top view)

6 Part identification

6.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

6.2 Format

Part numbers for this device have the following format:

Q K## A M FFF R T PP CC N

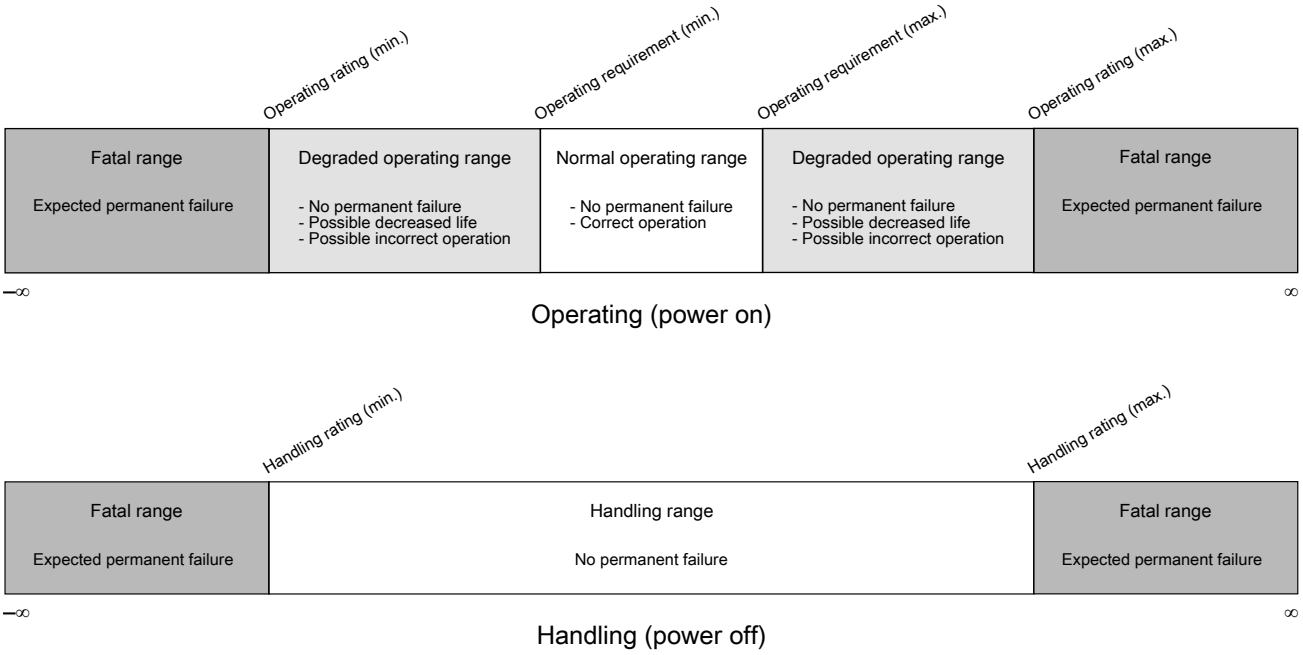
6.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
Q	Qualification status	• M = Fully qualified, general market flow, full reel • P = Prequalification • K = Fully qualified, general market flow, 100 piece reel
K##	Kinetis family	• K22
A	Key attribute	• D = Cortex-M4 w/ DSP • F = Cortex-M4 w/ DSP and FPU
M	Flash memory type	• N = Program flash only • X = Program flash and FlexMemory
FFF	Program flash memory size	• 128 = 128 KB • 256 = 256 KB • 512 = 512 KB
R	Silicon revision	• Z = Initial • (Blank) = Main • A = Revision after main
T	Temperature range (°C)	• V = –40 to 105 • C = –40 to 85
PP	Package identifier	• LH = 64 LQFP (10 mm x 10 mm) • MP = 64 MAPBGA (5 mm x 5 mm) • FX = 88 QFN (10mm x 10mm) • LL = 100 LQFP (14 mm x 14 mm) • MC = 121 XFBGA (8 mm x 8 mm) • DC = 121 XFBGA (8 mm x 8 mm x 0.5 mm)
CC	Maximum CPU frequency (MHz)	• 5 = 50 MHz • 7 = 72 MHz • 10 = 100 MHz • 12 = 120 MHz • 15 = 150 MHz
N	Packaging type	• R = Tape and reel

Symbol	Description	Value	Unit
T_A	Ambient temperature	25	°C
V_{DD}	Supply voltage	3.3	V

7.4 Relationship between ratings and operating requirements



7.5 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

8 Revision History

The following table provides a revision history for this document.