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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	C28x
Core Size	32-Bit Single-Core
Speed	150MHz
Connectivity	CANbus, EBI/EMI, I²C, McBSP, SCI, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	88
Program Memory Size	512KB (256K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	34K x 16
Voltage - Supply (Vcc/Vdd)	1.805V ~ 1.995V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-55°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-BGA
Supplier Device Package	176-BGA (15x15)
Purchase URL	https://www.e-xfl.com/product-detail/texas-instruments/sm320f28335gjzmep

2. SAM3N Block Diagram

Figure 2-1. SAM3N 100-pin version Block Diagram

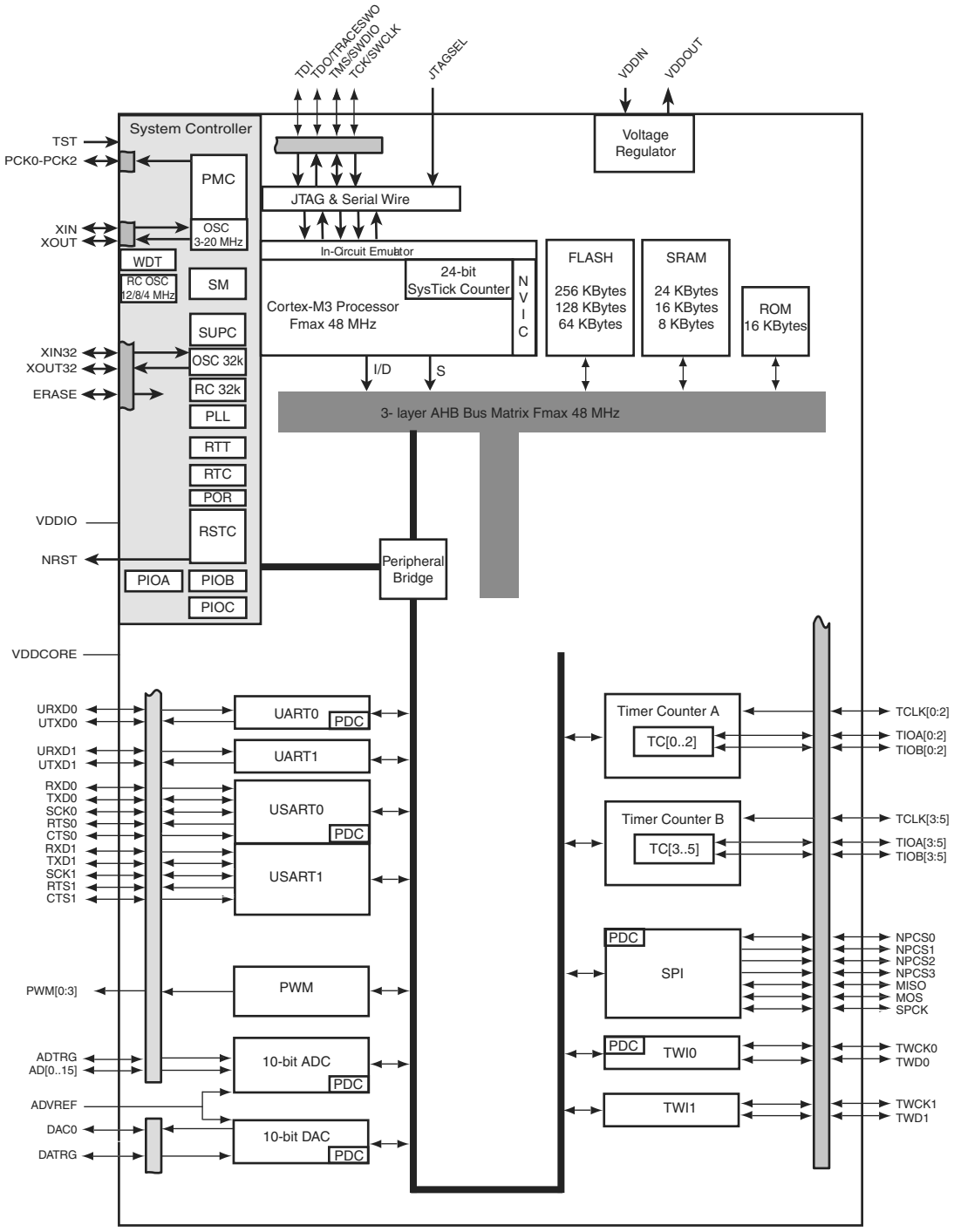
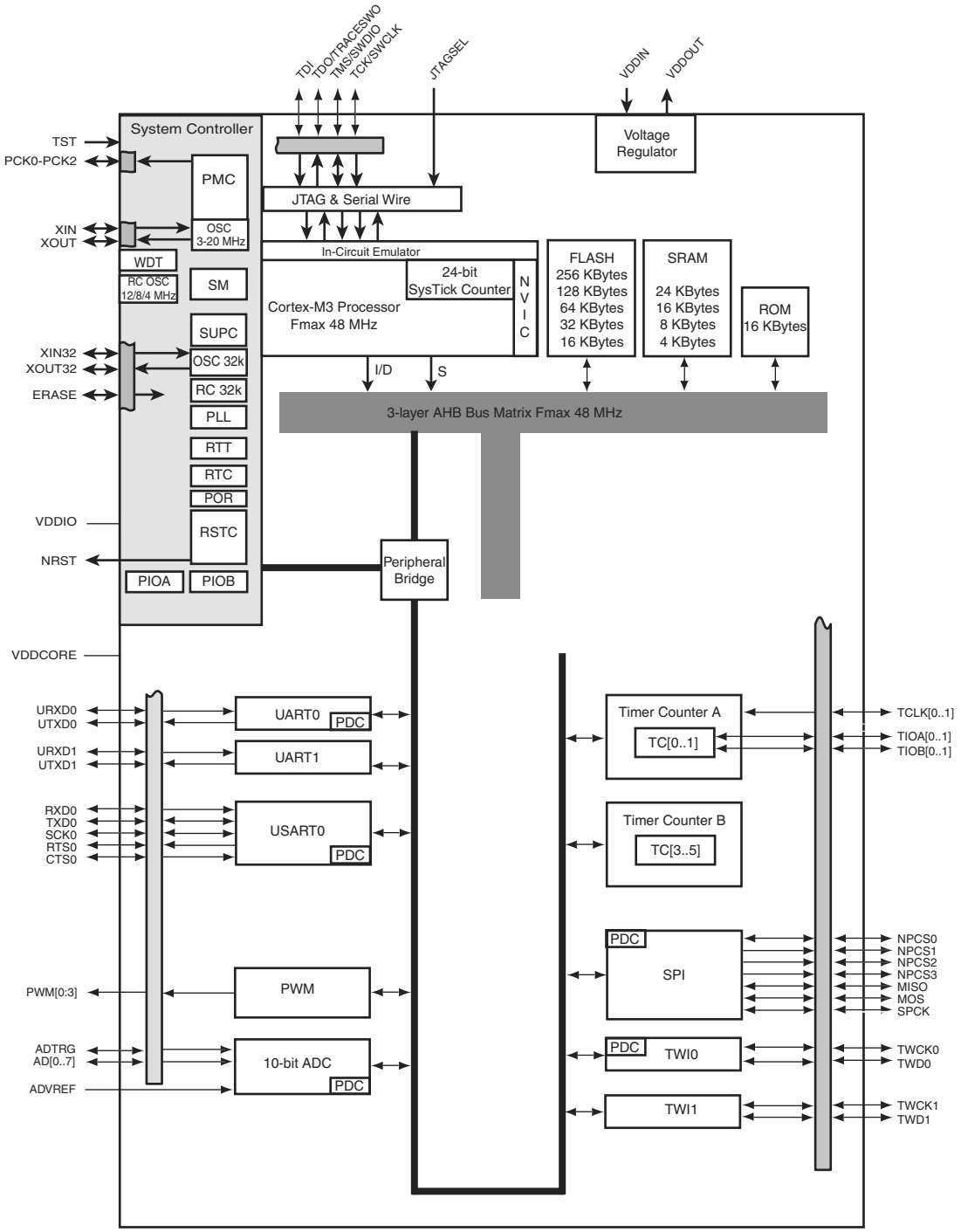


Figure 2-3. SAM3N 48-pin version Block Diagramz



4.3 SAM3N4/2/1/0/00A Package and Pinout

Figure 4-5. Orientation of the 48-pad QFN Package

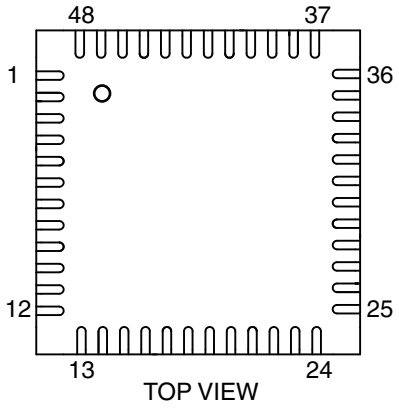


Figure 4-6. Orientation of the 48-lead LQFP Package

48

1

4.3.1 48-Lead LQFP and QFN Pinout

Table 4-4. 48-pin SAM3N4/2/1/0/00A Pinout

1	ADVREF	13	VDDIO	25	*TDI/PB4*	37	*TDO/TRACESWO/ PB5*
2	GND	14	PA16/PGMD4	26	PA6/PGMNOE	38	JTAGSEL
3	*PB0/AD4*	15	PA15/PGMD3	27	PA5/PGMRDY	39	*TMS/SWDIO/PB6*
4	*PB1/AD5*	16	PA14/PGMD2	28	PA4/PGMNCMD	40	*TCK/SWCLK/PB7*
5	*PB2/AD6*	17	PA13/PGMD1	29	NRST	41	VDDCORE
6	*PB3/AD7*	18	VDDCORE	30	TST	42	*ERASE/PB12*
7	VDDIN	19	PA12/PGMD0	31	PA3	43	*PB10*
8	VDDOUT	20	PA11/PGMM3	32	PA2/PGMEN2	44	*PB11*
9	PA17/PGMD5/AD0	21	PA10/PGMM2	33	VDDIO	45	*XOUT/PB8*
10	PA18/PGMD6/AD1	22	PA9/PGMM1	34	GND	46	*XIN/P/PB9/GMCK*
11	PA19/PGMD7/AD2	23	PA8/XOUT32/PGMM0	35	PA1/PGMEN1	47	VDDIO
12	PA20/AD3	24	PA7/XIN32/PGMNVALID	36	PA0/PGMEN0	48	VDDPLL

Note: The bottom pad of the QFN package must be connected to ground.

Figure 5-1. Single Supply

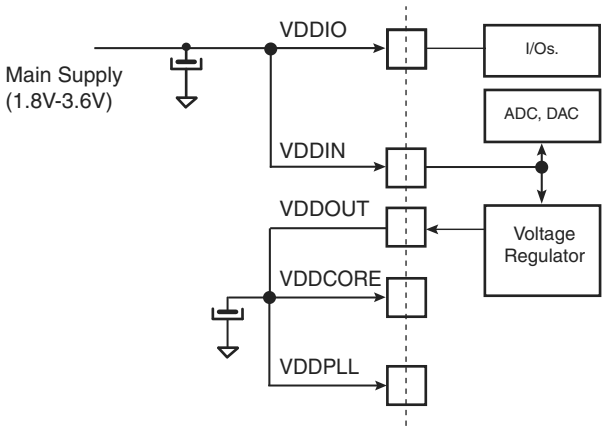
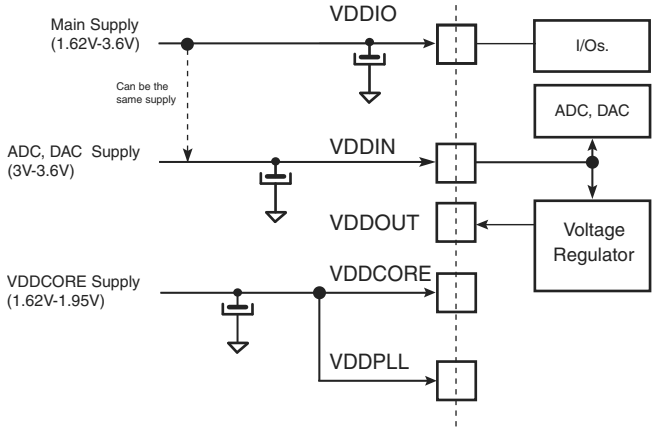


Figure 5-2. Core Externally Supplied



Note: Restrictions
With Main Supply < 3V, ADC and DAC are not usable.
With Main Supply >= 3V, all peripherals are usable.

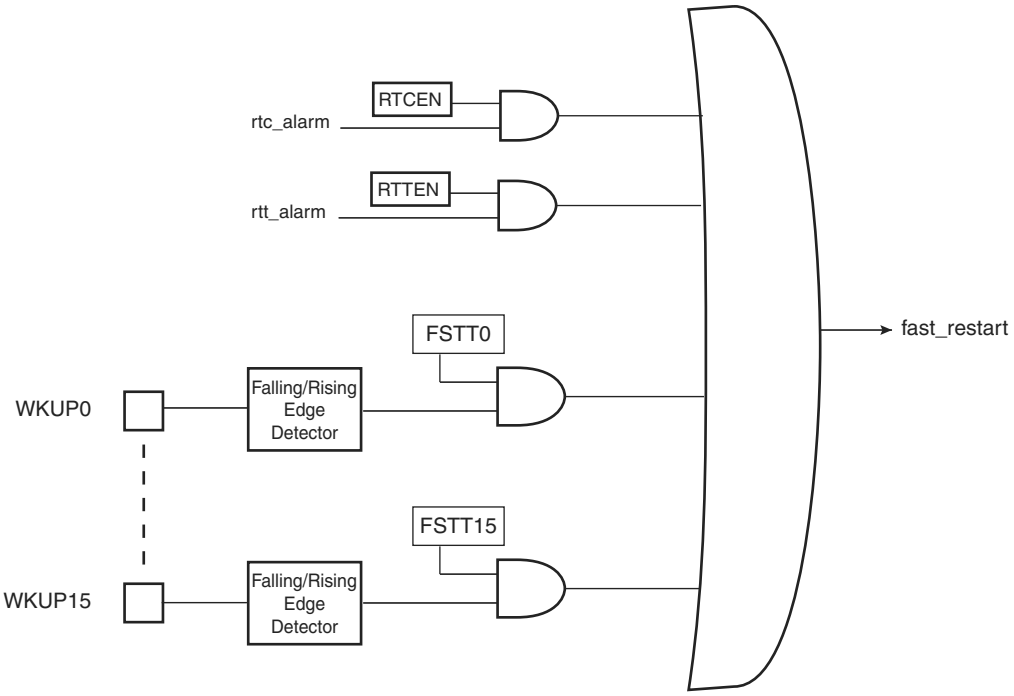
Figure 5-3 below provides an example of the powering scheme when using a backup battery. Since the PIO state is preserved when in backup mode, any free PIO line can be used to switch off the external regulator by driving the PIO line at low level (PIO is input, pull-up enabled after backup reset). External wake-up of the system can be from a push button or any signal. See Section 5.6 “Wake-up Sources” for further details.TFBGA

5.7 Fast Start-Up

The SAM3N allows the processor to restart in a few microseconds while the processor is in wait mode. A fast start up can occur upon detection of a low level on one of the 19 wake-up inputs (WKUP0 to 15 + SM + RTC + RTT).

The fast restart circuitry, as shown in Figure 5-5, is fully asynchronous and provides a fast start-up signal to the Power Management Controller. As soon as the fast start-up signal is asserted, the PMC automatically restarts the embedded 4 MHz fast RC oscillator, switches the master clock on this 4 MHz clock and reenables the processor clock.

Figure 5-5. Fast Start-Up Sources



6.3 Test Pin

The TST pin is used for JTAG Boundary Scan Manufacturing Test or Fast Flash programming mode of the SAM3N series. The TST pin integrates a permanent pull-down resistor of about 15 kΩ to GND, so that it can be left unconnected for normal operations. To enter fast programming mode, see the Fast Flash Programming Interface (FFPI) section. For more on the manufacturing and test mode, refer to the “Debug and Test” section of the product datasheet.

6.4 NRST Pin

The NRST pin is bidirectional. It is handled by the on-chip reset controller and can be driven low to provide a reset signal to the external components or asserted low externally to reset the microcontroller. It will reset the Core and the peripherals except the Backup region (RTC, RTT and Supply Controller). There is no constraint on the length of the reset pulse and the reset controller can guarantee a minimum pulse length. The NRST pin integrates a permanent pull-up resistor to VDDIO of about 100 kΩ. By default, the NRST pin is configured as an input.

6.5 ERASE Pin

The ERASE pin is used to reinitialize the Flash content (and some of its NVM bits) to an erased state (all bits read as logic level 1). It integrates a pull-down resistor of about 100 kΩ to GND, so that it can be left unconnected for normal operations.

This pin is debounced by SCLK to improve the glitch tolerance. When the ERASE pin is tied high during less than 100 ms, it is not taken into account. The pin must be tied high during more than 220 ms to perform a Flash erase operation.

The ERASE pin is a system I/O pin and can be used as a standard I/O. At startup, the ERASE pin is not configured as a PIO pin. If the ERASE pin is used as a standard I/O, startup level of this pin must be low to prevent unwanted erasing. Please refer to Section 11.2 “Peripheral Signals Multiplexing on I/O Lines” on page 42. Also, if the ERASE pin is used as a standard I/O output, asserting the pin to low does not erase the Flash.

7.7 Debug and Test Features

- Debug access to all memory and registers in the system, including Cortex-M3 register bank when the core is running, halted, or held in reset.
- Serial Wire Debug Port (SW-DP) and Serial Wire JTAG Debug Port (SWJ-DP) debug access
- Flash Patch and Breakpoint (FPB) unit for implementing breakpoints and code patches
- Data Watchpoint and Trace (DWT) unit for implementing watchpoints, data tracing, and system profiling
- Instrumentation Trace Macrocell (ITM) for support of printf style debugging
- IEEE1149.1 JTAG Boundary-can on All Digital Pins

9.1.3.9 *Fast Flash Programming Interface*

The Fast Flash Programming Interface allows programming the device through either a serial JTAG interface or through a multiplexed fully-handshaked parallel port. It allows gang programming with market-standard industrial programmers.

The FFPI supports read, page program, page erase, full erase, lock, unlock and protect commands.

The Fast Flash Programming Interface is enabled and the Fast Programming Mode is entered when TST and PA0 and PA1are tied low.

9.1.3.10 *SAM-BA Boot*

The SAM-BA Boot is a default Boot Program which provides an easy way to program in-situ the on-chip Flash memory.

The SAM-BA Boot Assistant supports serial communication via the UART0.

The SAM-BA Boot provides an interface with SAM-BA Graphic User Interface (GUI).

The SAM-BA Boot is in ROM and is mapped in Flash at address 0x0 when GPNVM bit 1 is set to 0.

9.1.3.11 *GPNVM Bits*

The SAM3N features three GPNVM bits that can be cleared or set respectively through the commands “Clear GPNVM Bit” and “Set GPNVM Bit” of the EEFC User Interface.

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Table 9-2. General-purpose Non volatile Memory Bits

GPNVMBit[#]	Function
0	Security bit
1	Boot mode selection

9.1.4 Boot Strategies

The system always boots at address 0x0. To ensure a maximum boot possibilities the memory layout can be changed via GPNVM.

A general purpose NVM (GPNVM) bit is used to boot either on the ROM (default) or from the Flash.

The GPNVM bit can be cleared or set respectively through the commands “Clear General-purpose NVM Bit” and “Set General-purpose NVM Bit” of the EEFC User Interface.

Setting the GPNVM Bit 1 selects the boot from the Flash, clearing it selects the boot from the ROM. Asserting ERASE clears the GPNVM Bit 1 and thus selects the boot from the ROM by default.

10. System Controller

The System Controller is a set of peripherals, which allow handling of key elements of the system, such as power, resets, clocks, time, interrupts, watchdog, etc...

See the System Controller block diagram in Figure 10-1 on page 35.

10.8 SysTick Timer

- 24-bit down counter
- Self-reload capability
- Flexible System timer

10.9 Real-time Timer

- Real-time Timer, allowing backup of time with different accuracies
  - 32-bit Free-running back-up Counter
  - Integrates a 16-bit programmable prescaler running on slow clock
  - Alarm register capable to generate a wake-up of the system through the Shut Down Controller

10.10 Real Time Clock

- Low power consumption
- Full asynchronous design
- Two hundred year calendar
- Programmable Periodic Interrupt
- Alarm and update parallel load
- Control of alarm and update Time/Calendar Data In

10.11 General Purpose Backup Registers

- Eight 32-bit general-purpose backup registers

10.12 Nested Vectored Interrupt Controller

- Thirty Two maskable external interrupts
- Sixteen priority levels
- Processor state automatically saved on interrupt entry, and restored on
- Dynamic reprioritization of interrupts
- Priority grouping
  - selection of pre-empting interrupt levels and non pre-empting interrupt levels
- Support for tail-chaining and late arrival of interrupts
  - back-to-back interrupt processing without the overhead of state saving and restoration between interrupts.
- Processor state automatically saved on interrupt entry and restored on interrupt exit, with no instruction overhead

10.13 Chip Identification

- Chip Identifier (CHIPID) registers permit recognition of the device and its revision.

Table 10-1. SAM3N Chip ID Register

Chip Name	CHIPID_CIDR	CHIPID_EXID
ATSAM3N4C (Rev A)	0x29540960	0x0
ATSAM3N2C (Rev A)	0x29590760	0x0
ATSAM3N1C (Rev A)	0x29580560	0x0
ATSAM3N4B (Rev A)	0x29440960	0x0
ATSAM3N2B (Rev A)	0x29490760	0x0
ATSAM3N1B (Rev A)	0x29480560	0x0
ATSAM3N4A (Rev A)	0x29340960	0x0
ATSAM3N2A (Rev A)	0x29390760	0x0
ATSAM3N1A (Rev A)	0x29380560	0x0

- JTAG ID: 0x05B2E03F

10.14 UART

- Two-pin UART
  - Implemented features are 100% compatible with the standard Atmel USART
  - Independent receiver and transmitter with a common programmable Baud Rate Generator
  - Even, Odd, Mark or Space Parity Generation
  - Parity, Framing and Overrun Error Detection
  - Automatic Echo, Local Loopback and Remote Loopback Channel Modes
  - Support for two PDC channels with connection to receiver and transmitter

10.15 PIO Controllers

- 3 PIO Controllers, PIOA, PIOB and PIOC (100-pin version only) controlling a maximum of 79 I/O Lines
- Each PIO Controller controls up to 32 programmable I/O Lines
- Fully programmable through Set/Clear Registers

Table 10-2. PIO available according to pin count

Version	48 pin	64 pin	100 pin
PIOA	21	32	32
PIOB	13	15	15
PIOC	-	-	32

- Multiplexing of four peripheral functions per I/O Line
- For each I/O Line (whether assigned to a peripheral or used as general purpose I/O)
  - Input change, rising edge, falling edge, low level and level interrupt
  - Debouncing and Glitch filter

– Multi-drive option enables driving in open drain
– Programmable pull up on each I/O line
– Pin data status register, supplies visibility of the level on the pin at any time

• Selection of the drive level
• Synchronous output, provides Set and Clear of several I/O lines in a single write

11. Peripherals

11.1 Peripheral Identifiers

Table 11-1 defines the Peripheral Identifiers of the SAM3N4/2/1/0/00. A peripheral identifier is required for the control of the peripheral interrupt with the Nested Vectored Interrupt Controller and for the control of the peripheral clock with the Power Management Controller.

Table 11-1. Peripheral Identifiers

Instance ID	Instance Name	NVIC Interrupt	PMC Clock Control	Instance Description
0	SUPC	**X**		**Supply Controller**
1	RSTC	**X**		Reset Controller
2	RTC	**X**		Real Time Clock
3	RTT	**X**		Real Time Timer
4	WDT	**X**		Watchdog Timer
5	PMC	**X**		Power Management Controller
6	EEFC	**X**		Enhanced Flash Controller
7	-	**-**		Reserved
8	UART0	**X**	**X**	UART 0
9	UART1	**X**	**X**	UART 1
10	-	**-**	**-**	Reserved
11	PIOA	**X**	**X**	Parallel I/O Controller A
12	PIOB	**X**	**X**	Parallel I/O Controller B
13	PIOC	**X**	**X**	Parallel I/O Controller C
14	USART0	**X**	**X**	USART 0
15	USART1	**X**	**X**	USART 1
16	-	**-**	**-**	Reserved
17	-	**-**	**-**	Reserved
18	-	**-**	**-**	Reserved
19	TWI0	**X**	**X**	Two Wire Interface 0
20	TWI1	**X**	**X**	Two Wire Interface 1
21	SPI	**X**	**X**	Serial Peripheral Interface
22	-	**-**	**-**	Reserved
23	TC0	**X**	**X**	Timer/Counter 0
24	TC1	**X**	**X**	Timer/Counter 1

Table 11-1. Peripheral Identifiers (Continued)

Instance ID	Instance Name	NVIC Interrupt	PMC Clock Control	Instance Description
25	TC2	**X**	**X**	Timer/Counter 2
26	TC3	**X**	**X**	Timer/Counter 3
27	TC4	**X**	**X**	Timer/Counter 4
28	TC5	**X**	**X**	Timer/Counter 5
29	ADC	**X**	**X**	Analog-to-Digital Converter
30	DACC	**X**	**X**	Digital-to-Analog Converter
31	PWM	**X**	**X**	Pulse Width Modulation

11.2 Peripheral Signals Multiplexing on I/O Lines

The SAM3N product features 2 PIO controllers (48-pin and 64-pin version) or 3 PIO controllers (100-pin version), PIOA, PIOB and PIOC, that multiplex the I/O lines of the peripheral set.

The SAM3N 64-pin and 100-pin PIO Controller controls up to 32 lines (see Table 10-2, “PIO available according to pin count,” on page 40). Each line can be assigned to one of three peripheral functions: A, B or C. The multiplexing tables in the following paragraphs define how the I/O lines of the peripherals A, B and C are multiplexed on the PIO Controllers. The column “Comments” has been inserted in this table for the user’s own comments; it may be used to track how pins are defined in an application.

Note that some peripheral functions which are output only, might be duplicated within the tables.

11.2.1 PIO Controller A Multiplexing

Table 11-2. Multiplexing on PIO Controller A (PIOA)

I/O Line	Peripheral A	Peripheral B	Peripheral C	Extra Function	System Function	Comments
PA0	PWM0	TIOA0		WKUP0		High drive
PA1	PWM1	TIOB0		WKUP1		High drive
PA2	PWM2	SCK0	DATRG	WKUP2		High drive
PA3	TWD0	NPCS3				High drive
PA4	TWCK0	TCLK0		WKUP3		
PA5	RXD0	NPCS3		WKUP4		
PA6	TXD0	PCK0				
PA7	RTS0	PWM3			XIN32	
PA8	CTS0	ADTRG		WKUP5	XOUT32	
PA9	URXD0	NPCS1		WKUP6		
PA10	UTXD0	NPCS2				
PA11	NPCS0	PWM0		WKUP7		
PA12	MISO	PWM1				
PA13	MOSI	PWM2				
PA14	SPCK	PWM3		WKUP8		
PA15		TIOA1		WKUP14		
PA16		TIOB1		WKUP15		
PA17		PCK1		AD0		
PA18		PCK2		AD1		
PA19				AD2/WKUP9		
PA20				AD3/WKUP10		
PA21	RXD1	PCK1		AD8		64/100-pin versions
PA22	TXD1	NPCS3		AD9		64/100-pin versions
PA23	SCK1	PWM0				64/100-pin versions
PA24	RTS1	PWM1				64/100-pin versions
PA25	CTS1	PWM2				64/100-pin versions
PA26		TIOA2				64/100-pin versions
PA27		TIOB2				64/100-pin versions
PA28		TCLK1				64/100-pin versions
PA29		TCLK2				64/100-pin versions
PA30		NPCS2		WKUP11		64/100-pin versions
PA31	NPCS1	PCK2				64/100-pin versions

  - Support for two PDC channels with connection to receiver and transmitter (for UART0 only)

12.4 USART

- Programmable Baud Rate Generator
- 5- to 9-bit full-duplex synchronous or asynchronous serial communications
  - 1, 1.5 or 2 stop bits in Asynchronous Mode or 1 or 2 stop bits in Synchronous Mode
  - Parity generation and error detection
  - Framing error detection, overrun error detection
  - MSB- or LSB-first
  - Optional break generation and detection
  - By 8 or by-16 over-sampling receiver frequency
  - Hardware handshaking RTS-CTS
  - Receiver time-out and transmitter timeguard
  - Optional Multi-drop Mode with address generation and detection
- RS485 with driver control signal
- ISO7816, T = 0 or T = 1 Protocols for interfacing with smart cards (Only on USART0)
  - NACK handling, error counter with repetition and iteration limit
- SPI Mode
  - Master or Slave
  - Serial Clock programmable Phase and Polarity
  - SPI Serial Clock (SCK) Frequency up to MCK/4
- IrDA modulation and demodulation (Only on USART0)
  - Communication at up to 115.2 Kbps
- Test Modes
  - Remote Loopback, Local Loopback, Automatic Echo
- PDC support (for USART0 only)

12.5 Timer Counter (TC)

- Six 16-bit Timer Counter Channels
- Wide range of functions including:
  - Frequency Measurement
  - Event Counting
  - Interval Measurement
  - Pulse Generation
  - Delay Timing
  - Pulse Width Modulation
  - Up/down Capabilities
- Each channel is user-configurable and contains:
  - Three external clock inputs
  - Five internal clock inputs

  - Two multi-purpose input/output signals
- Two global registers that act on all three TC Channels
- Quadrature decoder
  - Advanced line filtering
  - Position/revolution/speed
- 2-bit Gray Up/Down Counter for Stepper Motor

12.6 Pulse Width Modulation Controller (PWM)

- Four channels, one 16-bit counter per channel
- Common clock generator, providing thirteen different clocks
  - One Modulo n counter providing eleven clocks
  - Two independent linear dividers working on modulo n counter outputs
- Independent channel programming
  - Independent enable/disable commands
  - Independent clock selection
  - Independent period and duty cycle, with double buffering
  - Programmable selection of the output waveform polarity

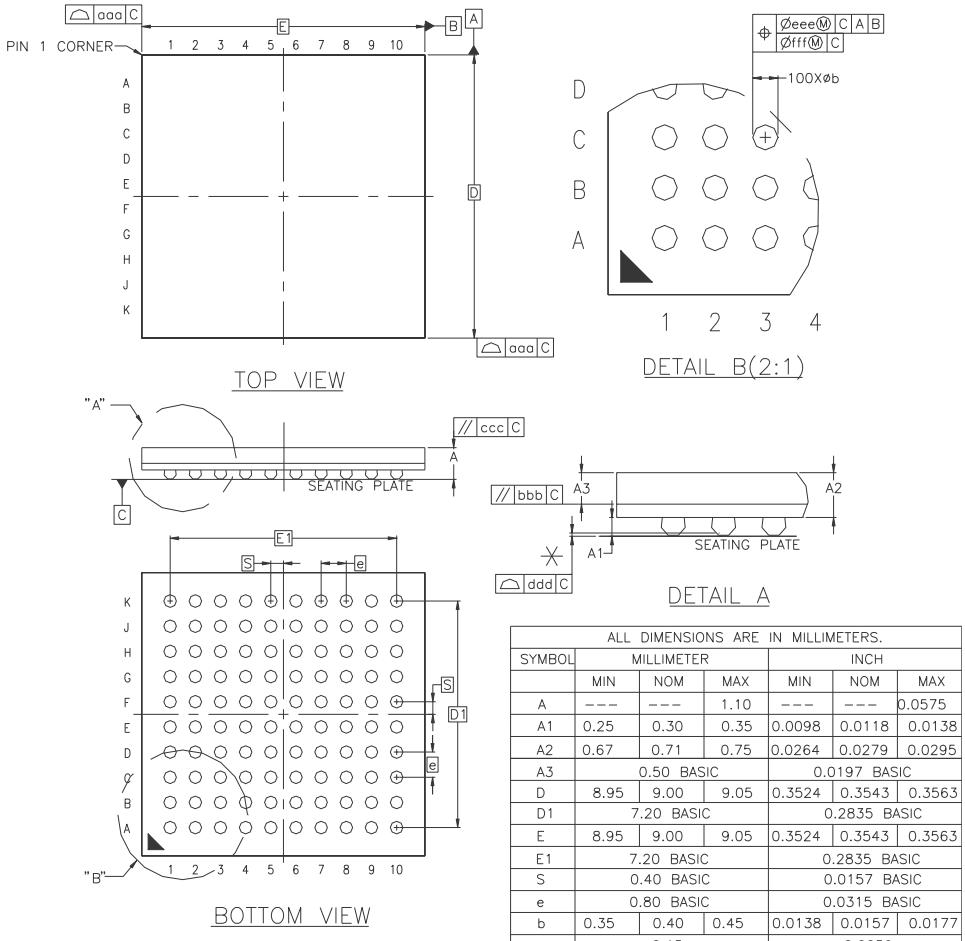
12.7 10-bit Analog-to-Digital Converter

- Up to 16-channel ADC
- 10-bit 384 Ksamples/sec. or 8-bit 583 Ksamples/sec. Successive Approximation Register ADC
- ±2 LSB Integral Non Linearity, ±1 LSB Differential Non Linearity
- Integrated 8-to-1 multiplexer, offering eight independent 3.3V analog inputs
- External voltage reference for better accuracy on low voltage inputs
- Individual enable and disable of each channel
- Multiple trigger source
  - Hardware or software trigger
  - External trigger pin
  - Timer Counter 0 to 2 outputs TIOA0 to TIOA2 trigger
- Sleep Mode and conversion sequencer
  - Automatic wakeup on trigger and back to sleep mode after conversions of all enabled channels

12.8 Digital-to-Analog Converter (DAC)

- 1 channel 10-bit DAC
- Up to 500 ksamples/s conversion rate
- Flexible conversion range
- Multiple trigger sources
- One PDC channel

Figure 13-2. 100-ball TFBGA Package Drawing

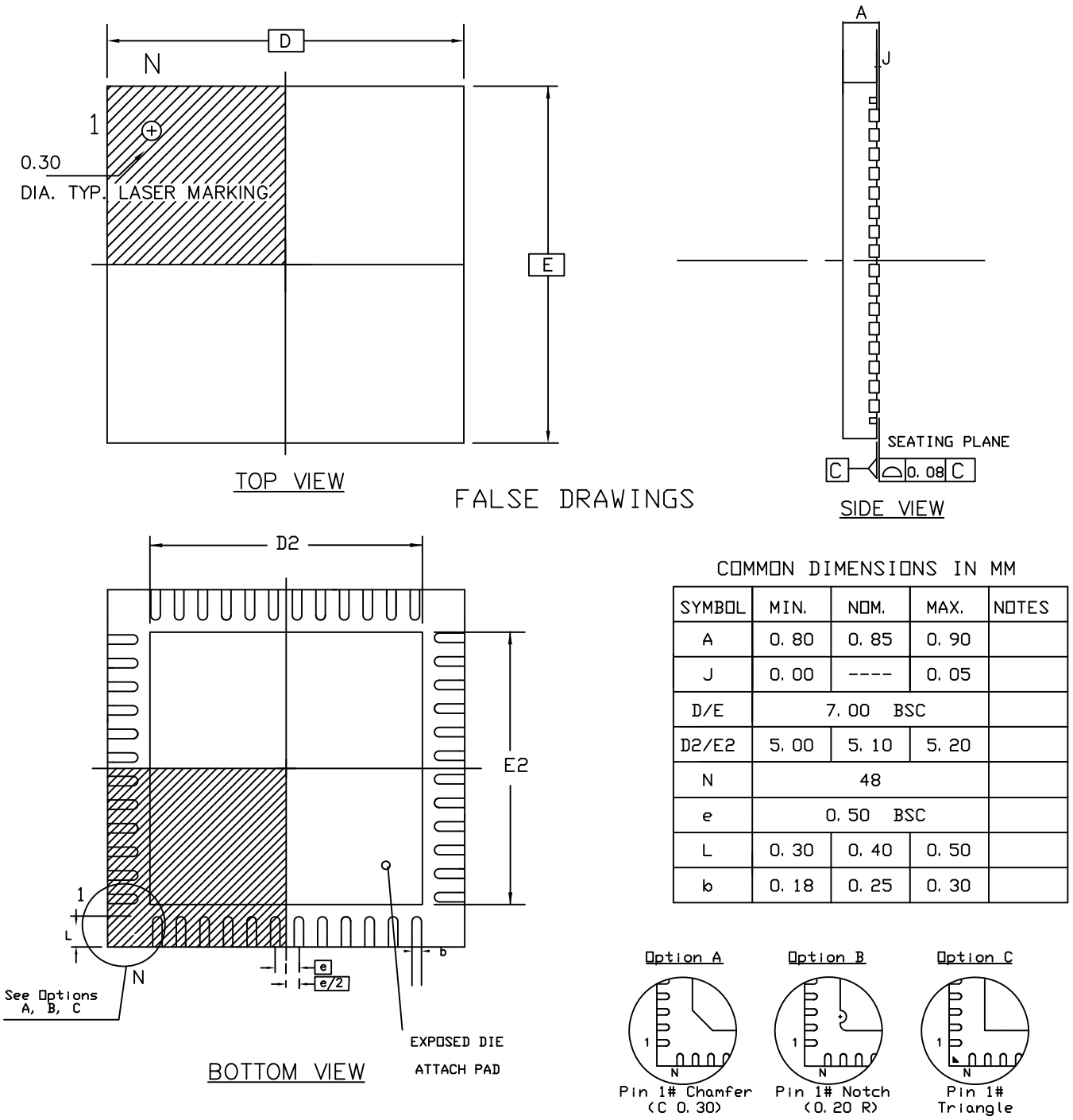


ALL DIMENSIONS ARE IN MILLIMETERS.						
SYMBOL	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.10	---	---	0.0575
A1	0.25	0.30	0.35	0.0098	0.0118	0.0138
A2	0.67	0.71	0.75	0.0264	0.0279	0.0295
A3	0.50 BASIC			0.0197 BASIC		
D	8.95	9.00	9.05	0.3524	0.3543	0.3563
D1	7.20 BASIC			0.2835 BASIC		
E	8.95	9.00	9.05	0.3524	0.3543	0.3563
E1	7.20 BASIC			0.2835 BASIC		
S	0.40 BASIC			0.0157 BASIC		
e	0.80 BASIC			0.0315 BASIC		
b	0.35	0.40	0.45	0.0138	0.0157	0.0177
aaa	0.15			0.0059		
bbb	0.20			0.0079		
ccc	0.20			0.0079		
ddd	0.12			0.0047		
eee	0.15			0.0059		
fff	0.08			0.0031		

Table 13-1. 48-lead LQFP Package Dimensions (in mm)

Symbol	Millimeter			Inch		
	Min	**Nom**	**Max**	**Min**	**Nom**	**Max**
A	–	–	1.60	–	–	0.063
A1	0.05	–	0.15	0.002	–	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	9.00 BSC			0.354 BSC		
D1	7.00 BSC			0.276 BSC		
E	9.00 BSC			0.354 BSC		
E1	7.00 BSC			0.276 BSC		
R2	0.08	–	0.20	0.003	–	0.008
R1	0.08	–	–	0.003	–	–
q	0°	3.5°	7°	0°	3.5°	7°
θ_1	0°	–	–	0°	–	–
θ_2	11°	12°	13°	11°	12°	13°
θ_3	11°	12°	13°	11°	12°	13°
c	0.09	–	0.20	0.004	–	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	–	–	0.008	–	–
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BSC.			0.020 BSC.		
D2	5.50			0.217		
E2	5.50			0.217		
Tolerances of Form and Position						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

Figure 13-4. 48-pad QFN Package Drawing



COMMON DIMENSIONS IN MM

SYMBOL	MIN.	NOM.	MAX.	NOTES
A	0.80	0.85	0.90	
J	0.00	----	0.05	
D/E	7.00 BSC			
D2/E2	5.00	5.10	5.20	
N	48			
e	0.50 BSC			
L	0.30	0.40	0.50	
b	0.18	0.25	0.30	