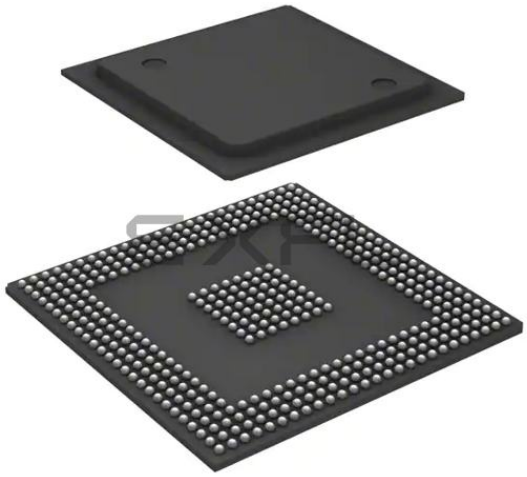

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z7
Core Size	32-Bit Dual-Core
Speed	264MHz
Connectivity	CANbus, EBI/EMI, Ethernet, FlexCANbus, LINbus, SCI, SPI
Peripherals	DMA, LVD, POR, Zipwire
Number of I/O	293
Program Memory Size	4MB (4M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 40x12b eQADCx2
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	416-BGA
Supplier Device Package	416-MAPBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5775edk3mme3

1 Introduction

1.1 Features summary

On-chip modules available within the family include the following features:

- Three dual issue, 32-bit CPU core complexes (e200z7), two of which run in lockstep
  - Power Architecture embedded specification compliance
  - Instruction set enhancement allowing variable length encoding (VLE), optional encoding of mixed 16-bit and 32-bit instructions, for code size footprint reduction
  - On the two computational cores: Signal processing extension (SPE1.1) instruction support for digital signal processing (DSP)
  - Single-precision floating point operations
  - On the two computational cores: 16 KB I-Cache and 16 KB D-Cache
  - Hardware cache coherency between cores
- 16 hardware semaphores
- 3-channel CRC module
- 4 MB on-chip flash memory
  - Supports read during program and erase operations, and multiple blocks allowing EEPROM emulation
- 512 KB on-chip general-purpose SRAM including 64 KB standby RAM
- Two multichannel direct memory access controllers (eDMA)
  - 64 channels per eDMA
- Dual core Interrupt Controller (INTC)
- Dual phase-locked loops (PLLs) with stable clock domain for peripherals and frequency modulation (FM) domain for computational shell
- Crossbar Switch architecture for concurrent access to peripherals, flash memory, or RAM from multiple bus masters with End-To-End ECC
- System Integration Unit (SIU)
- Error Injection Module (EIM) and Error Reporting Module (ERM)
- Four protected port output (PPO) pins
- Boot Assist Module (BAM) supports serial bootload via CAN or SCI
- Up to three second-generation Enhanced Time Processor Units (eTPUs)
  - 32 channels per eTPU
  - Total of 36 KB code RAM
  - Total of 9 KB parameter RAM

Table 3. Device operating conditions (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
V_{RL_SD}	SDADC ground reference voltage	—	V_{SSA_SD}			V
V_{DDA_SD}	SDADC supply voltage[15]	—	4.5	—	5.5	V
$V_{DDA\_EQA/B}$	eQADC supply voltage	—	4.75	—	5.25	V
V_{RH_SD}	SDADC reference	—	4.5	V_{DDA_SD}	5.5	V
$V_{DDA\_SD} - V_{RH\_SD}$	SDADC reference differential voltage	—	—	—	25	mV
$V_{SSA\_SD} - V_{RL\_SD}$	V_{RL_SD} differential voltage	—	–25	—	25	mV
V_{RH_EQ}	eQADC reference	—	4.75	—	5.25	V
$V_{DDA\_EQA/B} - V_{RH\_EQ}$	eQADC reference differential voltage	—	—	—	25	mV
$V_{SSA\_EQ} - V_{RL\_EQ}$	V_{RL_EQ} differential voltage	—	–25	—	25	mV
$V_{SSA\_EQ} - V_{SS}$	V_{SSA_EQ} differential voltage	—	–25	—	25	mV
$V_{SSA\_SD} - V_{SS}$	V_{SSA_SD} differential voltage	—	–25	—	25	mV
V_{RAMP}	Slew rate on power supply pins	—	—	—	100	V/ms
Current						
I_{IC}	DC injection current (per pin)[16, 17, 18]	Digital pins and analog pins	–3.0	—	3.0	mA
I_{MAXSEG}	Maximum current per power segment[19, 20]	—	–80	—	80	mA

1. Maximum operating frequency is applicable to the computational cores and platform for the device. See the Clocking chapter in the MPC5775E Microcontroller Reference Manual for more information on the clock limitations for the various IP blocks on the device.
2. If frequency modulation (FM) is enabled, the maximum frequency still cannot exceed this value.
3. MPC5775B Max value is 220 MHz.
4. MPC5775B Max value is 110 MHz
5. The maximum specification for operating junction temperature T_J must be respected. Thermal characteristics provides details.
6. Core voltage as measured on device pin to guarantee published silicon performance
7. During power ramp, voltage measured on silicon might be lower. Maximum performance is not guaranteed, but correct silicon operation is guaranteed. See power management and reset management for description.
8. Maximum core voltage is not permitted for entire product life. See absolute maximum rating.
9. When internal LVD/HVDs are disabled, external monitoring is required to guarantee device operation. Failure to monitor externally supply voltage may result in erroneous operation of the device.
10. This LVD/HVD disabled supply voltage condition only applies after LVD/HVD are disabled by the application during the reset sequence, and the LVD/HVD are active until that point.
11. This spec does not apply to V_{DDEH1}.
12. When internal flash memory regulator is used:
    - Flash memory read operation is supported for a minimum V_{DDPMC} value of 3.15 V.
    - Flash memory read, program, and erase operations are supported for a minimum V_{DDPMC} value of 3.5 V.

    When flash memory power is supplied externally (V_{DDPMC} shorted to V_{DDFLA}): The V_{DDPMC} range must be within the limits specified for LVD_FLASH and HVD_FLASH monitoring. Table 26 provides the monitored LVD_FLASH and HVD_FLASH limits.
13. If the standby RAM regulator is not used, the V_{STBY} supply input pin must be tied to ground.
14. V_{STBY_BO} is the maximum voltage that sets the standby RAM brownout flag in the device logic. The minimum voltage for RAM data retention is guaranteed always to be less than the V_{STBY_BO} maximum value.

15. For supply voltages between 3.0 V and 4.0 V there will be no guaranteed precision of ADC (accuracy/linearity). ADC will recover to a fully functional state when the voltage rises above 4.0 V.
16. Full device lifetime without performance degradation
17. I/O and analog input specifications are only valid if the injection current on adjacent pins is within these limits. See the absolute maximum ratings table for maximum input current for reliability requirements.
18. The I/O pins on the device are clamped to the I/O supply rails for ESD protection. When the voltage of the input pin is above the supply rail, current will be injected through the clamp diode to the supply rail. For external RC network calculation, assume a typical 0.3 V drop across the active diode. The diode voltage drop varies with temperature.
19. The sum of all controller pins (including both digital and analog) must not exceed 200 mA. A V_{DDEx}/V_{DDEHx} power segment is defined as one or more GPIO pins located between two V_{DDEx}/V_{DDEHx} supply pins.
20. The average current values given in I/O pad current specifications should be used to calculate total I/O segment current.

3.5 DC electrical specifications

NOTE

I_{DDA_MISC} is the sum of current consumption of IRC, I_{TRNG}, and I_{STBY} in the 5 V domain. IRC current is provided in the IRC specifications.

NOTE

I/O, XOSC, EQADC, SDADC, and Temperature Sensor current specifications are in those components' dedicated sections.

Table 4. DC electrical specifications

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
I_{DD}	Operating current on the V_{DD} core logic supply[1]	LVD/HVD enabled, V_{DD} = 1.2 V to 1.32 V	—	0.65	1.35	A
		LVD/HVD disabled, V_{DD} = 1.2 V to 1.38 V	—	0.65	1.4	
I_{DD_PE}	Operating current on the V_{DD} supply for flash memory program/erase	—	—	—	85	mA
I_{DDPMC}	Operating current on the V_{DDPMC} supply[2]	Flash memory read	—	—	40	mA
		Flash memory program/erase	—	—	70	
		PMC only	—	—	35	
	Operating current on the V_{DDPMC} supply (internal core regulator bypassed)	Flash memory read	—	—	10	mA
		Flash memory program/erase	—	—	40	
		PMC only	—	—	5	
I_{REGCTL}	Core regulator DC current output on V_{REGCTL} pin	—	—	—	25	mA
I_{STBY}	Standby RAM supply current (T_J = 150°C)	1.08 V	—	—	1140	µA
		1.25 V to 5.5 V	—	—	1170	
I_{DD_PWR}	Operating current on the V_{DDPWR} supply	—	—	—	50	mA
I_{BG_REF}	Bandgap reference current consumption[3]		—	—	600	µA
I_{TRNG}	True Random Number Generator current	—	—	—	2.1	mA

Table 7. I/O pullup/pulldown DC electrical characteristics

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
I_{WPU}	Weak pullup current	V_{IN} = 0.35 * V_{DDEx} 4.5 V < V_{DDEx} < 5.5 V	40	—	120	µA
		V_{IN} = 0.35 * V_{DDEx} 3.0 V < V_{DDEx} < 3.6 V	25	—	80	
I_{WPD}	Weak pulldown current	V_{IN} = 0.65 * V_{DDEx} 4.5 V < V_{DDEx} < 5.5 V	40	—	120	µA
		V_{IN} = 0.65 * V_{DDEx} 3.0 V < V_{DDEx} < 3.6 V	25	—	80	

The specifications in Table 8 apply to the pins ANA0_SDA0 to ANA7, ANA16_SDB0 to ANA23_SDC3, and ANB0_SDD0 to ANB7_SDD7.

Table 8. I/O pullup/pulldown resistance electrical characteristics

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
R_{PUPD}	Analog input bias / diagnostic pullup/ pulldown resistance	200 kΩ	130	200	280	kΩ
		100 kΩ	65	100	140	
		5 kΩ	1.4	5	7.5	
Δ_{PUPD}	R_{PUPD} pullup/pulldown resistance mismatch	—	—	—	5	%

3.6.2 Output pad specifications

Figure 4 shows output DC electrical characteristics.

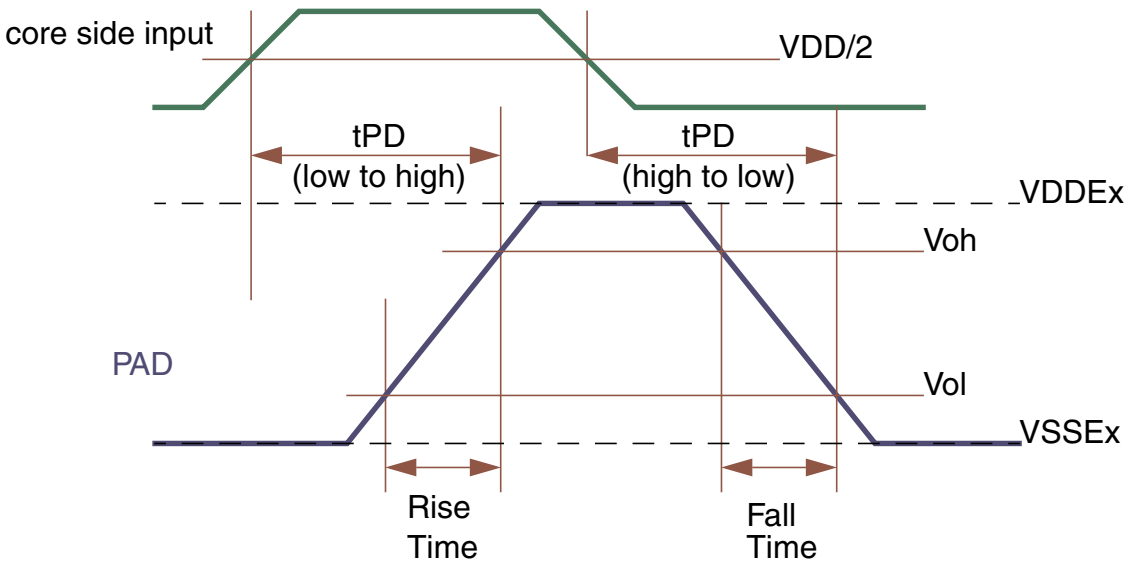

Figure 4. I/O output DC electrical characteristics definition

The following tables specify output DC electrical characteristics.

Table 9. GPIO data pad output buffer electrical characteristics (SR pads)[1]

Symbol	Parameter	Conditions[2]		Value[3]			Unit
				Min	Typ	Max	
I_{OH}	GPIO pad output high current	V_{OH} = 0.8 * V_{DDEx}	PCR[SRC] = 11b or 01b	25	—	—	mA
		4.5 V < V_{DDEx} < 5.5 V	PCR[SRC] = 10b or 00b	15	—	—	
		V_{OH} = 0.8 * V_{DDEx}	PCR[SRC] = 11b or 01b	13	—	—	
		3.0 V < V_{DDEx} < 3.6 V	PCR[SRC] = 10b or 00b	8	—	—	
I_{OL}	GPIO pad output low current	V_{OL} = 0.2 * V_{DDEx}	PCR[SRC] = 11b or 01b	48	—	—	mA
		4.5 V < V_{DDEx} < 5.5 V	PCR[SRC] = 10b or 00b	22	—	—	
		V_{OL} = 0.2 * V_{DDEx}	PCR[SRC] = 11b or 01b	17	—	—	
		3.0 V < V_{DDEx} < 3.6 V	PCR[SRC] = 10b or 00b	10.5	—	—	

Table continues on the next page...

Table 9. GPIO data pad output buffer electrical characteristics (SR pads)[1] (continued)

Symbol	Parameter	Conditions[2]		Value[3]			Unit
				Min	Typ	Max	
t_{R_F}	GPIO pad output transition time (rise/fall)	PCR[SRC] = 11b	C_L = 25 pF	—	—	1.2	ns
		4.5 V < V_{DDEx} < 5.5 V	C_L = 50 pF	—	—	2.5	
			C_L = 200 pF	—	—	8	
		PCR[SRC] = 11b	C_L = 25 pF	—	—	1.7	
		3.0 V < V_{DDEx} < 3.6 V	C_L = 50 pF	—	—	3.25	
			C_L = 200 pF	—	—	12	
		PCR[SRC] = 10b	C_L = 50 pF	—	—	5	
		4.5 V < V_{DDEx} < 5.5 V	C_L = 200 pF	—	—	18	
		PCR[SRC] = 10b	C_L = 50 pF	—	—	7	
		3.0 V < V_{DDEx} < 3.6 V	C_L = 200 pF	—	—	25	
		PCR[SRC] = 01b	C_L = 50 pF	—	—	13	
		4.5 V < V_{DDEx} < 5.5 V	C_L = 200 pF	—	—	24	
		PCR[SRC] = 01b	C_L = 50 pF	—	—	25	
		3.0 V < V_{DDEx} < 3.6 V	C_L = 200 pF	—	—	30	
		PCR[SRC] = 00b	C_L = 50 pF	—	—	24	
		4.5 V < V_{DDEx} < 5.5 V	C_L = 200 pF	—	—	50	
		PCR[SRC] = 00b	C_L = 50 pF	—	—	40	
		3.0 V < V_{DDEx} < 3.6 V	C_L = 200 pF	—	—	51	
t_{PD}	GPIO pad output propagation delay time	PCR[SRC] = 11b	C_L = 50 pF	—	—	6	ns
		4.5 V < V_{DDEx} < 5.5 V	C_L = 200 pF	—	—	13	
		PCR[SRC] = 11b	C_L = 50 pF	—	—	8.25	
		3.0 V < V_{DDEx} < 3.6 V	C_L = 200 pF	—	—	19.5	
		PCR[SRC] = 10b	C_L = 50 pF	—	—	9	
		4.5 V < V_{DDEx} < 5.5 V	C_L = 200 pF	—	—	22	
		PCR[SRC] = 10b	C_L = 50 pF	—	—	12.5	
		3.0 V < V_{DDEx} < 3.6 V	C_L = 200 pF	—	—	35	
		PCR[SRC] = 01b	C_L = 50 pF	—	—	27	
		4.5 V < V_{DDEx} < 5.5 V	C_L = 200 pF	—	—	40	
		PCR[SRC] = 01b	C_L = 50 pF	—	—	45	
		3.0 V < V_{DDEx} < 3.6 V	C_L = 200 pF	—	—	65	
		PCR[SRC] = 00b	C_L = 50 pF	—	—	40	
		4.5 V < V_{DDEx} < 5.5 V	C_L = 200 pF	—	—	65	
		PCR[SRC] = 00b	C_L = 50 pF	—	—	75	
		3.0 V < V_{DDEx} < 3.6 V	C_L = 200 pF	—	—	100	
$\lvert t_{SKEW\_W} \rvert$	Difference between rise and fall time	—		—	—	25	%

1. All GPIO pad output specifications are valid for 3.0 V < V_{DDEx} < 5.5 V, except where explicitly stated.
2. PCR[SRC] values refer to the setting of that register field in the SIU.
3. All values to be confirmed during device validation.

Table 12. PLL1 electrical characteristics (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
Δ_{PLL1IN}	PLL1 input clock duty cycle[1]	—	35	—	65	%
$f_{PLL1VCO}$	PLL1 VCO frequency	—	600	—	1250	MHz
$f_{PLL1PHI}$	PLL1 output clock PHI	—	4.762	—	264[2]	MHz
$t_{PLL1LOCK}$	PLL1 lock time	—	—	—	100	µs
$\lvert\Delta_{PLL1PHISPJ}\rvert$	PLL1_PHI single period peak-to-peak jitter	$f_{PLL1PHI}$ = 200 MHz, 6-sigma	—	—	500[3]	ps
$f_{PLL1MOD}$	PLL1 modulation frequency	—	—	—	250	kHz
$\lvert\delta_{PLL1MOD}\rvert$	PLL1 modulation depth (when enabled)	Center spread	0.25	—	2	%
		Down spread	0.5	—	4	%
I_{PLL1}	PLL1 consumption	FINE LOCK state	—	—	6	mA

1. PLL1IN clock retrieved directly from either internal PLL0 or external XOSC clock. Input characteristics are granted when using internal PLL0 or external oscillator in functional mode.
2. MPC5775B Max value is 220MHz.
3. Noise on the V_{DD} supply with frequency content below 40 kHz and above 50 MHz is filtered by the PLL. Noise on the V_{DD} supply with frequency content in the range of 40 kHz – 50 MHz must be filtered externally to the device.

3.7.2 Oscillator electrical specifications

NOTE

All oscillator specifications in Table 13 are valid for V_{DDEH6} = 3.0 V to 5.5 V.

Table 13. External oscillator (XOSC) electrical specifications

Symbol	Parameter	Conditions	Value		Unit
			Min	Max	
f_{XTAL}	Crystal frequency range	—	8	40	MHz
t_{cst}	Crystal start-up time[1, 2]	T_J = 150 °C	—	5	ms
t_{rec}	Crystal recovery time[3]	—	—	0.5	ms
V_{IHEXT}	EXTAL input high voltage (external reference)	V_{REF} = 0.28 * V_{DDEH6}	V_{REF} + 0.6	—	V
V_{ILEXT}	EXTAL input low voltage (external reference)	V_{REF} = 0.28 * V_{DDEH6}	—	V_{REF} – 0.6	V
C_{S_EXTAL}	Total on-chip stray capacitance on EXTAL pin[4]	416-ball MAPBGA	2.3	3.0	pF
C_{S_XTAL}	Total on-chip stray capacitance on XTAL pin[4]	416-ball MAPBGA	2.3	3.0	pF
g_m	Oscillator transconductance[5]	Low	3	10	mA/V
		Medium	10	27	
		High	12	35	
V_{EXTAL}	Oscillation amplitude on the EXTAL pin after startup[6]	—	0.5	1.6	V
V_{HYS}	Comparator hysteresis	—	0.1	1.0	V
I_{XTAL}	XTAL current[6, 7]	—	—	14	mA

11. All channels have same 10 kΩ < Rs < 100 kΩ Channel under test has Rs = 10 kΩ, I_{INJ}=I_{INJMAX},I_{INJMIN}.
12. The TUE specification is always less than the sum of the INL, DNL, offset, and gain errors due to cancelling errors.
13. TUE does not apply to differential conversions.
14. Variable gain is controlled by setting the PRE_GAIN bits in the ADC_ACR1-8 registers to select a gain factor of ×1, ×2, or ×4. Settings are for differential input only. Tested at ×1 gain. Values for other settings are guaranteed as indicated.
15. Guaranteed 10-bit monotonicity.
16. At $V_{RH\_EQ} - V_{RL\_EQ}$ = 5.12 V, one LSB = 1.25 mV.

3.8.2 Sigma-Delta ADC (SDADC)

The SDADC is a 16-bit Sigma-Delta analog-to-digital converter with a 333 Ksps maximum output conversion rate.

NOTE

The voltage range is 4.5 V to 5.5 V for SDADC specifications, except where noted otherwise.

Table 17. SDADC electrical specifications

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
V_{IN}	ADC input signal	—	0	—	V_{DDA_SD}	V
V_{IN_PK2PK}[1]	Input range peak to peak $V_{IN\_PK2PK} = V_{INP}$[2] – V_{INM},[3]	Single ended $V_{INM} = V_{RL\_SD}$	V_{RH_SD}/GAIN			V
		Single ended $V_{INM} = 0.5*V_{RH\_SD}$ GAIN = 1	±0.5*V_{RH_SD}			
		Single ended $V_{INM} = 0.5*V_{RH\_SD}$ GAIN = 2,4,8,16	±V_{RH_SD}/GAIN			
		Differential $0 < V_{IN} < V_{DDEx}$	±V_{RH_SD}/GAIN			
f_{ADCD_M}	SD clock frequency[4]	—	4	14.4	16	MHz
f_{ADCD_S}	Conversion rate	—	—	—	333	Ksps
—	Oversampling ratio	Internal modulator	24	—	256	—
RESOLUTION	SD register resolution[5]	2's complement notation	16			bit
GAIN	ADC gain	Defined through SDADC_MCR[PGAN]. Only integer powers of 2 are valid gain values.	1	—	16	—

Table continues on the next page...

Table 17. SDADC electrical specifications (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
$SINAD_{DIFF150}$	Signal to noise and distortion ratio in differential mode, 150 Ksps output rate	Gain = 1 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	72	—	—	dBFS
		Gain = 2 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	72	—	—	
		Gain = 4 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	69	—	—	
		Gain = 8 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	68.8	—	—	
		Gain = 16 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	64.8	—	—	
$SINAD_{DIFF333}$	Signal to noise and distortion ratio in differential mode, 333 Ksps output rate	Gain = 1 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	66	—	—	dBFS
		Gain = 2 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	66	—	—	
		Gain = 4 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	63	—	—	
		Gain = 8 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	62	—	—	
		Gain = 16 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	59	—	—	

Table continues on the next page...

Table 17. SDADC electrical specifications (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
$THD_{DIFF333}$	Total harmonic distortion in differential mode, 333 Ksps output rate	Gain = 1 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	65	—	—	dBFS
		Gain = 2 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	68	—	—	
		Gain = 4 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	74	—	—	
		Gain = 8 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	80	—	—	
		Gain = 16 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	80	—	—	
THD_{SE150}	Total harmonic distortion in single-ended mode, 150 Ksps output rate	Gain = 1 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	68	—	—	dBFS
		Gain = 2 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	68	—	—	
		Gain = 4 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	66	—	—	
		Gain = 8 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	68	—	—	
		Gain = 16 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	68	—	—	
SFDR	Spurious free dynamic range	Any GAIN	60	—	—	dB
Z_{DIFF}	Differential input impedance[10, 11]	GAIN = 1	1000	1250	1500	kΩ
		GAIN = 2	600	800	1000	
		GAIN = 4	300	400	500	
		GAIN = 8	200	250	300	
		GAIN = 16	200	250	300	

Table continues on the next page...

Table 17. SDADC electrical specifications (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
δ_{GROUP}	Group delay	Within pass band: Tclk is f_{ADCD_M} / 2	—	—	—	—
		OSR = 24	—	—	235.5	Tclk
		OSR = 28	—	—	275	
		OSR = 32	—	—	314.5	
		OSR = 36	—	—	354	
		OSR = 40	—	—	393.5	
		OSR = 44	—	—	433	
		OSR = 48	—	—	472.5	
		OSR = 56	—	—	551.5	
		OSR = 64	—	—	630.5	
		OSR = 72	—	—	709.5	
		OSR = 75	—	—	696	
		OSR = 80	—	—	788.5	
		OSR = 88	—	—	867.5	
		OSR = 96	—	—	946.5	
		OSR = 112	—	—	1104.5	
		OSR = 128	—	—	1262.5	
		OSR = 144	—	—	1420.5	
		OSR = 160	—	—	1578.5	
		OSR = 176	—	—	1736.5	
		OSR = 192	—	—	1894.5	
		OSR = 224	—	—	2210.5	
		OSR = 256	—	—	2526.5	
		Distortion within pass band	–0.5/ f_{ADCD_S}	—	+0.5/ f_{ADCD_S}	—
f_{HIGH}	High pass filter 3 dB frequency	Enabled	—	10e–5* fADCD_S	—	—
$t_{STARTUP}$	Startup time from power down state	—	—	—	100	µs
$t_{LATENCY}$	Latency between input data and converted data when input mux does not change[15]	HPF = ON	—	—	δ_{GROUP} + f_{ADCD_S}	—
		HPF = OFF	—	—	δ_{GROUP}	
$t_{SETTLING}$	Settling time after mux change	Analog inputs are muxed HPF = ON	—	—	$2*\delta_{GROUP}$ + $3*f_{ADCD\_S}$	—
		HPF = OFF	—	—	$2*\delta_{GROUP}$ + $2*f_{ADCD\_S}$	
$t_{ODRECOVERY}$	Overdrive recovery time	After input comes within range from saturation HPF = ON	—	—	$2*\delta_{GROUP}$ + f_{ADCD_S}	—
		HPF = OFF	—	—	$2*\delta_{GROUP}$	

Table continues on the next page...

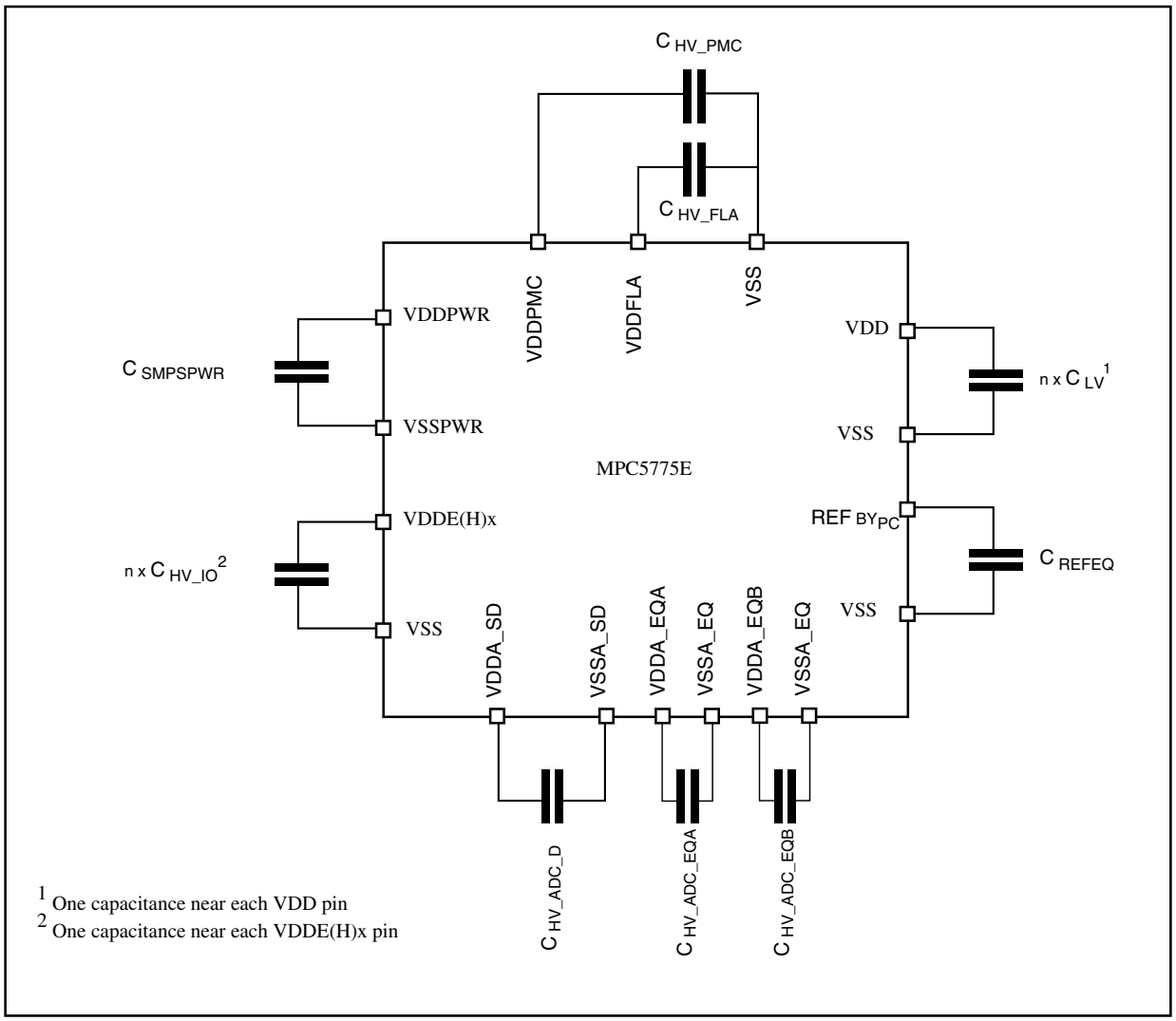

Figure 13. Recommended supply pin circuits

The following table describes the supply stability capacitances required on the device for proper operation.

Table 25. Device power supply integration

Symbol	Parameter	Conditions	Value[1]			Unit
			Min	Typ	Max	
C_{LV}	Minimum V_{DD} external bulk capacitance[2, 3]	LDO mode	4.7	—	—	µF
		SMPS mode	22	—	—	µF
$C_{SMPSPWR}$	Minimum SMPS driver supply capacitance	—	22	—	—	µF
C_{HV_PMC}	Minimum V_{DDPMC} external bulk capacitance[4, 5]	LDO mode	22	—	—	µF
		SMPS mode	22	—	—	µF
C_{HV_IO}	Minimum V_{DDEx}/V_{DDEHx} external capacitance[2]	—	—	4.7[6]	—	µF
C_{HV_FLA}	Minimum V_{DD_FLA} external capacitance[7]	—	1.0	2.0	—	µF
$C_{HV\_ADC\_EQA/B}$	Minimum $V_{DDA\_EQA/B}$ external capacitance[8]	—	0.01	—	—	µF

Table continues on the next page...

NOTE

In these descriptions, *star route layout* means a track split as close as possible to the power supply source. Each of the split tracks is routed individually to the intended end connection.

1. For both LDO mode and SMPS mode, V_{DDPMC} and V_{DDPWR} must be connected together (shorted) to ensure aligned voltage ramping up/down. In addition:
   - For SMPS mode, a star route layout of the power track is required to minimize mutual noise. If SMPS mode is not used, the star route layout is not required. V_{DDPWR} is the supply pin for the SMPS circuitry.
   - For 3.3 V operation, V_{DDFLA} must also be star routed and shorted to V_{DDPWR} and V_{DDPMC}. This triple connection is required because 3.3 V does not guarantee correct functionality of the internal V_{DDFLA} regulator. Consequently, V_{DDFLA} is supplied externally.
2. V_{DDA_MISC}: IRC operation is required to provide the clock for chip startup.
   - The V_{DDPMC}, V_{DD}, and V_{DDEH1} (reset pin pad segment) supplies are monitored. They hold IRC until all of them reach operational voltage. In other words, V_{DDA_MISC} must reach its specified minimum operating voltage before or at the same time that all of these monitored voltages reach their respective specified minimum voltages.
   - An alternative is to connect the same supply voltage to both V_{DDEH1} and V_{DDA_MISC}. This alternative approach requires a star route layout to minimize mutual noise.
3. Multiple V_{DDEx} supplies can be powered up in any order.

   During any time when V_{DD} is powered up but V_{DDEx} is not yet powered up: pad outputs are unpowered.

   During any time when V_{DDEx} is powered up before all other supplies: all pad output buffers are tristated.
4. Ramp up V_{DDA_EQ} before V_{DD}. Otherwise, a reset might occur.
5. When the device is powering down while using the internal SMPS regulator, V_{DDPMC} and V_{DDPWR} supplies must ramp down through the voltage range from 2.5 V to 1.5 V in less than 1 second. Slower ramp-down times might result in reduced lifetime reliability of the device.

3.12 Flash memory specifications

3.12.1 Flash memory program and erase specifications

NOTE

All timing, voltage, and current numbers specified in this section are defined for a single embedded flash memory within an SoC, and represent average currents for given supplies and operations.

Table 27 shows the estimated Program/Erase times.

Table 27. Flash memory program and erase specifications

Symbol	Characteristic[1]	Typ[2]	Factory Programming[3, 4]		Field Update			Unit
			Initial Max	Initial Max, Full Temp	Typical End of Life[5]	Lifetime Max[6]		
			20°C ≤T_A ≤30°C	-40°C ≤T_J ≤150°C	-40°C ≤T_J ≤150°C	≤ 1,000 cycles	≤ 250,000 cycles	
t_{dwpgm}	Doubleword (64 bits) program time	43	100	150	55	500		µs
t_{ppgm}	Page (256 bits) program time	73	200	300	108	500		µs
t_{qppgm}	Quad-page (1024 bits) program time	268	800	1,200	396	2,000		µs
t_{16kers}	16 KB Block erase time	168	290	320	250	1,000		ms
t_{16kpgm}	16 KB Block program time	34	45	50	40	1,000		ms
t_{32kers}	32 KB Block erase time	217	360	390	310	1,200		ms
t_{32kpgm}	32 KB Block program time	69	100	110	90	1,200		ms
t_{64kers}	64 KB Block erase time	315	490	590	420	1,600		ms
t_{64kpgm}	64 KB Block program time	138	180	210	170	1,600		ms
$t_{256kers}$	256 KB Block erase time	884	1,520	2,030	1,080	4,000	—	ms
$t_{256kpgm}$	256 KB Block program time	552	720	880	650	4,000	—	ms

1. Program times are actual hardware programming times and do not include software overhead. Block program times assume quad-page programming.
2. Typical program and erase times represent the median performance and assume nominal supply values and operation at 25 °C. Typical program and erase times may be used for throughput calculations.
3. Conditions: ≤ 150 cycles, nominal voltage.
4. Plant Programing times provide guidance for timeout limits used in the factory.
5. Typical End of Life program and erase times represent the median performance and assume nominal supply values. Typical End of Life program and erase values may be used for throughput calculations.
6. Conditions: -40°C ≤ T_J ≤ 150°C, full spec voltage.

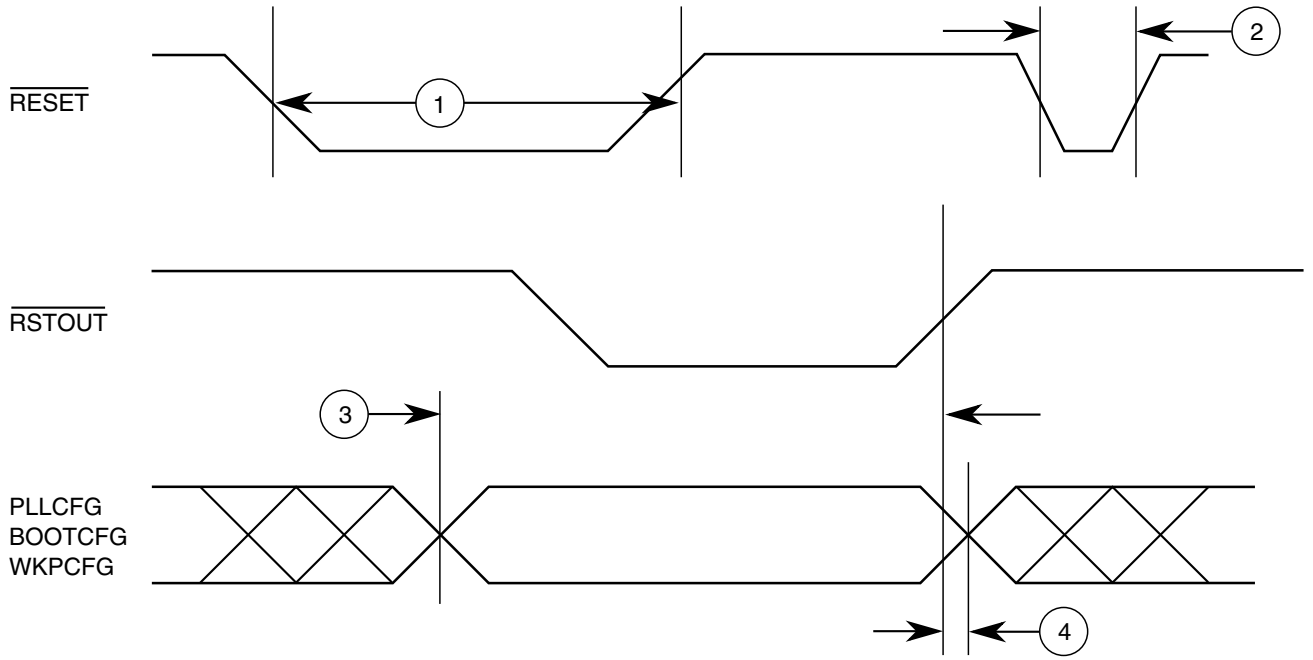

Figure 17. Reset and configuration pin timing

3.13.3 IEEE 1149.1 interface timing

Table 33. JTAG pin AC electrical characteristics[1]

#	Symbol	Characteristic	Value		Unit
			Min	Max	
1	t_{JCYC}	TCK cycle time	100	—	ns
2	t_{JDC}	TCK clock pulse width	40	60	%
3	$t_{TCKRISE}$	TCK rise and fall times (40%–70%)	—	3	ns
4	t_{TMSS}, t_{TDIS}	TMS, TDI data setup time	5	—	ns
5	t_{TMSH}, t_{TDIH}	TMS, TDI data hold time	5	—	ns
6	t_{TDOV}	TCK low to TDO data valid	—	16[2]	ns
7	t_{TDOI}	TCK low to TDO data invalid	0	—	ns
8	t_{TDOHZ}	TCK low to TDO high impedance	—	15	ns
9	t_{JCMPPW}	JCOMP assertion time	100	—	ns
10	t_{JCMPS}	JCOMP setup time to TCK low	40	—	ns
11	t_{BSDV}	TCK falling edge to output valid	—	600[3]	ns
12	t_{BSDVZ}	TCK falling edge to output valid out of high impedance	—	600	ns
13	t_{BSDHZ}	TCK falling edge to output high impedance	—	600	ns
14	t_{BSDST}	Boundary scan input valid to TCK rising edge	15	—	ns
15	t_{BSDHT}	TCK rising edge to boundary scan input invalid	15	—	ns

1. These specifications apply to JTAG boundary scan only. See Table 34 for functional specifications.
2. Timing includes TCK pad delay, clock tree delay, logic delay and TDO output pad delay.
3. Applies to all pins, limited by pad slew rate. Refer to I/O delay and transition specification and add 20 ns for JTAG delay.

Table 34. Nexus debug port timing[1] (continued)

Spec	Characteristic	Symbol	Min	Max	Unit
8	Absolute minimum TCK cycle time[4] (TDO sampled on posedge of TCK)	t_{TCYC}	40[5]	—	ns
	Absolute minimum TCK cycle time[4] (TDO sampled on negedge of TCK)		20[5]	—	
9	TCK Duty Cycle	t_{TDC}	40	60	%
10	TDI, TMS Data Setup Time[6]	t_{NTDIS}, t_{NTMSS}	8	—	ns
11	TDI, TMS Data Hold Time[6]	T_{NTDIH}, t_{NTMSH}	5	—	ns
12	TCK Low to TDO Data Valid[6]	t_{NTDOV}	0	18	ns
13	$\overline{RDY}$ Valid to MCKO[7]	—	—	—	—
14	TDO hold time after TCLK low[6]	t_{NTDOH}	1	—	ns

1. All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal. Nexus timing specified at V_{DD} = 1.08 V to 1.32 V, V_{DDE} = 3.0 V to 3.6 V, V_{DD33} and V_{DDSYN} = 3.0 V to 3.6 V, $T_A = T_L$ to T_H, and C_L = 30 pF with DSC = 0b10.
2. MDO, $\overline{MSEO}$, and $\overline{EVTO}$ data is held valid until next MCKO low cycle.
3. This is a functionally allowable feature. However, it may be limited by the maximum frequency specified by the absolute minimum TCK period specification.
4. This value is TDO propagation time plus 2 ns setup time to sampling edge.
5. This may require a maximum clock speed that is less than the maximum functional capability of the design depending on the actual system frequency being used.
6. Applies to TMS pin timing for the bit frame when using the 1149.7 advanced protocol.
7. The $\overline{RDY}$ pin timing is asynchronous to MCKO. The timing is guaranteed by design to function correctly.

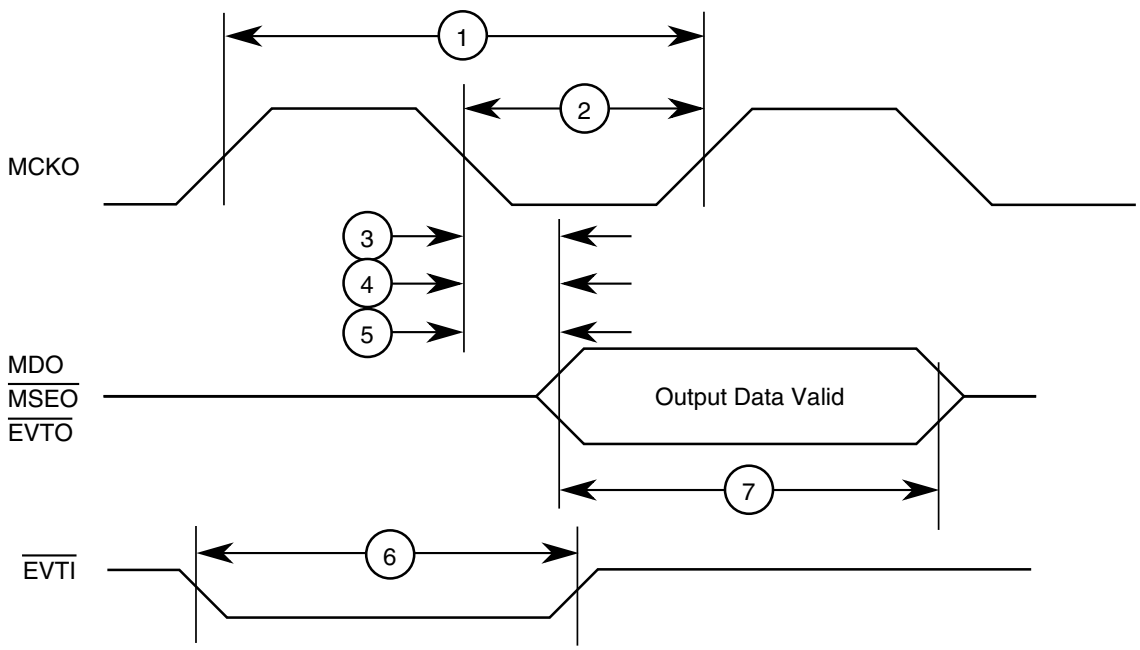

Figure 22. Nexus timings

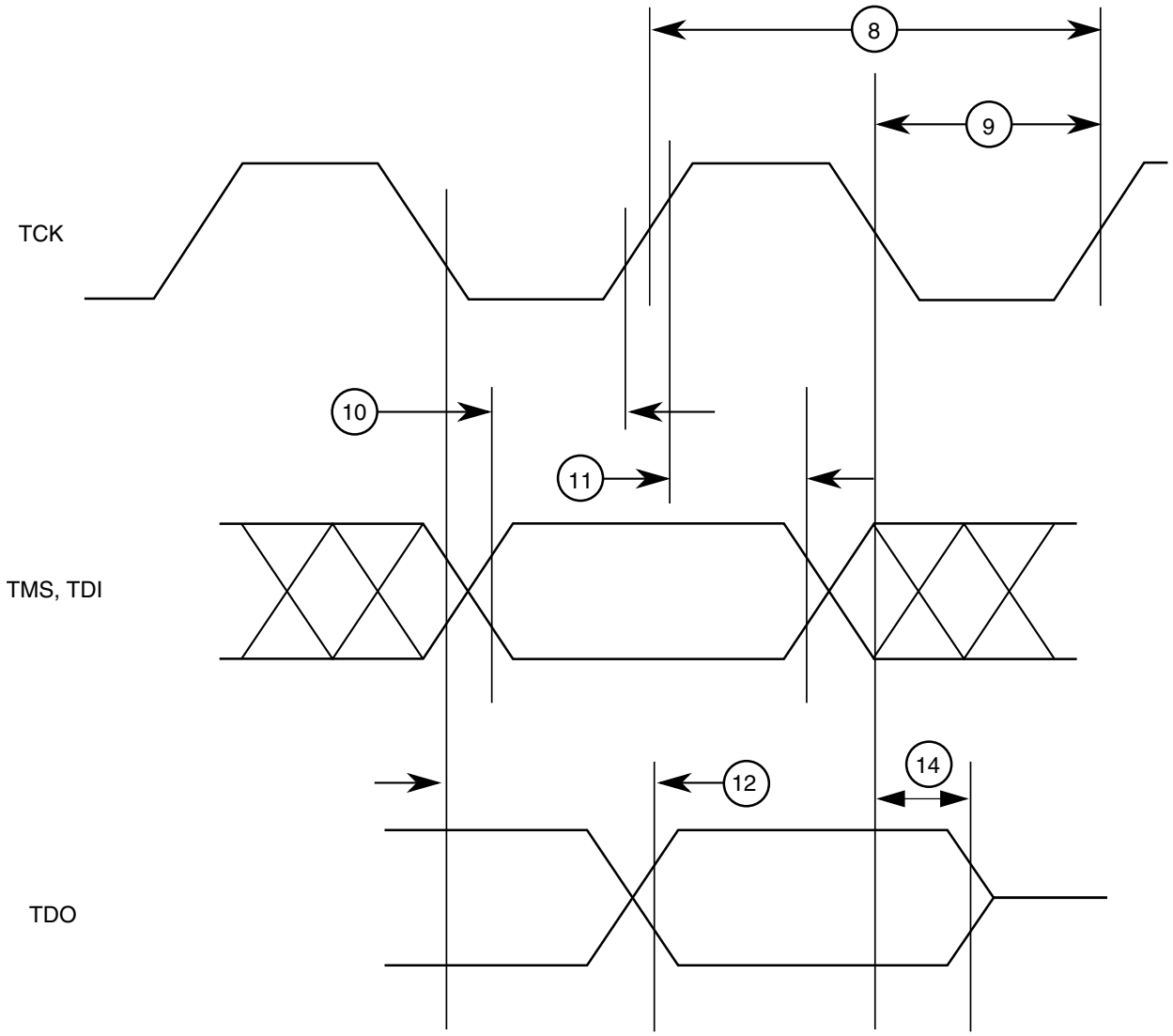

Figure 23. Nexus TCK, TDI, TMS, TDO Timing

3.13.5 External interrupt timing (IRQ/NMI pin)

Table 35. External Interrupt timing[1]

Spec	Characteristic	Symbol	Min	Max	Unit
1	IRQ/NMI Pulse Width Low	t_{IPWL}	3	—	t_{cyc}[2]
2	IRQ/NMI Pulse Width High	t_{IPWH}	3	—	t_{cyc}[2]
3	IRQ/NMI Edge to Edge Time[3]	t_{ICYC}	6	—	t_{cyc}[2]

1. IRQ/NMI timing specified at V_{DD} = 1.08 V to 1.32 V, V_{DDEH} = 3.0 V to 5.5 V, $T_A = T_L$ to T_H.
2. For further information on t_{cyc}, see Table 3.
3. Applies when IRQ/NMI pins are configured for rising edge or falling edge events, but not both.

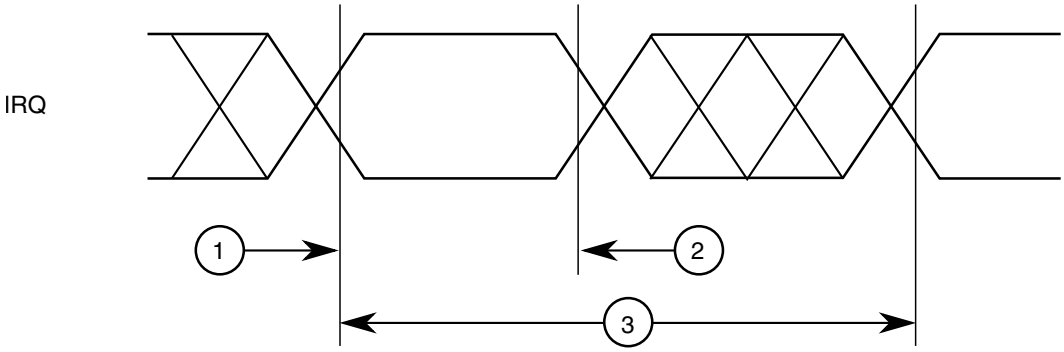

Figure 24. External interrupt timing

3.13.6 eTPU timing

Table 36. eTPU timing[1]

Spec	Characteristic	Symbol	Min	Max	Unit
1	eTPU Input Channel Pulse Width	t_{ICPW}	4	—	t_{CYC_ETPU}[2]
2	eTPU Output Channel Pulse Width	t_{OCPW}	1[3]	—	t_{CYC_ETPU}[2]

1. eTPU timing specified at V_{DD} = 1.08 V to 1.32 V, V_{DDEH} = 3.0 V to 5.5 V, $T_A = T_L$ to T_H, and C_L = 200 pF with SRC = 0b00.
2. For further information on t_{CYC_ETPU}, see Table 3.
3. This specification does not include the rise and fall times. When calculating the minimum eTPU pulse width, include the rise and fall times defined in the slew rate control fields (SRC) of the pad configuration registers (PCR).

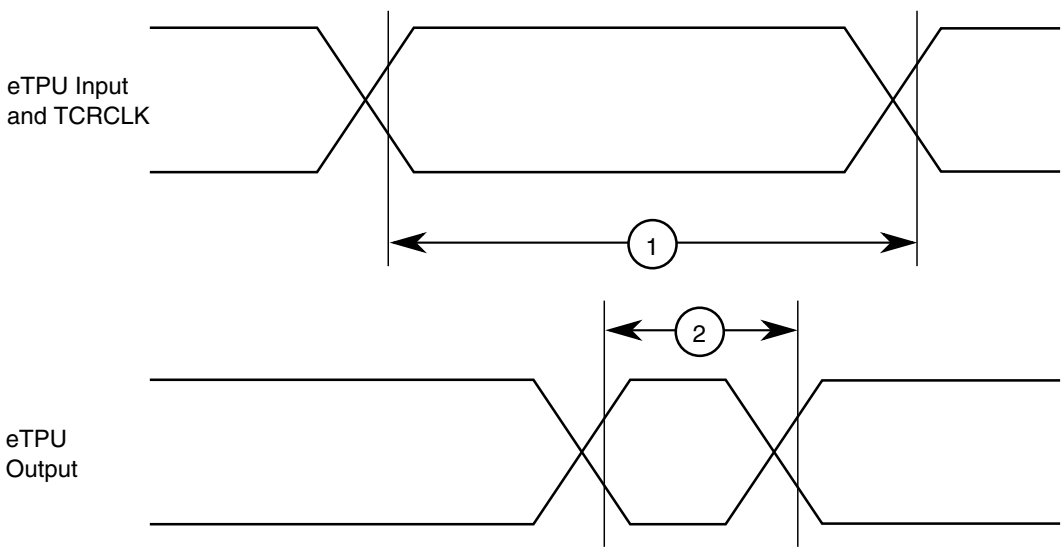

Figure 25. eTPU timing

Table 40. DSPI CMOS master modified timing (full duplex and output only) – MTFE = 1, CPHA = 0 or 1[1] (continued)

#	Symbol	Characteristic	Condition[2]		Value[3]		Unit
			Pad drive[4]	Load (C_L)	Min	Max	
7	t_{SUI}	SIN setup time to SCK CPHA = 0[10]	PCR[SRC]=11b	25 pF	29 – (P^{11} × t_{SYS}, [6])	—	ns
			PCR[SRC]=10b	50 pF	31 – (P^{11} × t_{SYS}, [6])	—	
			PCR[SRC]=01b	50 pF	62 – (P^{11} × t_{SYS}, [6])	—	
		SIN setup time to SCK CPHA = 1[10]	PCR[SRC]=11b	25 pF	29.0	—	ns
			PCR[SRC]=10b	50 pF	31.0	—	
			PCR[SRC]=01b	50 pF	62.0	—	
SIN hold time							
8	t_{HI}[12]	SIN hold time from SCK CPHA = 0[10]	PCR[SRC]=11b	0 pF	–1 + (P^{11} × t_{SYS}, [6])	—	ns
			PCR[SRC]=10b	0 pF	–1 + (P^{11} × t_{SYS}, [6])	—	
			PCR[SRC]=01b	0 pF	–1 + (P^{11} × t_{SYS}, [6])	—	
		SIN hold time from SCK CPHA = 1[10]	PCR[SRC]=11b	0 pF	–1.0	—	ns
			PCR[SRC]=10b	0 pF	–1.0	—	
			PCR[SRC]=01b	0 pF	–1.0	—	
SOUT data valid time (after SCK edge)							
9	t_{SUO}	SOUT data valid time from SCK CPHA = 0[13]	PCR[SRC]=11b	25 pF	—	7.0 + t_{SYS}[6]	ns
			PCR[SRC]=10b	50 pF	—	8.0 + t_{SYS}[6]	
			PCR[SRC]=01b	50 pF	—	18.0 + t_{SYS}[6]	
		SOUT data valid time from SCK CPHA = 1[13]	PCR[SRC]=11b	25 pF	—	7.0	ns
			PCR[SRC]=10b	50 pF	—	8.0	
			PCR[SRC]=01b	50 pF	—	18.0	
SOUT data hold time (after SCK edge)							
10	t_{HO}	SOUT data hold time after SCK CPHA = 0[13]	PCR[SRC]=11b	25 pF	–9.0 + t_{SYS}[6]	—	ns
			PCR[SRC]=10b	50 pF	–10.0 + t_{SYS}[6]	—	
			PCR[SRC]=01b	50 pF	–21.0 + t_{SYS}[6]	—	
		SOUT data hold time after SCK CPHA = 1[13]	PCR[SRC]=11b	25 pF	–9.0	—	ns
			PCR[SRC]=10b	50 pF	–10.0	—	
			PCR[SRC]=01b	50 pF	–21.0	—	

1. All output timing is worst case and includes the mismatching of rise and fall times of the output pads.
2. When a characteristic involves two signals, the pad drive and load conditions apply to each signal's pad, unless specified otherwise.
3. All timing values for output signals in this table are measured to 50% of the output voltage.
4. Pad drive is defined as the PCR[SRC] field setting in the SIU. Timing is guaranteed to same drive capabilities for all signals; mixing of pad drives may reduce operating speeds and may cause incorrect operation.
5. N is the number of clock cycles added to time between PCS assertion and SCK assertion and is software programmable using DSPI_CTARx[PSSCK] and DSPI_CTARx[CSSCK]. The minimum value is 2 cycles unless TSB mode or Continuous SCK clock mode is selected, in which case, N is automatically set to 0 clock cycles (PCS and SCK are driven by the same edge of DSPI_CLKn).
6. t_{SYS} is the period of DSPI_CLKn clock, the input clock to the DSPI module. Maximum frequency is 100 MHz (min t_{SYS} = 10 ns).
7. M is the number of clock cycles added to time between SCK negation and PCS negation and is software programmable using DSPI_CTARx[PASC] and DSPI_CTARx[ASC]. The minimum value is 2 cycles unless TSB mode or Continuous SCK

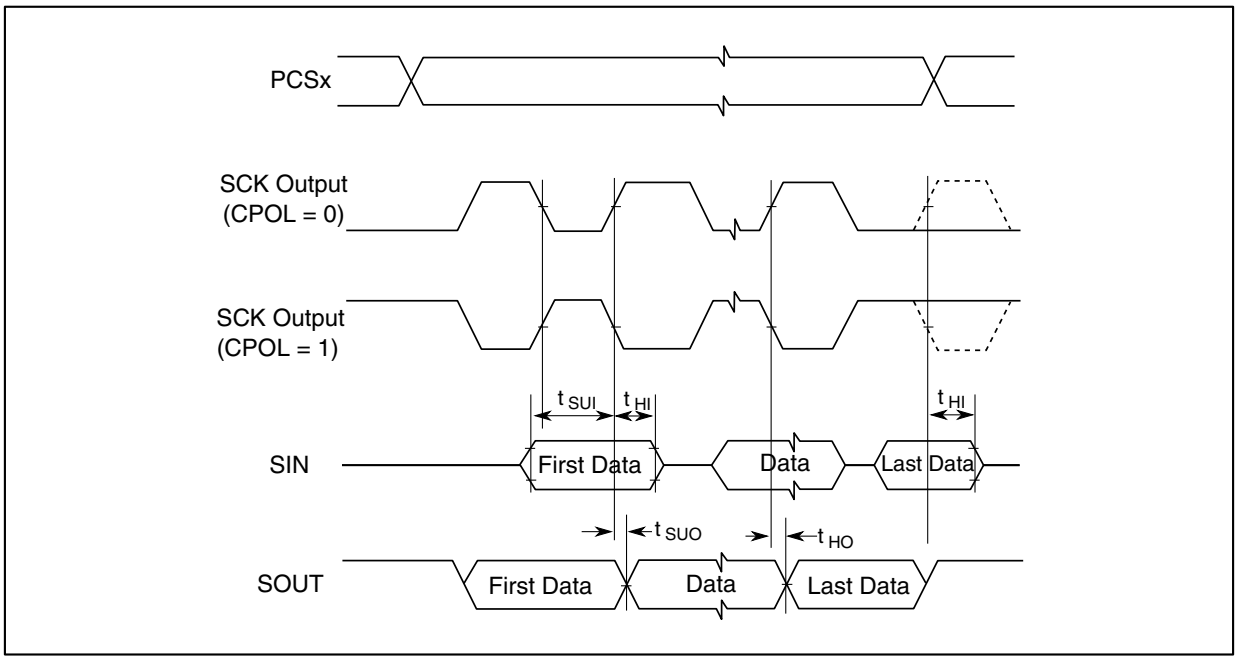

Figure 31. DSPI CMOS master mode – modified timing, CPHA = 1

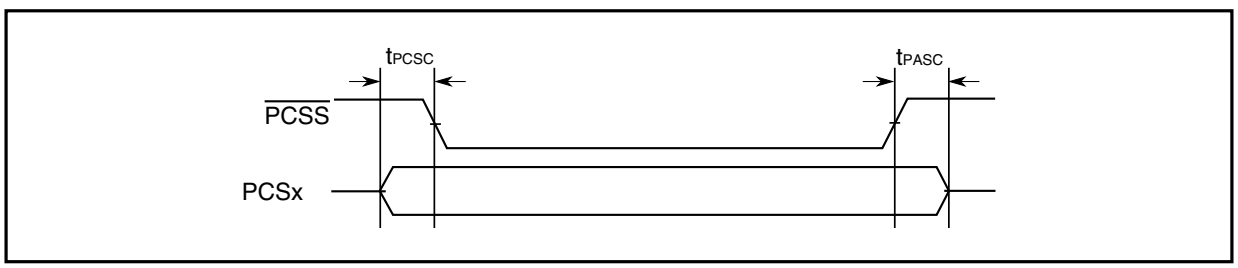

Figure 32. DSPI PCS strobe ($\overline{\text{PCSS}}$) timing (master mode)

3.13.8.1.3 DSPI LVDS Master Mode – Modified Timing

Table 41. DSPI LVDS master timing – full duplex – modified transfer format (MTFE = 1), CPHA = 0 or 1

#	Symbol	Characteristic	Condition[1]		Value[2]		Unit
			Pad drive[3]	Load (C_L)	Min	Max	
1	t_{SCK}	SCK cycle time	LVDS	15 pF to 25 pF differential	33.3	—	ns
2	t_{CSC}	PCS to SCK delay (LVDS SCK)	PCS: PCR[SRC]=11b	25 pF	($N^4 \times t_{SYS}$, [5]) – 10	—	ns
			PCS: PCR[SRC]=10b	50 pF	($N^4 \times t_{SYS}$, [5]) – 10	—	ns
			PCS: PCR[SRC]=01b	50 pF	($N^4 \times t_{SYS}$, [5]) – 32	—	ns

Table continues on the next page...