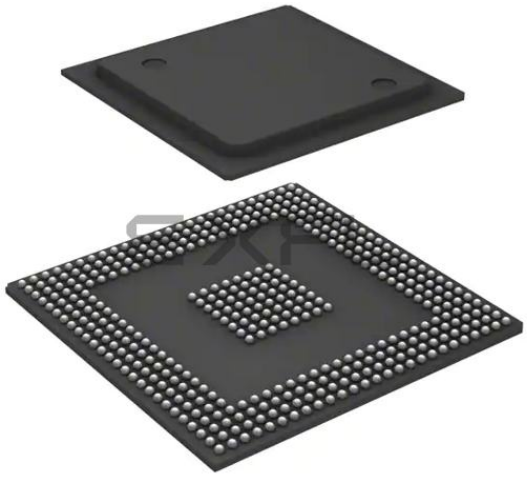

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Details	
Product Status	Active
Core Processor	e200z7
Core Size	32-Bit Dual-Core
Speed	264MHz
Connectivity	CANbus, EBI/EMI, Ethernet, FlexCANbus, LINbus, SCI, SPI
Peripherals	DMA, LVD, POR, Zipwire
Number of I/O	293
Program Memory Size	4MB (4M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 40x12b eQADCx2
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	416-BGA
Supplier Device Package	416-MAPBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5775edk3mme3r

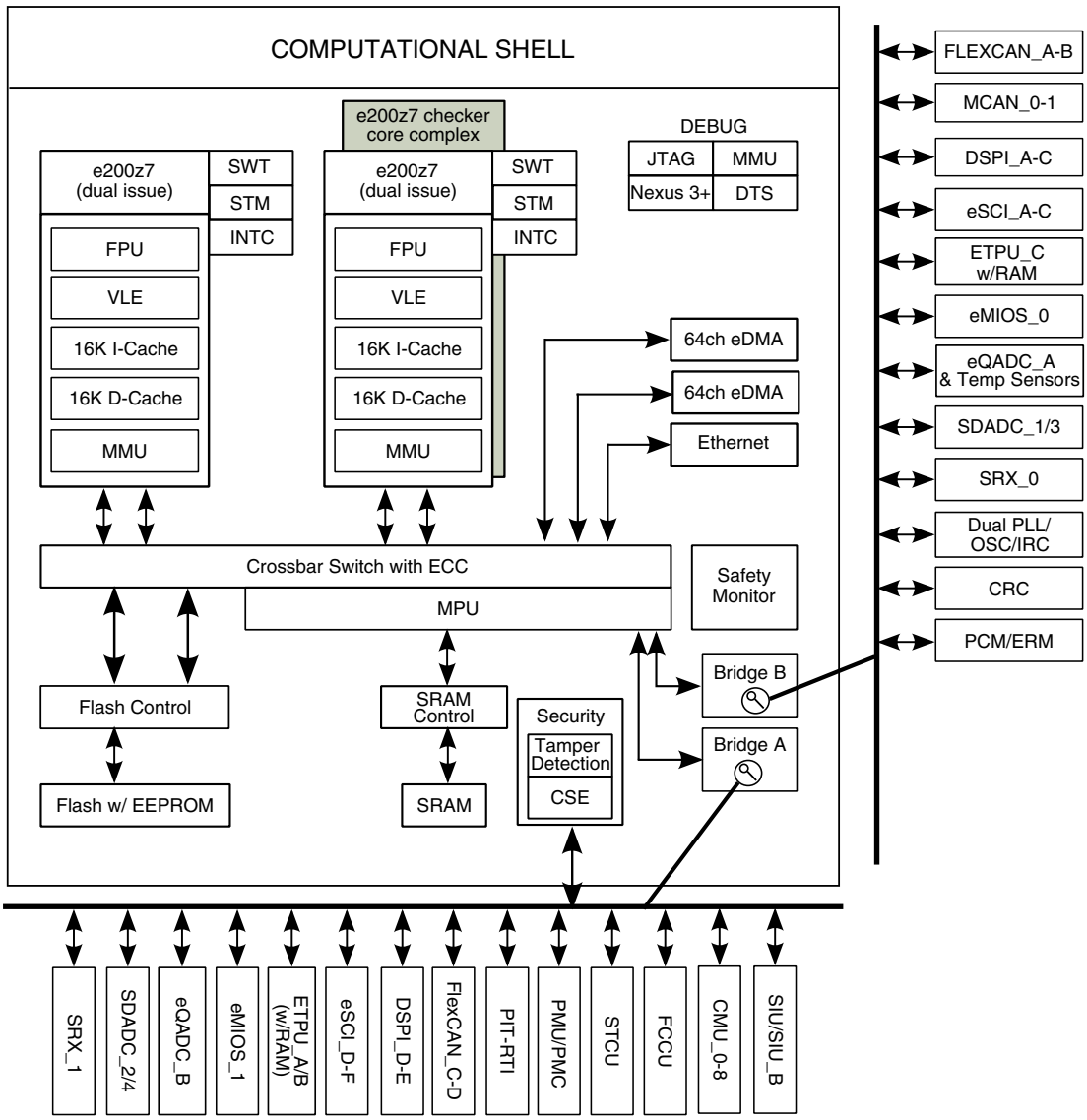


Figure 1. MPC5775E block diagram

2 Pinouts

2.1 416-ball MAPBGA pin assignments

Figure 2 shows the 416-ball MAPBGA pin assignments.

1. I_{DD} measured on an application-specific pattern with all cores enabled at full frequency, T_J = 40°C to 150°C. Flash memory program/erase current on the V_{DD} supply not included.
2. This value is considering the use of the internal core regulator with the simulation of an external transistor with the minimum value of h_{FE} of 60.
3. This bandgap reference is for EQADC calibration and Temperature Sensors.

3.6 I/O pad specifications

The following table describes the different pad types on the chip.

Table 5. I/O pad specification descriptions

Pad type	Description
General-purpose I/O pads	General-purpose I/O with four selectable output slew rate settings; also called SR pads
LVDS pads	Low Voltage Differential Signal interface pads
Input-only pads	Low-input-leakage pads that are associated with the ADC channels

NOTE

Each I/O pin on the device supports specific drive configurations. See the signal description table in the device reference manual for the available drive configurations for each I/O pin.

NOTE

Throughout the I/O pad specifications, the symbol V_{DDEx} represents all V_{DDEx} and V_{DDEHx} segments.

3.6.1 Input pad specifications

Table 6 provides input DC electrical characteristics as described in Figure 3.

Table 7. I/O pullup/pulldown DC electrical characteristics

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
I_{WPU}	Weak pullup current	V_{IN} = 0.35 * V_{DDEx} 4.5 V < V_{DDEx} < 5.5 V	40	—	120	µA
		V_{IN} = 0.35 * V_{DDEx} 3.0 V < V_{DDEx} < 3.6 V	25	—	80	
I_{WPD}	Weak pulldown current	V_{IN} = 0.65 * V_{DDEx} 4.5 V < V_{DDEx} < 5.5 V	40	—	120	µA
		V_{IN} = 0.65 * V_{DDEx} 3.0 V < V_{DDEx} < 3.6 V	25	—	80	

The specifications in Table 8 apply to the pins ANA0_SDA0 to ANA7, ANA16_SDB0 to ANA23_SDC3, and ANB0_SDD0 to ANB7_SDD7.

Table 8. I/O pullup/pulldown resistance electrical characteristics

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
R_{PUPD}	Analog input bias / diagnostic pullup/ pulldown resistance	200 kΩ	130	200	280	kΩ
		100 kΩ	65	100	140	
		5 kΩ	1.4	5	7.5	
Δ_{PUPD}	R_{PUPD} pullup/pulldown resistance mismatch	—	—	—	5	%

3.6.2 Output pad specifications

Figure 4 shows output DC electrical characteristics.

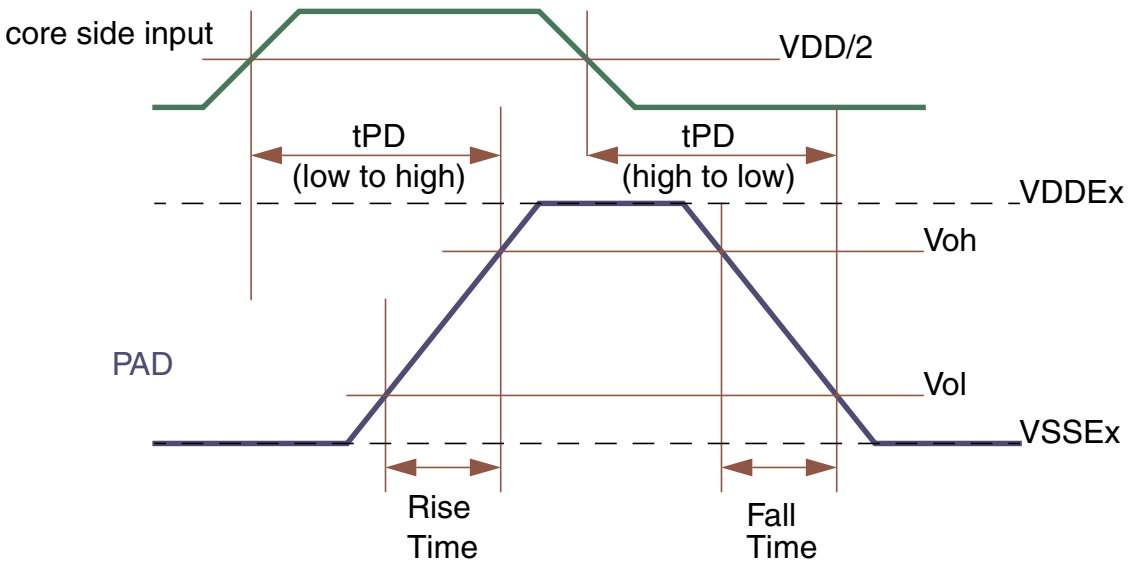


Figure 4. I/O output DC electrical characteristics definition

The following tables specify output DC electrical characteristics.

Table 9. GPIO data pad output buffer electrical characteristics (SR pads)[1]

Symbol	Parameter	Conditions[2]		Value[3]			Unit
				Min	Typ	Max	
I_{OH}	GPIO pad output high current	V_{OH} = 0.8 * V_{DDEx}	PCR[SRC] = 11b or 01b	25	—	—	mA
		4.5 V < V_{DDEx} < 5.5 V	PCR[SRC] = 10b or 00b	15	—	—	
		V_{OH} = 0.8 * V_{DDEx}	PCR[SRC] = 11b or 01b	13	—	—	
		3.0 V < V_{DDEx} < 3.6 V	PCR[SRC] = 10b or 00b	8	—	—	
I_{OL}	GPIO pad output low current	V_{OL} = 0.2 * V_{DDEx}	PCR[SRC] = 11b or 01b	48	—	—	mA
		4.5 V < V_{DDEx} < 5.5 V	PCR[SRC] = 10b or 00b	22	—	—	
		V_{OL} = 0.2 * V_{DDEx}	PCR[SRC] = 11b or 01b	17	—	—	
		3.0 V < V_{DDEx} < 3.6 V	PCR[SRC] = 10b or 00b	10.5	—	—	

Table continues on the next page...

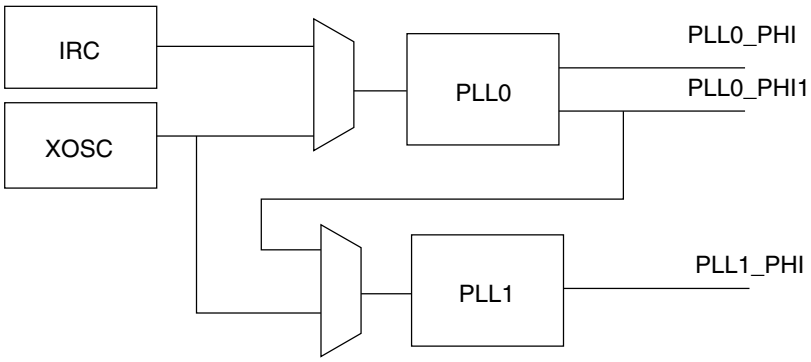


Figure 5. PLL integration

3.7.1 PLL electrical specifications

Table 11. PLL0 electrical characteristics

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
f_{PLL0IN}	PLL0 input clock[1, 2]	—	8	—	44	MHz
Δ_{PLL0IN}	PLL0 input clock duty cycle[2]	—	40	—	60	%
$f_{PLL0VCO}$	PLL0 VCO frequency	—	600	—	1250	MHz
$f_{PLL0PHI}$	PLL0 output frequency	—	4.762	—	200	MHz
$t_{PLL0LOCK}$	PLL0 lock time	—	—	—	110	µs
$\lvert\Delta_{PLL0PHISPJ}\rvert$	PLL0_PHI single period jitter f_{PLL0IN} = 20 MHz (resonator)	$f_{PLL0PHI}$ = 200 MHz, 6-sigma	—	—	200	ps
$\lvert\Delta_{PLL0PHI1SPJ}\rvert$	PLL0_PHI1 single period jitter f_{PLL0IN} = 20 MHz (resonator)	$f_{PLL0PHI1}$ = 40 MHz, 6-sigma	—	—	300[3]	ps
$\Delta_{PLL0LTJ}$	PLL0 output long term jitter[3] f_{PLL0IN} = 20 MHz (resonator), VCO frequency = 800 MHz	10 periods accumulated jitter (80 MHz equivalent frequency), 6-sigma pk-pk	—	—	±250	ps
		16 periods accumulated jitter (50 MHz equivalent frequency), 6-sigma pk-pk	—	—	±300	ps
		long term jitter (< 1 MHz equivalent frequency), 6-sigma pk-pk)	—	—	±500	ps
I_{PLL0}	PLL0 consumption	FINE LOCK state	—	—	7.5	mA

1. Ensure that the f_{PLL0IN} frequency divided by PLLDIG_PLL0DV[PREDIV] is in the range 8 MHz to 20 MHz.
2. PLL0IN clock retrieved directly from either internal IRC or external XOSC clock. Input characteristics are granted when using internal IRC or external oscillator is used in functional mode.
3. Noise on the V_{DD} supply with frequency content below 40 kHz and above 50 MHz is filtered by the PLL. Noise on the V_{DD} supply with frequency content in the range of 40 kHz – 50 MHz must be filtered externally to the device.

Table 12. PLL1 electrical characteristics

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
f_{PLL1IN}	PLL1 input clock[1]	—	38	—	78	MHz

Table continues on the next page...

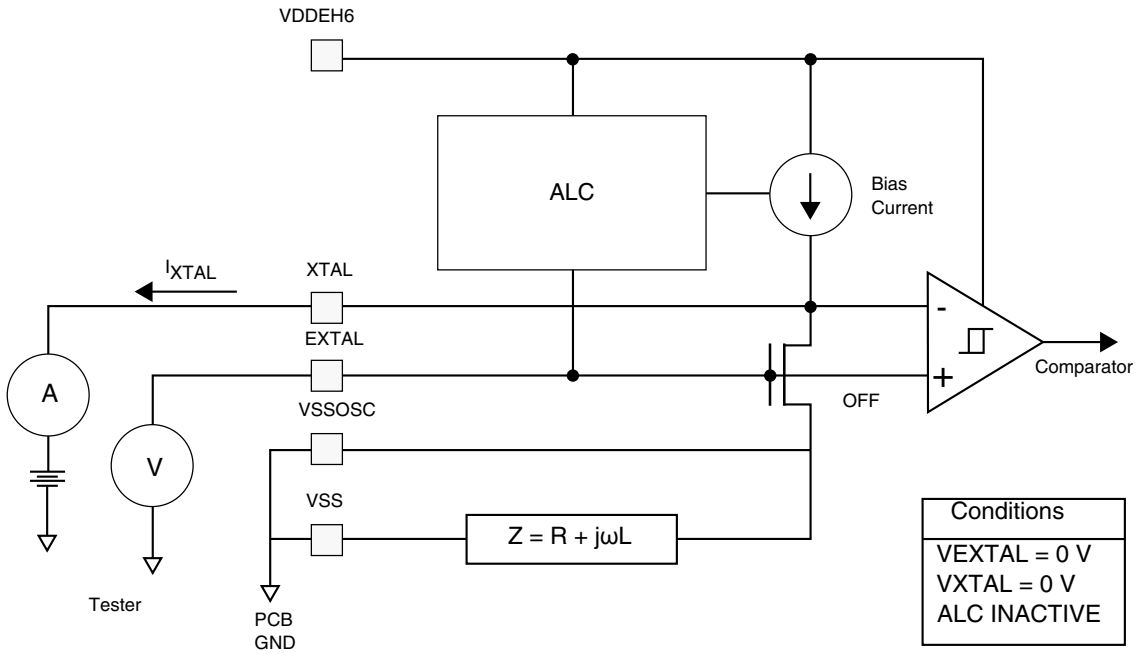


Figure 6. Test circuit

Table 15. Internal RC (IRC) oscillator electrical specifications

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
f_{Target}	IRC target frequency	—	—	16	—	MHz
δf_{var_T}	IRC frequency variation	T < 150 °C	–8	—	8	%

3.8 Analog-to-Digital Converter (ADC) electrical specifications

3.8.1 Enhanced Queued Analog-to-Digital Converter (eQADC)

Table 16. eQADC conversion specifications (operating)

Symbol	Parameter	Value		Unit
		Min	Max	
f_{ADCLK}	ADC Clock (ADCLK) Frequency	2	33	MHz
CC	Conversion Cycles	2 + 13	128 + 15[1]	ADCLK cycles
T_{SR}	Stop Mode Recovery Time[2]	10	—	µs
—	Resolution[3]	1.25	—	mV
INL	INL: 16.5 MHz eQADC clock[4]	–4	4	LSB[5]
	INL: 33 MHz eQADC clock[4]	–6	6	LSB

Table continues on the next page...

Table 16. eQADC conversion specifications (operating) (continued)

Symbol	Parameter	Value		Unit
		Min	Max	
DNL	DNL: 16.5 MHz eQADC clock[4]	–3	3	LSB
	DNL: 33 MHz eQADC clock[4]	–3	3	LSB
OFFNC	Offset Error without Calibration	0	140	LSB
OFFWC	Offset Error with Calibration	–8	8	LSB
GAINNC	Full Scale Gain Error without Calibration	–150	0	LSB
GAINWC	Full Scale Gain Error with Calibration	–8	8	LSB
I_{INJ}	Disruptive Input Injection Current[6, 7, 8, 9]	–3	3	mA
E_{INJ}	Incremental Error due to injection current[10, 11]	—	+4	Counts
TUE	TUE value[12, 13] (with calibration)	—	±8	Counts
GAINVGA1	Variable gain amplifier accuracy (gain = 1)[14]	-	-	Counts[16]
	INL, 16.5 MHz ADC	–4	4	
	INL, 33 MHz ADC	–8	8	
	DNL, 16.5 MHz ADC	–3[15]	3[15]	
	DNL, 33 MHz ADC	–3[15]	3[15]	
GAINVGA2	Variable gain amplifier accuracy (gain = 2)[14]	-	-	Counts
	INL, 16.5 MHz ADC	–5	5	
	INL, 33 MHz ADC	–8	8	
	DNL, 16.5 MHz ADC	–3	3	
	DNL, 33 MHz ADC	–3	3	
GAINVGA4	Variable gain amplifier accuracy (gain = 4)[14]	-	-	Counts
	INL, 16.5 MHz ADC	–7	7	
	INL, 33 MHz ADC	–8	8	
	DNL, 16.5 MHz ADC	–4	4	
	DNL, 33 MHz ADC	–4	4	
I_{ADC}	Current consumption per ADC (two ADCs per EQADC)	—	10	mA
I_{ADR}	Reference voltage current consumption per EQADC	—	200	µA

1. 128 sampling cycles (LST=128), differential conversion, pregain of x4
2. Stop mode recovery time is the time from the setting of either of the enable bits in the ADC Control Register to the time that the ADC is ready to perform conversions. Delay from power up to full accuracy = 8 ms.
3. At $V_{RH\_EQ} – V_{RL\_EQ}$ = 5.12 V, one count = 1.25 mV without using pregain. Based on 12-bit conversion result; does not account for AC and DC errors
4. INL and DNL are tested from V_{RL} + 50 LSB to V_{RH} – 50 LSB.
5. At $V_{RH\_EQ} – V_{RL\_EQ}$ = 5.12 V, one LSB = 1.25 mV.
6. Below disruptive current conditions, the channel being stressed has conversion values of $3FF for analog inputs greater than V_{RH} and $000 for values less than V_{RL}. Other channels are not affected by non-disruptive conditions.
7. Exceeding limit may cause conversion error on stressed channels and on unstressed channels. Transitions within the limit do not affect device reliability or cause permanent damage.
8. Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values using $V_{POSCLAMP} = V_{DDA}$ + 0.5 V and $V_{NEGCLAMP}$ = –0.3 V, then use the larger of the calculated values.
9. Condition applies to two adjacent pins at injection limits.
10. Performance expected with production silicon.

Table 17. SDADC electrical specifications (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
$\|\delta_{GAIN}\|$	Absolute value of the ADC gain error[6, 7]	Before calibration (applies to gain setting = 1)	—	—	1.5	%
		After calibration $\Delta V_{RH\_SD} < 5\%$, $\Delta V_{DDA\_SD} < 10\%$ $\Delta T_J < 50$ °C	—	—	5	mV
		After calibration $\Delta V_{RH\_SD} < 5\%$, $\Delta V_{DDA\_SD} < 10\%$ $\Delta T_J < 100$ °C	—	—	7.5	
		After calibration $\Delta V_{RH\_SD} < 5\%$, $\Delta V_{DDA\_SD} < 10\%$ $\Delta T_J < 150$ °C	—	—	10	
V_{OFFSET}	Conversion offset[6, 7]	Before calibration (applies to all gain settings: 1, 2, 4, 8, 16)	—	10*(1+1/gain)	20	mV
		After calibration $\Delta V_{DDA\_SD} < 10\%$ $\Delta T_J < 50$ °C	—	—	5	
		After calibration $\Delta V_{DDA\_SD} < 10\%$ $\Delta T_J < 100$ °C	—	—	7.5	
		After calibration $\Delta V_{DDA\_SD} < 10\%$ $\Delta T_J < 150$ °C	—	—	10	
$SNR_{DIFF150}$	Signal to noise ratio in differential mode, 150 Ksps output rate	4.5 V < V_{DDA_SD} < 5.5 V[8, 9] $V_{RH\_SD} = V_{DDA\_SD}$ GAIN = 1	80	—	—	dB
		4.5 V < V_{DDA_SD} < 5.5 V[8, 9] $V_{RH\_SD} = V_{DDA\_SD}$ GAIN = 2	77	—	—	
		4.5 V < V_{DDA_SD} < 5.5 V[8, 9] $V_{RH\_SD} = V_{DDA\_SD}$ GAIN = 4	74	—	—	
		4.5 V < V_{DDA_SD} < 5.5 V[8, 9] $V_{RH\_SD} = V_{DDA\_SD}$ GAIN = 8	71	—	—	
		4.5 V < V_{DDA_SD} < 5.5 V[8, 9] $V_{RH\_SD} = V_{DDA\_SD}$ GAIN = 16	68	—	—	

Table continues on the next page...

Table 17. SDADC electrical specifications (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
$SINAD_{SE150}$	Signal to noise and distortion ratio in single-ended mode, 150 Ksps output rate	Gain = 1 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	66	—	—	dBFS
		Gain = 2 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	66	—	—	
		Gain = 4 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	63	—	—	
		Gain = 8 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	62	—	—	
		Gain = 16 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	54	—	—	
$THD_{DIFF150}$	Total harmonic distortion in differential mode, 150 Ksps output rate	Gain = 1 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	65	—	—	dBFS
		Gain = 2 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	68	—	—	
		Gain = 4 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	74	—	—	
		Gain = 8 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	80	—	—	
		Gain = 16 4.5 V < V_{DDA_SD} < 5.5 V V_{RH_SD} = V_{DDA_SD}	80	—	—	

Table continues on the next page...

Table 17. SDADC electrical specifications (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
Z_{CM}	Common Mode input impedance[11, 12]	GAIN = 1	1400	1800	2200	kΩ
		GAIN = 2	1000	1300	1600	
		GAIN = 4	700	950	1150	
		GAIN = 8	500	650	800	
		GAIN = 16	500	650	800	
R_{BIAS}	Bare bias resistance	—	110	144	180	kΩ
ΔV_{INTCM}	Common Mode input reference voltage[13]	—	–12	—	+12	%
V_{BIAS}	Bias voltage	—	—	$V_{RH\_SD}/2$	—	V
δV_{BIAS}	Bias voltage accuracy	—	–2.5	—	+2.5	%
CMRR	Common mode rejection ratio	—	20	—	—	dB
R_{Caaf}	Anti-aliasing filter	External series resistance	—	—	20	kΩ
		Filter capacitances	220	—	—	pF
$f_{PASSBAND}$	Pass band[9]	—	0.01	—	0.333 * f_{ADCD_S}	kHz
δ_{RIPPLE}	Pass band ripple[14]	0.333 * f_{ADCD_S}	–1	—	1	%
$F_{rolloff}$	Stop band attenuation	[0.5 * f_{ADCD_S}, 1.0 * f_{ADCD_S}]	40	—	—	dB
		[1.0 * f_{ADCD_S}, 1.5 * f_{ADCD_S}]	45	—	—	
		[1.5 * f_{ADCD_S}, 2.0 * f_{ADCD_S}]	50	—	—	
		[2.0 * f_{ADCD_S}, 2.5 * f_{ADCD_S}]	55	—	—	
		[2.5 * f_{ADCD_S}, $f_{ADCD\_M}/2$]	60	—	—	

Table continues on the next page...

3.11.1 Power management electrical characteristics

The power management module monitors the different power supplies. It also generates the internal supplies that are required for correct device functionality. The power management is supplied by the V_{DDPMC} supply.

3.11.1.1 LDO mode recommended power transistors

Only specific orderable part numbers of MPC5775E support LDO regulation mode. See Ordering information for MPC5775E parts that support this regulation mode.

The following NPN transistors are recommended for use with the on-chip LDO voltage regulator controller: ON Semiconductor™ NJD2873. The collector of the external transistor is preferably connected to the same voltage supply source as the output stage of the regulator.

The following table describes the characteristics of the power transistors.

Table 21. Recommended operating characteristics

Symbol	Parameter	Value	Unit
h_{FE}	DC current gain (Beta)	60-550	—
P_D	Absolute minimum power dissipation	1.60	W
I_{CMaxDC}	Maximum DC collector current	2.0	A
VCE_{SAT}	Collector to emitter saturation voltage	300	mV
V_{BE}	Base to emitter voltage	0.95	V
V_c	Minimum voltage at transistor collector	2.5	V

The following table shows the recommended components to be used in LDO regulation mode.

Table 22. Recommended operating characteristics

Part name	Part type	Nominal	Description
Q1	NPN BJT	h_{FE} = 400	NJD2873: ON Semiconductor LDO voltage regulator controller (VRC)
CI	Capacitor	4.7 µF - 20 V	Ceramic capacitor, total ESR < 70 mΩ
CE	Capacitor	0.047–0.049 µF - 7 V	Ceramic—one capacitor for each V_{DD} pin
CV	Capacitor	22 µF - 20 V	Ceramic V_{DDPMC} (optional 0.1 µF)
CD	Capacitor	22 µF - 20 V	Ceramic supply decoupling capacitor, ESR < 50 mΩ (as close as possible to NPN collector)
CB	Capacitor	0.1 µF - 7 V	Ceramic V_{DDPWR}
R	Resistor	Application specific	Optional; reduces thermal loading on the NPN with high V_{DDPMC} levels

The following diagram shows the LDO configuration connection.

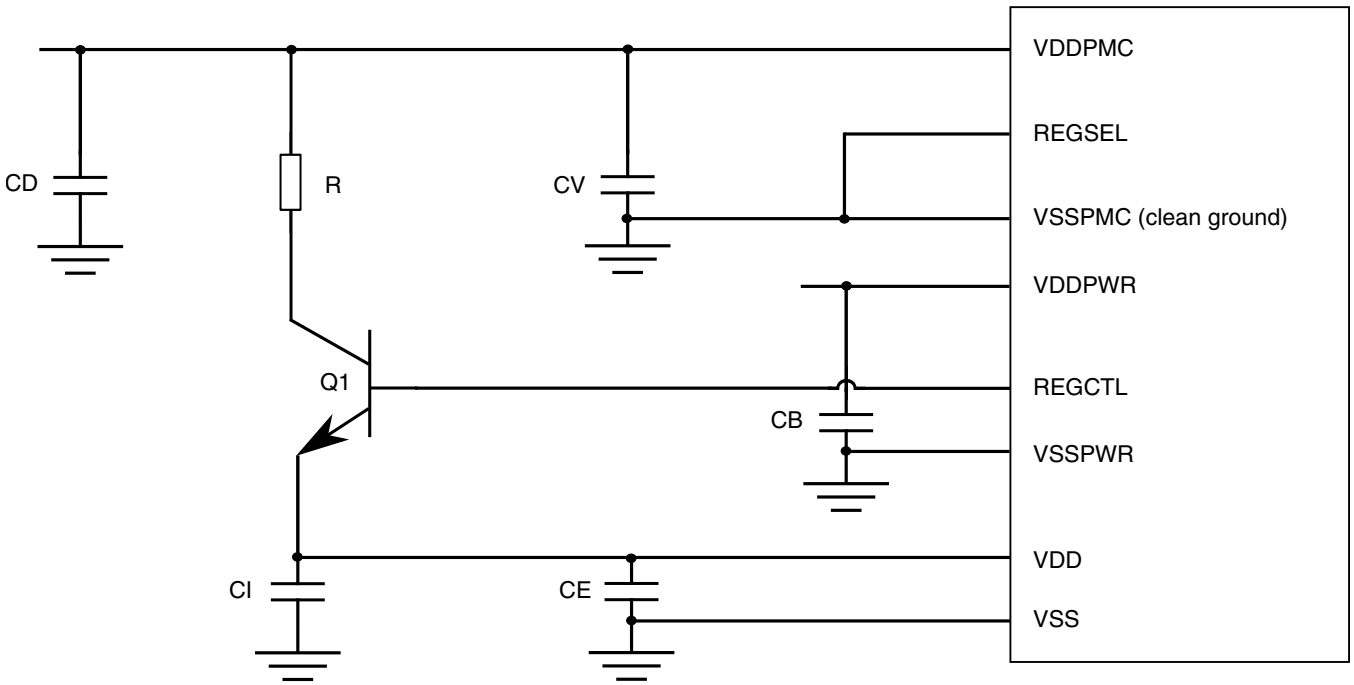


Figure 11. VRC 1.2 V LDO configuration

3.11.1.2 SMPS mode recommended external components and characteristics

The following table shows the recommended components to be used in SMPS regulation mode.

Table 23. Recommended operating characteristics

Part name	Part type	Nominal	Description
Q1	p-MOS	3 A - 20 V	SQ2301ES / FDC642P or equivalent: low threshold p-MOS, Vth < 2.0 V, Rdson @ 4.5 V < 100 mΩ, Cg < 5 nF
D1	Schottky	2 A - 20 V	SS8P3L or equivalent: Vishay™ low Vf Schottky diode
L	Inductor	3−4 µH - 1.5 A	Buck shielded coil low ESR
CI	Capacitor	22 µF - 20 V	Ceramic capacitor, total ESR < 70 mΩ
CE	Capacitor	0.1 µF - 7 V	Ceramic—one capacitor for each V_{DD} pin
CV	Capacitor	22 µF - 20 V	Ceramic V_{DDPMC} (optional 0.1 µF capacitor in parallel)
CD	Capacitor	22 µF - 20 V	Ceramic supply decoupling capacitor, ESR < 50 mΩ (as close as possible to the p-MOS source)
R	Resistor	2.0-4.7 kΩ	Pullup for power p-MOS gate
CB	Capacitor	22 µF - 20 V	Ceramic, connect 100 nF capacitor in parallel (as close as possible to package to reduce current loop from V_{DDPWR} to V_{SSPWR})

The following diagram shows the SMPS configuration connection.

3.12.2 Flash memory Array Integrity and Margin Read specifications

Table 28. Flash memory Array Integrity and Margin Read specifications

Symbol	Characteristic	Min	Typical	Max[1]	Units [2]
$t_{ai16kseq}$	Array Integrity time for sequential sequence on 16 KB block.	—	—	512 x Tperiod x Nread	—
$t_{ai32kseq}$	Array Integrity time for sequential sequence on 32 KB block.	—	—	1024 x Tperiod x Nread	—
$t_{ai64kseq}$	Array Integrity time for sequential sequence on 64 KB block.	—	—	2048 x Tperiod x Nread	—
tai256kseq	Array Integrity time for sequential sequence on 256 KB block.	—	—	8192 x Tperiod x Nread	—
$t_{mr16kseq}$	Margin Read time for sequential sequence on 16 KB block.	73.81	—	110.7	µs
$t_{mr32kseq}$	Margin Read time for sequential sequence on 32 KB block.	128.43	—	192.6	µs
$t_{mr64kseq}$	Margin Read time for sequential sequence on 64 KB block.	237.65	—	356.5	µs
$t_{mr256kseq}$	Margin Read time for sequential sequence on 256 KB block.	893.01	—	1,339.5	µs

1. Array Integrity times need to be calculated and is dependent on system frequency and number of clocks per read. The equation presented require Tperiod (which is the unit accurate period, thus for 200 MHz, Tperiod would equal 5e-9) and Nread (which is the number of clocks required for read, including pipeline contribution. Thus for a read setup that requires 6 clocks to read with no pipeline, Nread would equal 6. For a read setup that requires 6 clocks to read, and has the address pipeline set to 2, Nread would equal 4 (or 6 - 2).)
2. The units for Array Integrity are determined by the period of the system clock. If unit accurate period is used in the equation, the results of the equation are also unit accurate.

3.12.3 Flash memory module life specifications

Table 29. Flash memory module life specifications

Symbol	Characteristic	Conditions	Min	Typical	Units
Array P/E cycles	Number of program/erase cycles per block for 16 KB, 32 KB and 64 KB blocks.[1]	—	250,000	—	P/E cycles
	Number of program/erase cycles per block for 256 KB blocks.[2]	—	1,000	250,000	P/E cycles
Data retention	Minimum data retention.	Blocks with 0 - 1,000 P/E cycles.	50	—	Years
		Blocks with 100,000 P/E cycles.	20	—	Years
		Blocks with 250,000 P/E cycles.	10	—	Years

1. Program and erase supported across standard temperature specs.
2. Program and erase supported across standard temperature specs.

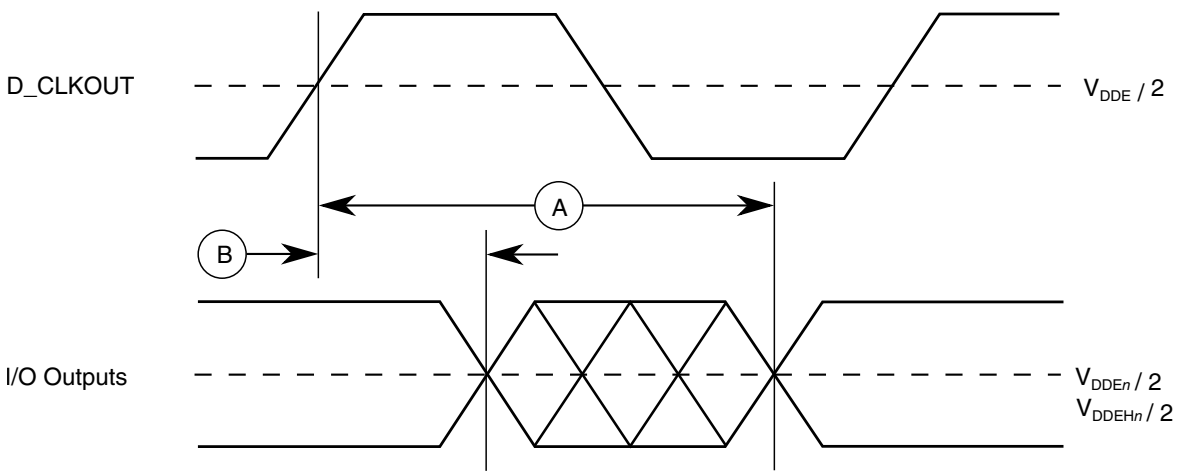
Table 31. Flash memory read wait-state and address-pipeline control combinations (continued)

Flash memory frequency	RWSC	APC	Flash memory read latency on mini-cache miss (# of f_{PLATF} clock periods)	Flash memory read latency on mini-cache hit (# of f_{PLATF} clock periods)
100 MHz < f_{PLATF} ≤ 133 MHz	3	1	6	1

3.13 AC timing

3.13.1 Generic timing diagrams

The generic timing diagrams in Figure 15 and Figure 16 apply to all I/O pins with pad types SR and FC. See the associated MPC5775E Microsoft Excel® file in the Reference Manual for the pad type for each pin.



A – Maximum Output Delay Time B – Minimum Output Hold Time

Figure 15. Generic output delay/hold timing

3.13.7 eMIOS timing

Table 37. eMIOS timing[1]

Spec	Characteristic	Symbol	Min	Max	Unit
1	eMIOS Input Pulse Width	t_{MIPW}	4	—	t_{CYC_PER}[2]
2	eMIOS Output Pulse Width	t_{MOPW}	1[3]	—	t_{CYC_PER}[2]

1. eMIOS timing specified at V_{DD} = 1.08 V to 1.32 V, V_{DDEH} = 3.0 V to 5.5 V, T_A = T_L to T_H, and C_L = 50 pF with SRC = 0b00.
2. For further information on t_{CYC_PER}, see Table 3.
3. This specification does not include the rise and fall times. When calculating the minimum eMIOS pulse width, include the rise and fall times defined in the slew rate control fields (SRC) of the pad configuration registers (PCR).

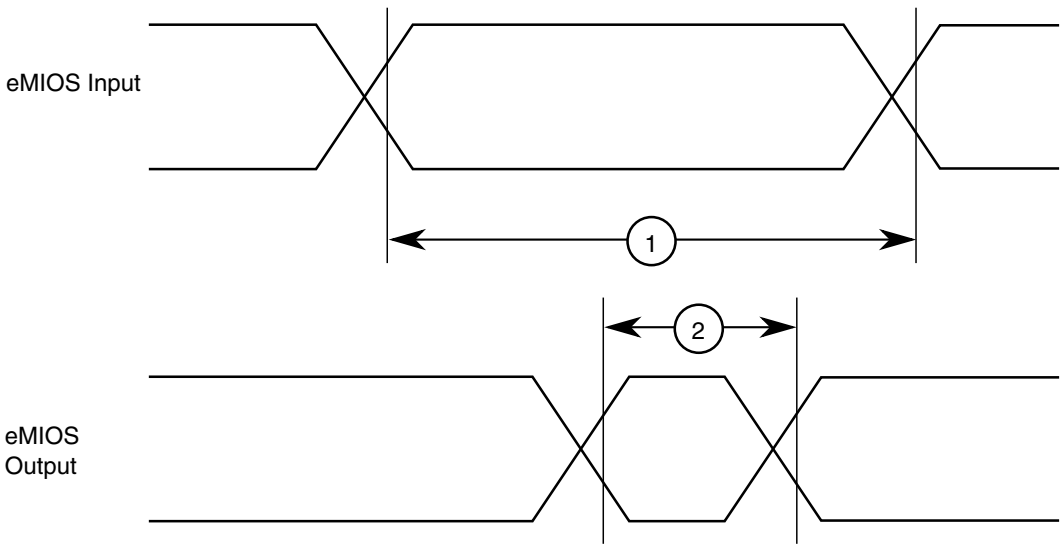


Figure 26. eMIOS timing

3.13.8 DSPI timing with CMOS and LVDS pads

NOTE

The DSPI in TSB mode with LVDS pads can be used to implement the Micro Second Channel (MSC) bus protocol.

DSPI channel frequency support is shown in Table 38. Timing specifications are shown in Table 39, Table 40, Table 41, Table 42, and Table 43.

Table 38. DSPI channel frequency support

DSPI use mode		Max usable frequency (MHz)[1, 2]
CMOS (Master mode)	Full duplex – Classic timing (Table 39)	17
	Full duplex – Modified timing (Table 40)	30
	Output only mode (SCK/SOUT/PCS) (Table 39 and Table 40)	30
	Output only mode TSB mode (SCK/SOUT/PCS) (Table 43)	30

Table continues on the next page...

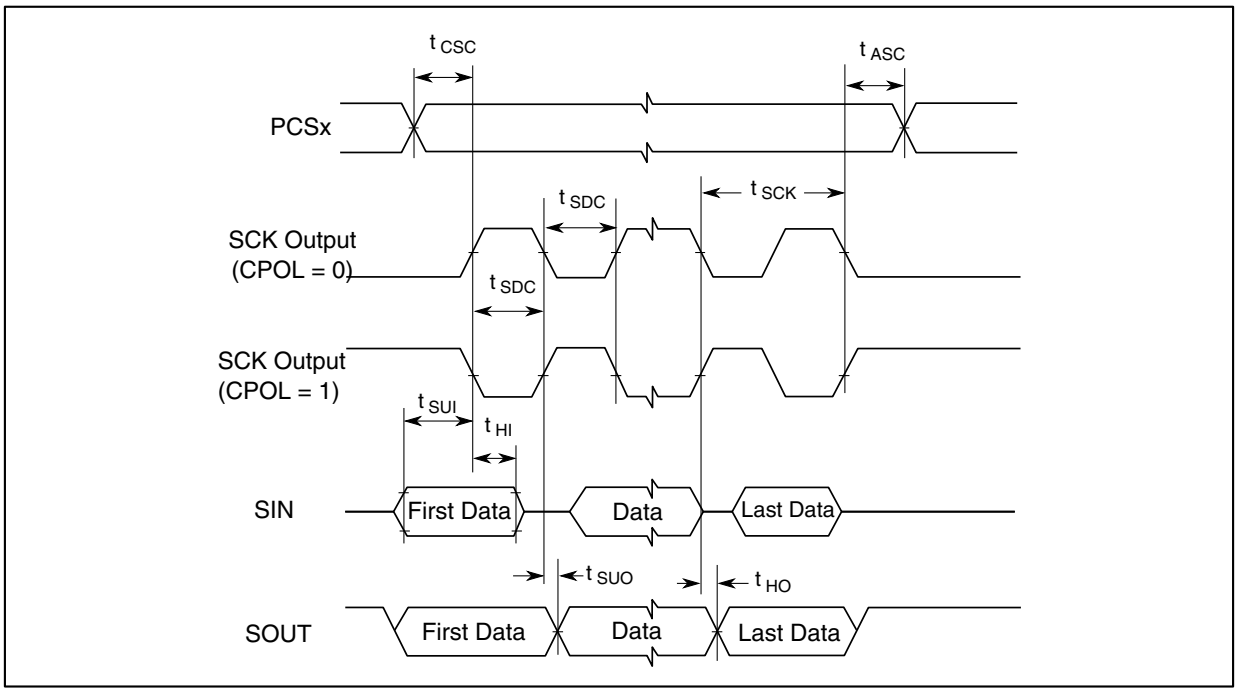


Figure 27. DSPI CMOS master mode – classic timing, CPHA = 0

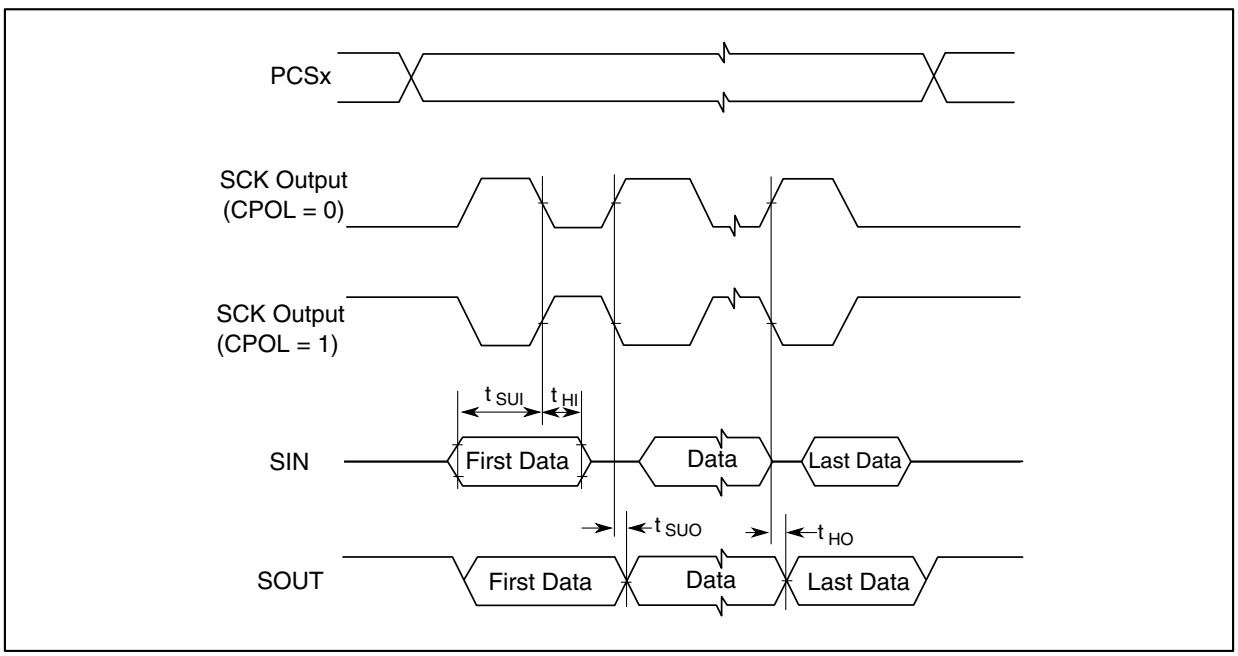


Figure 28. DSPI CMOS master mode – classic timing, CPHA = 1

4. All timing values for output signals in this table are measured to 50% of the output voltage.
5. Pad drive is defined as the PCR[SRC] field setting in the SIU. Timing is guaranteed to same drive capabilities for all signals; mixing of pad drives may reduce operating speeds and may cause incorrect operation.
6. With TSB mode or Continuous SCK clock mode selected, PCS and SCK are driven by the same edge of DSPI_CLKn. This timing value is due to pad delays and signal propagation delays.
7. SOUT Data Valid and Data hold are independent of load capacitance if SCK and SOUT load capacitances are the same value.

Table 43. DSPI CMOS master timing – output only – timed serial bus mode TSB = 1 or ITSB = 1, CPOL = 0 or 1, continuous SCK clock [1, 2]

#	Symbol	Characteristic	Condition[3]		Value[4]		Unit
			Pad drive[5]	Load (C_L)	Min	Max	
1	t_{SCK}	SCK cycle time	PCR[SRC]=11b	25 pF	33.0	—	ns
			PCR[SRC]=10b	50 pF	80.0	—	ns
			PCR[SRC]=01b	50 pF	200.0	—	ns
2	t_{CSV}	PCS valid after SCK[6]	PCR[SRC]=11b	25 pF	7	—	ns
			PCR[SRC]=10b	50 pF	8	—	ns
			PCR[SRC]=01b	50 pF	18	—	ns
			PCS: PCR[SRC]=01b SCK: PCR[SRC]=10b	50 pF	45	—	ns
3	t_{CSH}	PCS hold after SCK[6]	PCR[SRC]=11b	PCS: 0 pF SCK: 50 pF	–14	—	ns
			PCR[SRC]=10b	PCS: 0 pF SCK: 50 pF	–14	—	ns
			PCR[SRC]=01b	PCS: 0 pF SCK: 50 pF	–33	—	ns
			PCS: PCR[SRC]=01b SCK: PCR[SRC]=10b	PCS: 0 pF SCK: 50 pF	–35	—	ns
4	t_{SDC}	SCK duty cycle[7]	PCR[SRC]=11b	0 pF	$1/2t_{SCK} - 2$	$1/2t_{SCK} + 2$	ns
			PCR[SRC]=10b	0 pF	$1/2t_{SCK} - 2$	$1/2t_{SCK} + 2$	ns
			PCR[SRC]=01b	0 pF	$1/2t_{SCK} - 5$	$1/2t_{SCK} + 5$	ns
SOUT data valid time (after SCK edge)							
9	t_{SUO}	SOUT data valid time from SCK CPHA = 1[8]	PCR[SRC]=11b	25 pF	—	7.0	ns
			PCR[SRC]=10b	50 pF	—	8.0	ns
			PCR[SRC]=01b	50 pF	—	18.0	ns
SOUT data hold time (after SCK edge)							
10	t_{HO}	SOUT data hold time after SCK CPHA = 1[8]	PCR[SRC]=11b	25 pF	–9.0	—	ns
			PCR[SRC]=10b	50 pF	–10.0	—	ns
			PCR[SRC]=01b	50 pF	–21.0	—	ns

1. TSB = 1 or ITSB = 1 automatically selects MTFE = 1 and CPHA = 1.
2. All output timing is worst case and includes the mismatching of rise and fall times of the output pads.
3. When a characteristic involves two signals, the pad drive and load conditions apply to each signal's pad, unless specified otherwise.
4. All timing values for output signals in this table are measured to 50% of the output voltage.

A more accurate two-resistor thermal model can be constructed from the junction-to-board thermal resistance and the junction-to-case thermal resistance. The junction-to-case thermal resistance describes when using a heat sink or where a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit board. This model can be used to generate simple estimations and for computational fluid dynamics (CFD) thermal models. More accurate compact Flotherm models can be generated upon request.

To determine the junction temperature of the device in the application on a prototype board, use the thermal characterization parameter (Ψ_{JT}) to determine the junction temperature by measuring the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} x P_D)$$

where:

T_T = thermocouple temperature on top of the package (°C)

Ψ_{JT} = thermal characterization parameter (°C/W)

P_D = power dissipation in the package (W)

The thermal characterization parameter is measured in compliance with the JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. Position the thermocouple so that the thermocouple junction rests on the package. Place a small amount of epoxy on the thermocouple junction and approximately 1 mm of wire extending from the junction. Place the thermocouple wire flat against the package case to avoid measurement errors caused by the cooling effects of the thermocouple wire.

When board temperature is perfectly defined below the device, it is possible to use the thermal characterization parameter (Ψ_{JPB}) to determine the junction temperature by measuring the temperature at the bottom center of the package case (exposed pad) using the following equation:

$$T_J = T_B + (\Psi_{JPB} x P_D)$$

where:

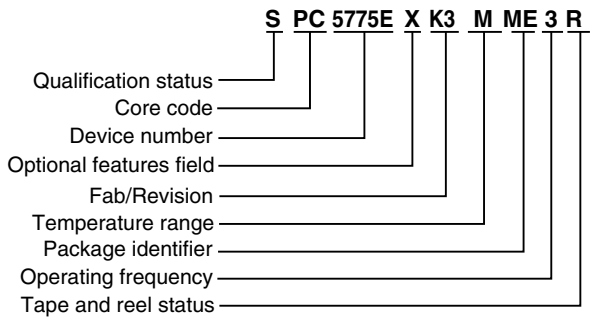
T_T = thermocouple temperature on bottom of the package (°C)

Ψ_{JT} = thermal characterization parameter (°C/W)

P_D = power dissipation in the package (W)

5 Ordering information

Figure 42 and Table 51 describe orderable part numbers for the MPC5775B and MPC5775E.



Device Number
MPC5775B or MPC5775E

Temperature range
M = –40 °C to 125 °C

Package identifier
ME = 416 MAPBGA Pb-Free

Tape and reel status
R = Tape and reel
(blank) = Trays

Qualification status
S = Fully spec. qualified, automotive flow

Operating frequency
3 = 264 MHz
2= 220 MHz

Optional features field
D = ISO-compliant CAN FD available, trimmed for SMPS or external regulator, and include SHE compliant security firmware

Figure 42. MPC5775B and MPC5775E Orderable part number description

Table 51. Example orderable part numbers

Part number	Package description	Speed (MHz)	Operating temperature[1]	
			Min (T_L)	Max (T_H)
SPC5775BDK3MME2	SPC5775B 416 package Lead-free (Pb-free)	220	–40 °C	125 °C
SPC5775EDK3MME3	SPC5775E 416 package Lead-free (Pb-free)	264	–40 °C	125 °C

1. The lowest ambient operating temperature is referenced by T_L; the highest ambient operating temperature is referenced by T_H.

6 Document revision history

The following table summarizes revisions to this document since the previous release.

Table 52. Revision history

Revision	Date	Description of changes
1	05/2018	Initial release

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Document Number MPC5775E
Revision 1, 05/2018