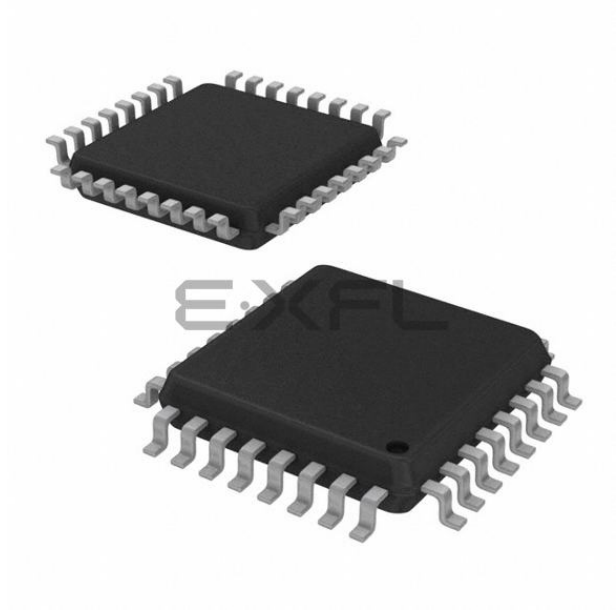

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, Motor Control PWM, POR, PWM, WDT
Number of I/O	30
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 5.5V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z32f06423ake

Registers

The base address of the PCU block is 0x4000_1000.

Register access is globally masked by the PORTEN register. To change register values except the PORTEN register, enable port access in advance.

Table 5-2 Base Address of Each Port Control

NAME	BASE ADDRESS
PCA	0x4000_1000
PCB	0x4000_1100
PCC	0x4000_1200
PCD	0x4000_1300

Table 5-3 PCU Register Map

NAME	OFFSET	TYPE	DESCRIPTION
PC*n*.MR	0x--00	RW	Port *n* pin mux select register
PC*n*.CR	0x--04	RW	Port *n* pin control register
PC*n*.PCR	0x--08	RW	Port *n* internal pull-up control register
PC*n*.DER	0x--0C	RW	Port *n* debounce control register
PC*n*.IER	0x--10	RW	Port *n* interrupt enable register
PC*n*.ISR	0x--14	RW	Port *n* interrupt status register
PC*n*.ICR	0x--18	RW	Port *n* interrupt control register
	0x--1C		Reserved
PORTEN	0x1FF0	RW	Port Access enable

PCC.CR PORT C Pin Control Register

This register is used for input or output control of each port pin. Each pin can be configured as input pin, output pin, or open-drain pin.

PCC.CR=0x4000_1204

31 30	29 28	27 26	25 24	23 22	21 20	19 18	17 16	15 14	13 12	11 10	9 8	7 6	5 4	3 2	1 0
P15	P14	P13	P12	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	P0
11	11	11	11	10	10	11	11	11	11	11	11	11	11	10	10
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Pn	Port control
00	Push-pull output
01	Open-drain output
10	Input
11	Analog

PCn.PCR PORT n Pull-up Resistor Control Register (Except for PCC.PCR)

Every pin in the port has on-chip pull-up resistors which can be configured by the PCn.PCR registers.

PCA.PCR=0x4000_1008, PCB.PCR=0x4000_1108
PCD.PCR=0x4000_1308

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PUE15	PUE14	PUE13	PUE12	PUE11	PUE10	PUE9	PUE8	PUE7	PUE6	PUE5	PUE4	PUE3	PUE2	PUE1	PUE0
0000															
RW															

n	PUEn	Port pull-up control
0		Disable pull-up resistor
1		Enable pull-up resister

FM.DIRTY Flash Memory Dirty Bit Register

FMDRTY is the internal Flash memory dirty bit clear register.

FM.DR=0x4000_0110

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FDIRTY																															
0x0000_0000																															
WO																															

31 0	FDIRTY	Write any value here, cache line fill flag will be cleared

FM.TICKFlash Memory Tick Timer Register

This is an internal Flash memory tick timer register.

FM.TICK=0x4000_011C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
														FTICK																	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x00000																	
								RW																							

17 0	FTICK	TICK goes to 0x3FFFF from written TICK value while TMR runs by PCLK clock while Flash PGM or ERS (counts up only when IDLE bit of FMMR register is low)

FM.CRC Flash CRC Check Register

FMCRC is the CRC value resulting from read accesses on internal Flash memory.

FM.CRC=0x4000_012C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																CRC16															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x00000															
																RW															

15 0	CRC16	CRC16 check value read register polynomial: (1 + x5 + x12 + x16) data width: 32 (the first serial bit is D[31])

Functional Description

The Flash memory controller is an internal Flash memory interface controller which primarily controls the programming of Flash memory and preparing read data to be requested from the bus.

Flash Organization

The 64 Kbytes code Flash memory consists of 512 pages which have a uniform 128 byte page size. The Flash controller allows reading or writing of Flash memory data. This memory is located at 0x0000_0000 address on the system memory map. The system expects the code to be executed on boot to be located at address 0x0000_0000. There is no ability to change this address on the Cortex M0.

Flash Read Operation

The Flash data read operation is requested from the bus. The Flash controller responds to the request. The wait time should be correctly defined because the bus speed is usually faster than the Flash data access time. The Flash data access time is 20 Mhz on the Z32F0642 device.

Flash Program Operation

Erase and Program access of Flash memory is available only in Flash mode. Once in Flash mode, Flash cannot be read normally; therefore, self-programming is not supported. The Flash program erase operations must be performed by the execution program in SRAM memory.

For every erase operation, a pre-program operation MUST be performed first, to prevent over-erase of Flash memory cells. Programming and erase operations use the 40 Mhz internal oscillator, so the HSI internal oscillator must be enabled and selected.

Erase operations can be either a page (32 words) or the entire chip. Programming can be a single word or a page.

Flash Erase and Program Examples

To erase a sector:

A. Flash mode enable to write FM.CR register (write 0x5A and then write 0xA5 into FMMR)
B. Set PMODE bit first
C. Wait until IDLE bit of FM.MR register becomes “1”
D. Set target Page address in FM.AR
E. Set FM.TMR register to be 0.5ms operation (based on 40MHz Int OSC clock)
F. set PPGM, WE, PGM bits of FMCR
G. Wait until IDLE bit of FM.MR register become “1” after pre-program
H. Clear WE, PGM bits of FMCR
I. Wait 5us
J. Clear PPGM bit of FM.CR
K. Wait 30us before returning to normal operation
L. Clear PMODE bit of FM.CR
M. Clear Flash mode (write 0x00 into FM.MR)
N. Insert at least 2 NOPs, and return to normal operation
O. Flash mode enable to write FM.CR register (write 0x5A and then write 0xA5 into FM.MR)
P. Set PMODE bit first

WDT.CON Watchdog Timer Control Register

The WDT module should be configured properly before running. When the target purpose is defined, WDT can be configured in the WDTCON register.

WDT.CON=0x4000_0208

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WDBG							WUF	WDTIE	WDTRE		WDTEN	CKSEL	WPRS		
1	0	0	0	0	0	0	0	0	1	0	1	1	100		
RW							RW	RW	RW		RW	RW	RW		

15	WDBG	Watchdog operation control in debug mode	
		0	Watchdog counter running when debug mode
		1	Watchdog counter stopped when debug mode
8	WUF	Watchdog timer underflow flag	
		0	No underflow
		1	Underflow is pending
7	WDTIE	Watchdog timer counter underflow interrupt enable	
		0	Disable interrupt
		1	Enable interrupt
6	WDTRE	Watchdog timer counter underflow interrupt enable	
		0	Disable reset
		1	Enable reset
4	WDTEN	Watchdog Counter enable	
		0	Watch dog counter disabled
		1	Watch dog counter enabled
3	CKSEL	WDTCLKIN clock source select	
		0	PCLK
		1	External clock
2 0	WPRS[2:0]	Counter clock prescaler WDTCLK = WDTCLKIN/WPRS	
		000	WDTCLKIN
		001	WDTCLKIN / 4
		010	WDTCLKIN / 8
		011	WDTCLKIN / 16
		100	WDTCLKIN / 32
		101	WDTCLKIN / 64
		110	WDTCLKIN / 128
		111	WDTCLKIN / 256

Functional Description

The watchdog timer count can be enabled by setting WDTEN (WDT.CON[4]) to '1'. As the watchdog timer is enabled, the down counter starts counting from the Load Value. If WDTRE (WDT.CON[6]) is set as '1', WDT reset will be asserted when the WDT counter value reaches '0' (underflow event) from the WDT.LR value. Before the WDT counter goes down to 0, the software can write a certain value to the WDT.LR register to reload the WDT counter.

Timing Diagram

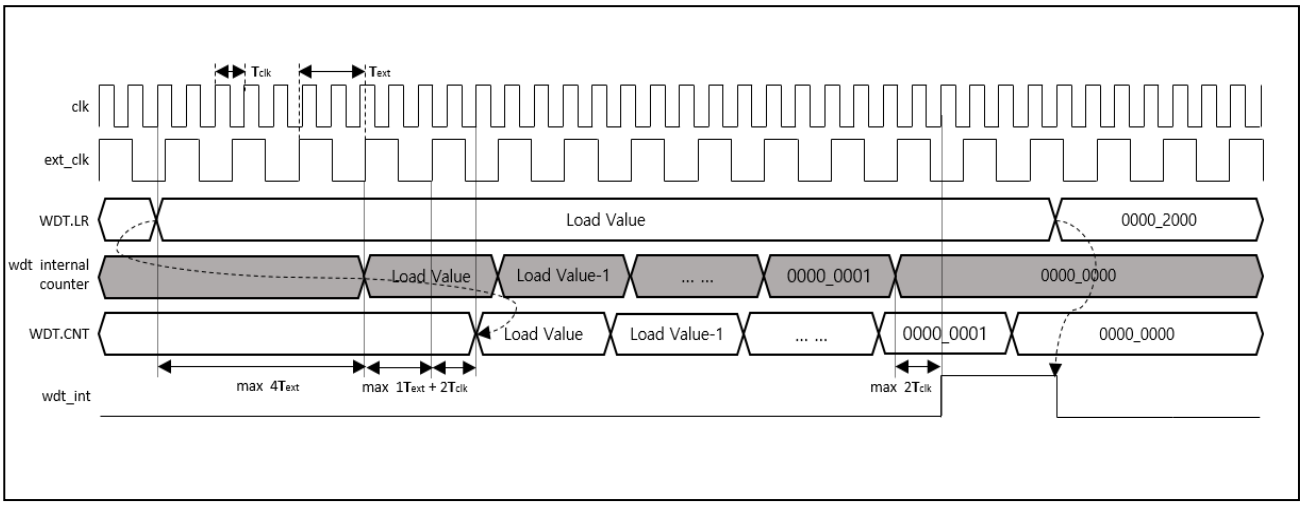


Figure 9-2 Timing Diagram in Interrupt Mode Operation when WDT Clock is External Clock

In WDT interrupt mode, after WDT underflow occurs, a certain count value is reloaded to prevent the next WDT interrupt in a short time period and this reloading action can only be activated when the watchdog timer counter is set to be in Interrupt mode (set WDTIE of WDT.CON). It takes up to 5 cycles from the Load value to the CNT value. The WDT interrupt signal and CNT value data might be delayed by a maximum of 2 system bus clocks in synchronous logic.

Prescale Table

The WDT includes a 32-bit down counter with programmable pre-scaler to define different time-out intervals.

The clock sources of the watchdog timer include the peripheral clock (PCLK) or one of five external clock sources. An external clock source can be enabled by setting CKSEL (WDT.CON[3]) to '1'. The external clock source is chosen in the MCCR3 register of the SCU (system control unit) block.

To make the WDT counter base clock, users can control 3-bit pre-scaler WPRS [2:0] in the WDT.CON register and the maximum pre-scaled value is "clock source frequency/256". The pre-scaled WDT counter clock frequency values are listed in following table.

Selectable clock source (40 kHz ~ 16 MHz) and the time out interval when 1 count

Time out period = {(Load Value) * (1/pre-scaled WDT counter clock frequency) + max 5Text} + max 4Tclk

*Time out period (time out period from load Value to interrupt set '1')

Functional Description

Timer Basic Operation

TMCLK in Figure 10-2 is a reference clock for operation of the timer. This clock is divided by the prescaler setting for the counting clock to work. Figure 10-2 shows the starting point of the counter and the ending of the period point of the counter in normal periodic mode.

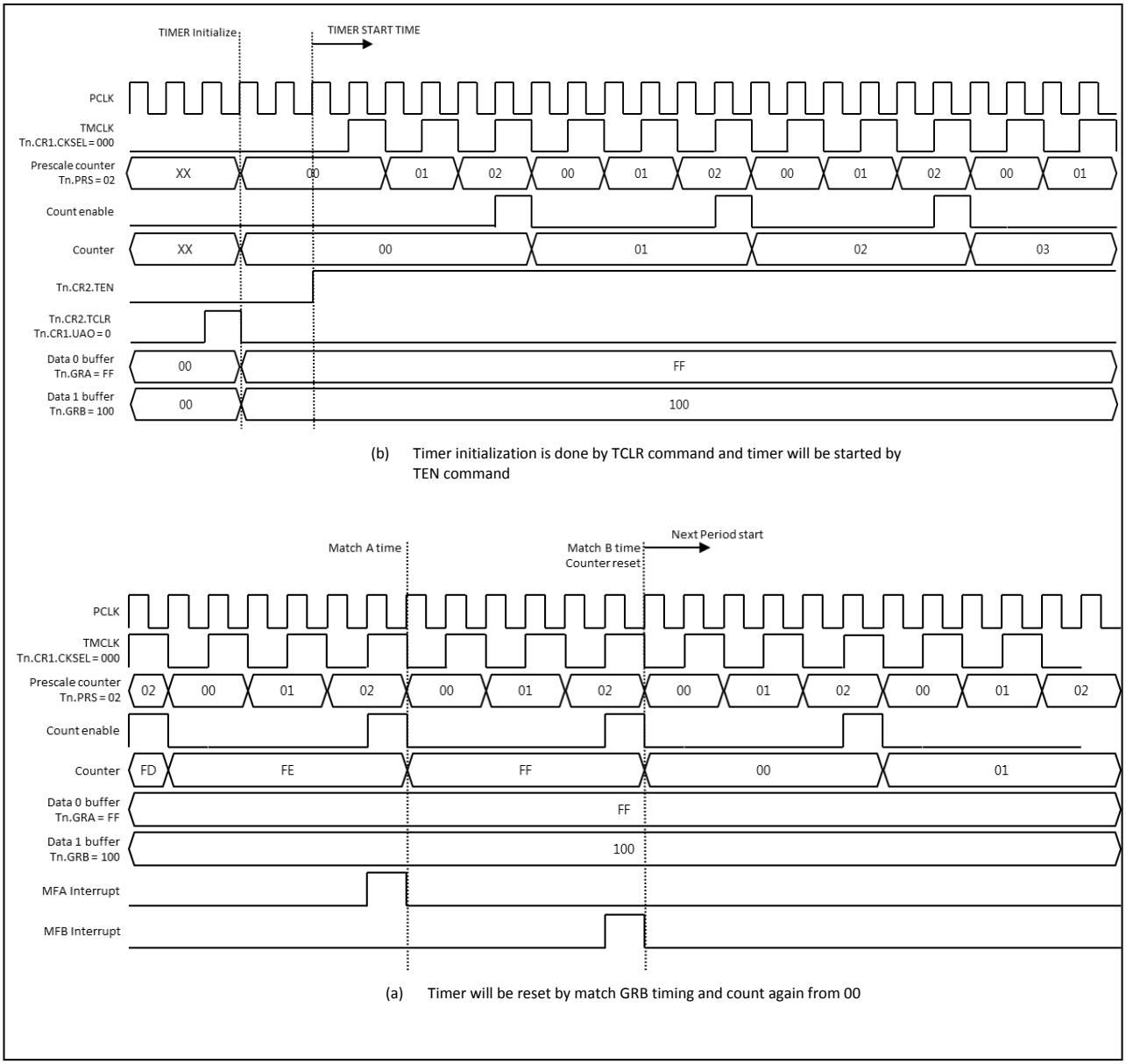


Figure 10-2 Basic Start and Match Operation

The period of timer count can be calculated using the following equation:

The period = TMCLK Period * Tn.GRB value.

Match A interrupt time = TMCLK Period * Tn.GRA value.

Registers

The base address of UART is 0x4000_8000 and the register map is described in Table 12-2 and Table 12-3.

Table 12-2 Base Address of Each Port

NAME	BASE ADDRESS
U0	0x4000_8000
U1	0x4000_8100

Table 12-3 UART Register Map

NAME	OFFSET	TYPE	DESCRIPTION	RESET VALUE
Un.RBR	0x00	R	Receive Data Buffer Register	0x00
Un.THR	0x00	W	Transmit Data Hold Register	0x00
Un.IER	0x04	RW	Interrupt Enable Register	0x00
Un.IIR	0x08	R	Interrupt ID Register	0x01
-	0x08	-	Reserved	-
Un.LCR	0x0C	RW	Line Control Register	0x00
Un.DCR	0x10	RW	Data Control Register	
Un.LSR	0x14	R	Line Status Register	0x00
-	0x18	-	Reserved	-
Un.SCR	0x1C	RW	Scratch Pad Register	0x00
Un.BDR	0x20	RW	Baud rate Divisor Latch Register	0x0000
Un.BFR	0x24	RW	Baud rate Fractional Counter Value	0x00
Un.IDTR	0x30	RW	Inter-frame Delay Time Register	0x80

Un.RBR Receive Buffer Register

The UART Receive Buffer register is an 8-bit read-only register. Received data is read out from this register. The maximum length of data is 8 bits. The last data received will be maintained in this register until a new byte is received.

U0.RBR=0x4000_8000, U1.RBR=0x4000_8100

7	6	5	4	3	2	1	0
RBR[7:0]							
-							
RO							

7 0	RBR	Receive Buffer Register

Un.BFR Baud Rate Fraction Counter Register

The Baud Rate Fraction Counter register is an 8-bit register.

U0.BFR=0x4000_8024, U1.BFR=0x4000_8124

7	6	5	4	3	2	1	0
BFR							
0x00							
RW							

7 0	BFR	Fractions counter value.	
		0	Fraction counter is disabled
		N	Fraction counter enabled. Fraction compensation mode is operating. Fraction counter is incremented by FCNT.

Table 12-7 Example of Baud Rate Calculation

$UART_{clock}$ =40 MHz			
Baud rate	**Divider**	**FCNT**	**Error (%)**
1200	2083	85	0.00%
2400	1041	170	0.00%
4800	520	213	0.00%
9600	260	106	0.00%
19200	130	53	0.00%
38400	65	262	0.00%
57600	43	103	0.00%
115200	21	179	0.01%

$$\mathrm{FCNT} = \mathrm{Float} * 256$$

The FCNT value is calculated using the equation above. For example, when the target baud rate is 4800 bps and $UART_{clock}$ is 40MHz, the BDR value is 520.8333. The integer number 520 should be the BDR value and the floating number 0.8333 will result in the FCNT value of 213, as shown below:

FCNT = 0.8333 * 256 = 213.3333, so the FCNT value is 213.

The 8-bit fractional counter will count up by FCNT value every (baud rate)/16 periods and when the fractional counter overflows, the divisor value increments by 1. Therefore, this period will be compensated. In the next period, the divisor value will return to the original set value.

Pin Description

Table 14-1 I²C Interface External Pins

PIN NAME	TYPE	DESCRIPTION
SCL	I/O	I²C channel Serial clock bus line (open-drain)
SDA	I/O	I²C channel Serial data bus line (open-drain)

Registers

The base address of I²C is 0x4000_A000. The register map is described in Table 14-2 and Table 14-3.

Table 14-2 I²C Interface Base Address

NAME	BASE ADDRESS
I²C	0x4000_A000

Table 14-3 I²C Register Map

NAME	OFFSET	TYPE	DESCRIPTION	RESET VALUE
IC.DR	0x00	RW	I²C Data Register	0xFF
IC.SR	0x08	R, RW	I²C Status Register	0x00
IC.SAR	0x0C	RW	I²C Slave Address Register	0x00
IC.CR	0x14	RW	I²C Control Register	0x00
IC.SCLL	0x18	RW	I²C SCL LOW duration Register	0xFFFF
IC.SCLH	0x1C	RW	I²C SCL HIGH duration Register	0xFFFF
IC.SDH	0x20	RW	I²C SDA Hold Register	0x7F

15. Motor Pulse Width Modulator (MPWM)

Overview

Motor Pulse Width Modulator (MPWM) is a programmable motor controller which is optimized for 3-phase AC and DC motor control applications. It can be used in many other applications that require timing, counting, and comparison features.

MPWM includes 3 channels, each of which controls a pair of outputs that can control a motor.

- 16-bit counter
- 6-channel outputs for motor control
- Dead-time support
- Protection event and over voltage event handling
- 6 ADC trigger outputs
- Interval interrupt mode (period interrupt only)
- Up-down count mode

The MPWM clock source which is MPWM counter clock source will be provided from the SCU block. The MPWM resolution and period will be defined by this MPWM clock configuration. The default MPWM clock is the same as the RINGOSC clock. Prior to enabling the MPWM module, proper MPWM clock selection is required.

Registers

The base address of MPWM is shown in Table 15-2.

Table 15-2 MPWM Base Address

NAME	BASE ADDRESS
MPWM	0x4000_4000

Table 15-3 shows the register memory map.

Table 15-3 MPWM Register Map

NAME	OFFSET	TYPE	DESCRIPTION	RESET VALUE
MP.MR	0x0000	RW	MPWM Mode register	0x0000_0000
MP.OLR	0x0004	RW	MPWM Output Level register	0x0000_0000
MP.FOR	0x0008	RW	MPWM Force Output register	0x0000_0000
MP.PRD	0x000C	RW	MPWM Period register	0x0000_0002
MP.DUH	0x0010	RW	MPWM Duty UH register	0x0000_0001
MP.DVH	0x0014	RW	MPWM Duty VH register	0x0000_0001
MP.DWH	0x0018	RW	MPWM Duty WH register	0x0000_0001
MP.DUL	0x001C	RW	MPWM Duty UL register	0x0000_0001
MP.DVL	0x0020	RW	MPWM Duty VL register	0x0000_0001
MP.DWL	0x0024	RW	MPWM Duty WL register	0x0000_0001
MP.CR1	0x0028	RW	MPWM Control register 1	0x0000_0000
MP.CR2	0x002C	RW	MPWM Control register 2	0x0000_0000
MP.SR	0x0030	R	MPWM Status register	0x0000_0000
MP.IER	0x0034	RW	MPWM Interrupt Enable	0x0000_0000
MP.CNT	0x0038	R	MPWM counter register	0x0000_0001
MP.DTR	0x003C	RW	MPWM dead time control	0x0000_0000
MP.PCR0	0x0040	RW	MPWM protection 0 control register	0x0000_0000
MP.PSR0	0x0044	RW	MPWM protection 0 status register	0x0000_0080
MP.PCR1	0x0048	RW	MPWM protection 1 control register	0x0000_0000
MP.PSR1	0x004C	RW	MPWM protection 1 status register	0x0000_0000
-	0x0054	-	Reserved	-
MP.ATR1	0x0058	RW	MPWM ADC Trigger reg1	0x0000_0000
MP.ATR2	0x005C	RW	MPWM ADC Trigger reg2	0x0000_0000
MP.ATR3	0x0060	RW	MPWM ADC Trigger reg3	0x0000_0000
MP.ATR4	0x0064	RW	MPWM ADC Trigger reg4	0x0000_0000
MP.ATR5	0x0068	RW	MPWM ADC Trigger reg5	0x0000_0000
MP.ATR6	0x006C	RW	MPWM ADC Trigger reg6	0x0000_0000

MP.CR1 MPWM Control Register 1

The PWM Control Register 1 is a 16-bit register.

MP.CR1=0x4000_4028

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
					IRQN										PWMEN
					000				0	0	0	0	0	0	0
					RW										RW

10 8	IRQN	IRQ interval number (Every 1~8th PRDIRQ,BOTIRQ,ATRn)
0	PWMEN	PWM enable When this bit set 0, the PWM block stay in reset state but user interface can be accessed. To operate the PWM block, this bit should be set 1.

Basically, PRDIRQ and BOTIRQ are generated every period. However, the interrupt interval can be controlled from 0 to 8 periods. When IRQN.CR1 = 0, the interrupt is requested every period, otherwise the interrupt is requested every (IRQN+1) times of period.

MP.CR2 MPWM Control Register 2

The PWM Control Register 2 is an 8-bit register.

MP.CR2=0x4000_402C

7	6	5	4	3	2	1	0
HALT							PSTART
0	0	0	0	0	0	0	0
RW							RW

7	HALT	PWM HALT (PWM counter stop but not reset) PWM outputs keep previous state	
0	PSTART	0	PWM counter stop and clear
		1	PWM counter start (will be resynced @PWM clock twice) PWMEN should be “1” to start PWM counter

MP.PCRn MPWM Protection 0,1 Control Register

The PWM Protection Control register is a 16-bit register.

MP.PCR0=0x4000_4040, MP.PCR1=0x4000_4048

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROTEN	PROTPOL				PROTD			PROTIE		WHPROTM	VHPROTM	UHPROTM	WLPROTM	VLPROTM	ULPROTM
0	0				000			0		0	0	0	0	0	0
RW	RW				RW			RW		RW	RW	RW	RW	RW	RW

15	PROT0EN	Enable Protection Input 0
14	PROT0POL	Select Protection Input Polarity 0: Low-Active 1: High-Active
10 8	PROTD	Protection Input debounce 0 – no debounce 1~7 – debounce by (MPWMCLK * PROTD[2:0])
7	PROTIE	Protection Interrupt enable 0 Disable protection interrupt 1 Enable protection interrupt
5	WHPROTM	Activate W-phase H-side protection output 0 Disable Protection Output 1 Enable Protection Output with FOR value
4	VHPROTM	Activate V-phase H-side protection output 0 Disable Protection Output 1 Enable Protection Output with FOR value
3	UHPROTM	Activate U-phase H-side protection output 0 Disable Protection Output 1 Enable Protection Output with FOR value
2	WLPROTM	Activate W-phase L-side protection output 0 Disable Protection Output 1 Enable Protection Output with FOR value
1	VLPROTM	Activate V-phase L-side protection output 0 Disable Protection Output 1 Enable Protection Output with FOR value
0	ULPROTM	Activate U-phase L-side protection output 0 Disable Protection Output 1 Enable Protection Output with FOR value

Note: MP.PCR0 is related to the PRTIN pin and MP.PCR1 is related to OVIN.

Description of ADC Triggering Function

A total of six ADC trigger timing registers are provided. This dedicated register triggers a signal to start ADC conversion. The conversion channel of ADC is defined in the ADC Control register.

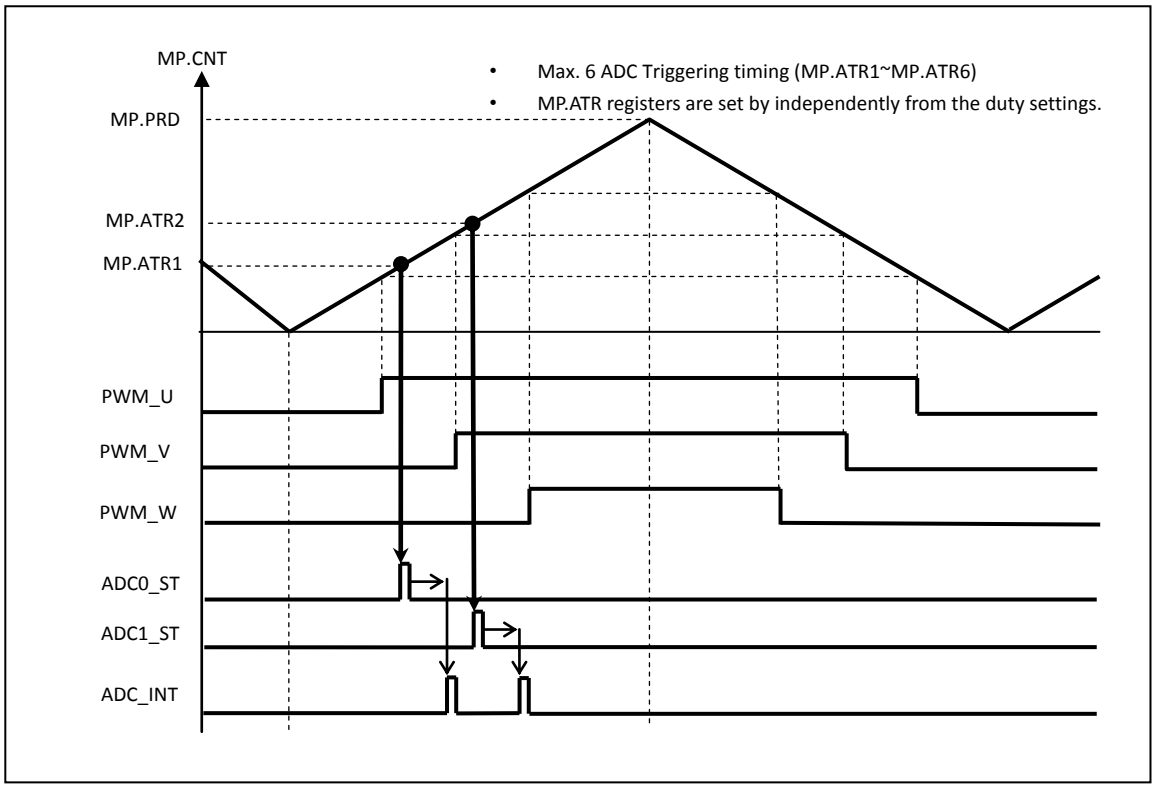


Figure 15-16 ADC Triggering Function Timing Diagram

16. Divider (DIV64)

Overview

The divider module provides the hardware divider the ability to accelerate complicated calculations. This divider is a sequential 64-bit/32-bit divider and requires 32 clock cycles for one operation.

The equation for this operation is:

(AREGH,AREGL)/BREG = (QREGH,QREGL)

- Unsigned 64-bit dividend
- Unsigned 32-bit divisor
- Unsigned 64-bit quotient
- Unsigned 32-bit remainder
- Unsigned 32-cycle operating time

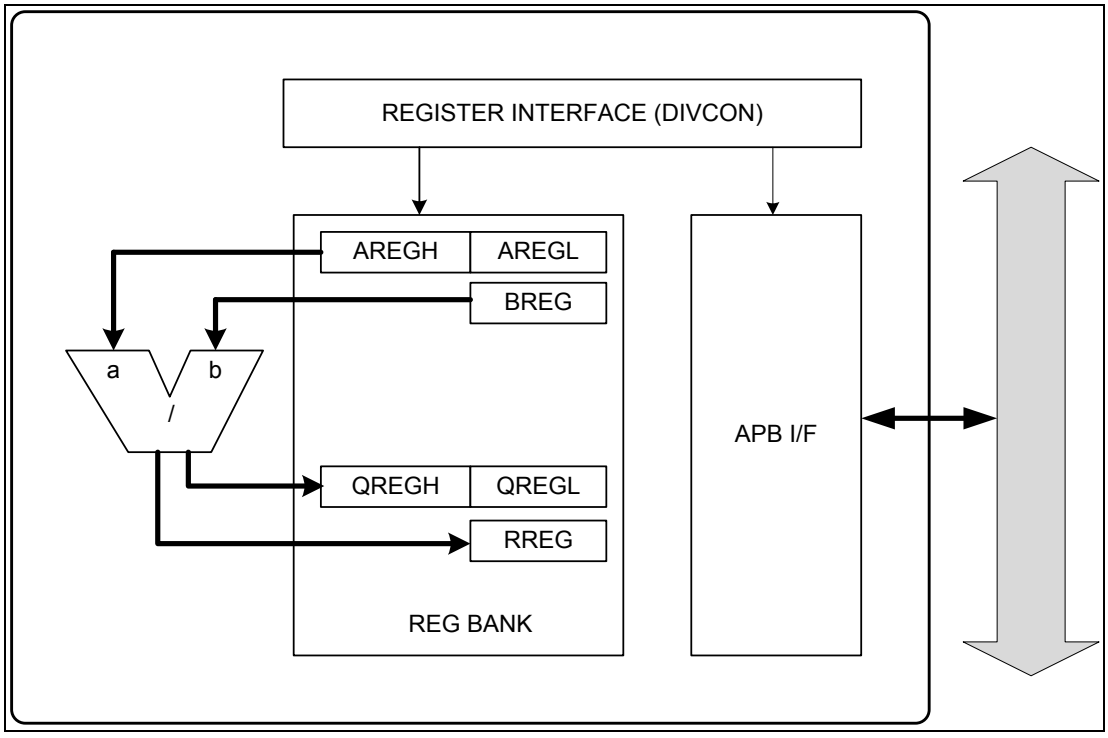


Figure 16-1 Block Diagram

QREGL QREG (Quotient) Lower 32-bit Register

The divider stores the lower 32-bit value of the quotient in this register.

QREGL=0x4000_0510

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
QREGL[31:0]																															
0x0000_0000																															
R																															

31 0	QREGL	Lower 32 bit value for quotient.

QREGH QREG (Quotient) High 32-bit Register

The divider stores the high 32-bit value of the quotient in this register.

QREGH=0x4000_0514

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
QREGH[63:32]																															
0x0000_0000																															
R																															

31 0	QREGH	High 32 bit value for quotient.

RREG RREG (Remainter) Register

The divider stores the 32-bit value of the remainder in this register.

RREG=0x4000_0518

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RREG[31:0]																															
0x0000_0000																															
R																															

31 0	RREG	32 bit value for remainder.

ADC Sequential Conversion Mode Timing Diagram

Single Sequential Conversion mode (Single Sequential mode) occurs when AD.MR.ADMOD is 0x0 and AD.MR.SEQCNT is not 0x0. To set Sequential Conversion mode, AD.MR.AMOD is 2'b00 and AD.MR.SEQCNT is not 2'b00.

The operation of Sequential mode is almost the same as the Burst mode. The difference is the source of SOC. Each SOC is made by the trigger of SEQTRGx as each SEQCNT. See Figure 17-5.

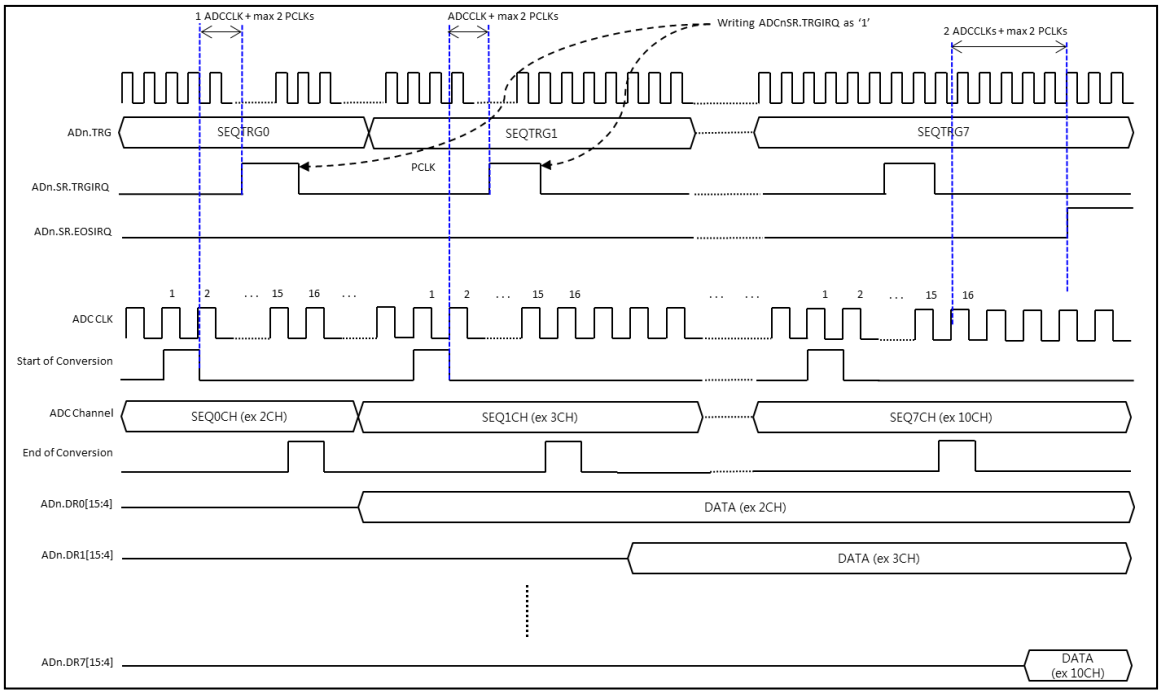


Figure 17-5 ADC Sequential Mode Timing (When AD.MR.AMOD = ó0 and AD.MR.SEQCNT Í ó0ô

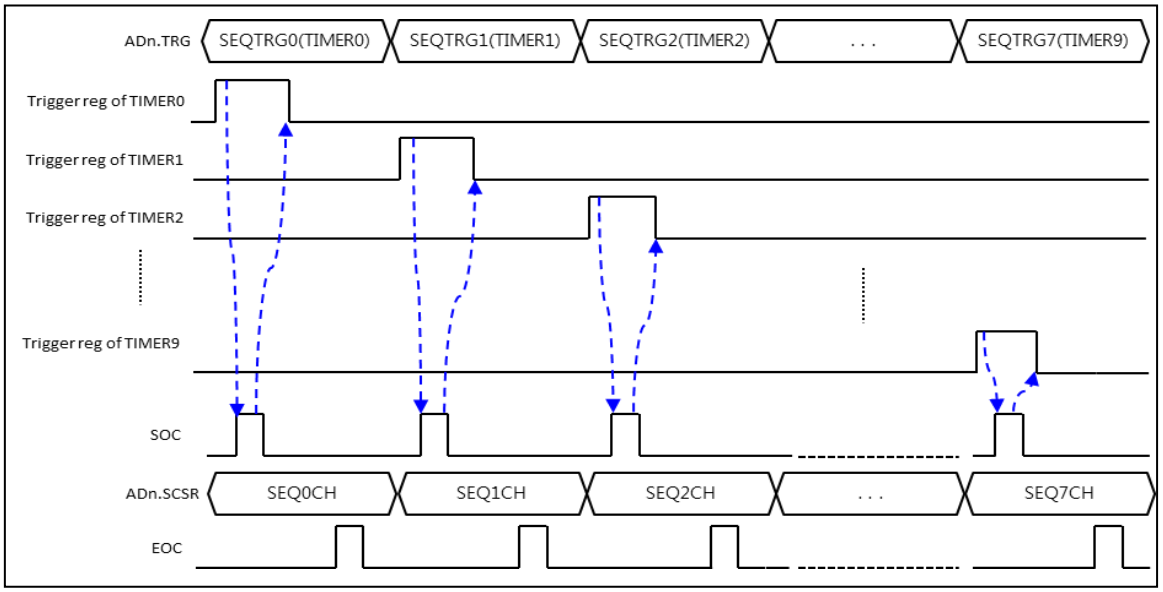


Figure 17-6 ADC Trigger Timing in Sequential Mode (SEQCNT = 3ô111, 8 Sequence Coversion)

18. Electrical Characteristics

DC Characteristics

Absolute Maximum Ratings

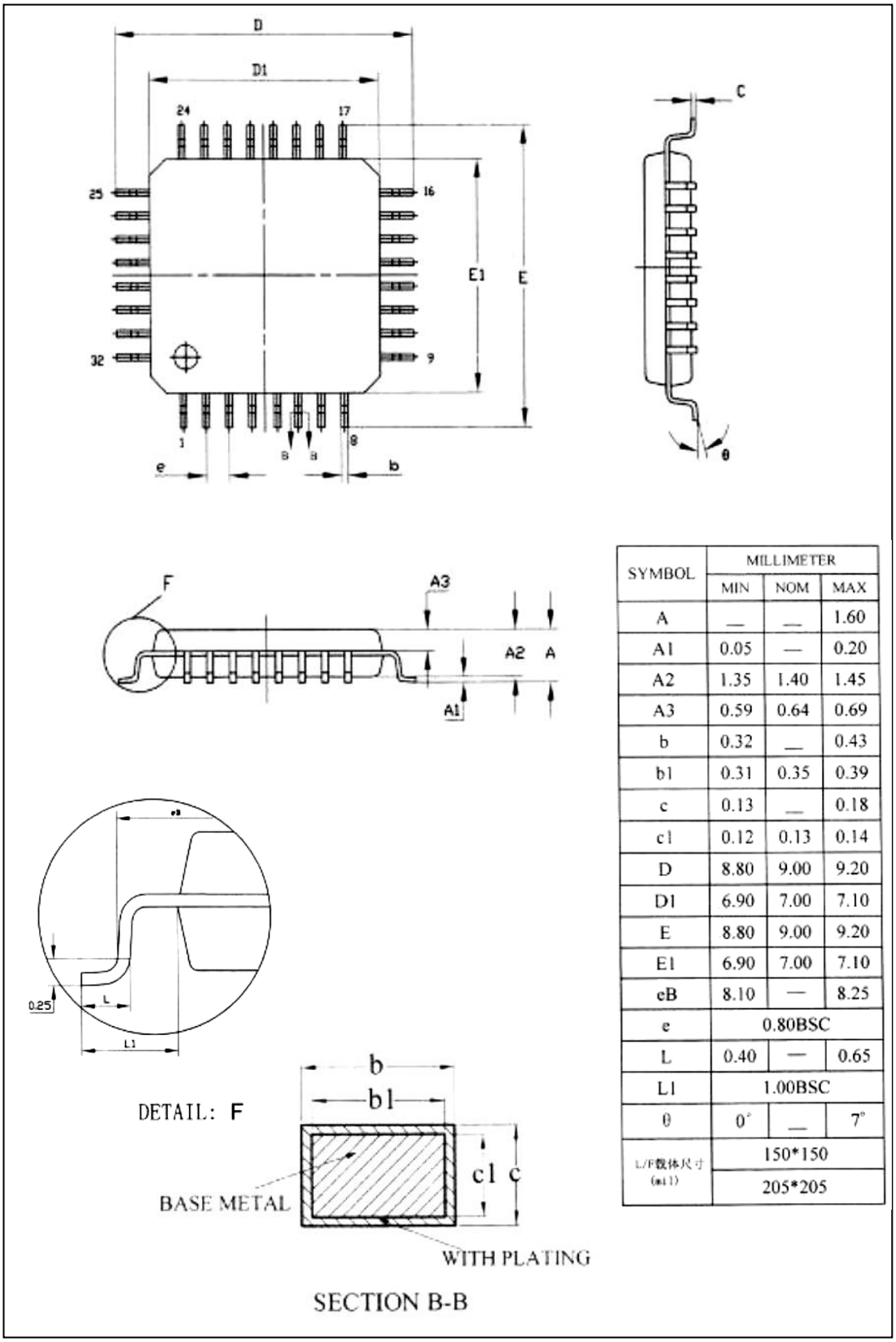
Absolute maximum ratings are limiting values of operating and environmental conditions which should not be exceeded under the worst possible conditions.

Table 18-1 Absolute Maximum Rating

Parameter	Symbol	Min	Max	Unit
Power Supply (VDD)	VDD	-0.5	+6	V
Analog Power Supply (AVDD)	AVDD	-0.5	+6	V
VDC Output Voltage	VDD18			V
Input High Voltage		-	VDD+0.5	V
Input Low Voltage		VSS – 0.5	-	V
Output Low Current per pin	I_{OL}		5	mA
Output Low Current Total	$\sum I_{OL}$		40	mA
Output High Current per pin	I_{OH}		5	mA
Output Low Current Total	$\sum I_{OH}$		40	mA
Power consumption				mW
Input Main Clock Range		4	16	MHz
Operating Frequency		-	40	MHz
Storage Temperature	Tst	-55	+125	℃
Operating Temperature	Top	-40	+105	℃

19. Package

LQFP-32 Package Dimension



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	—	0.20
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.32	—	0.43
b1	0.31	0.35	0.39
c	0.13	—	0.18
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
eB	8.10	—	8.25
e	0.80BSC		
L	0.40	—	0.65
L1	1.00BSC		
θ	0°	—	7°
L/F载体尺寸 (mil)	150*150		
	205*205		