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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Not For New Designs
Core Processor	M32C/80
Core Size	16/32-Bit
Speed	32MHz
Connectivity	CANbus, I ² C, IEBus, SIO, UART/USART
Peripherals	DMA, WDT
Number of I/O	85
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 26x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m30853fhgp-u5

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1.4 Product Information

Table 1.3 lists the product information. Figure 1.2 shows the product numbering system.

Table 1.3 M32C/85 Group (1) (M32C/85)

As of July, 2005

Type Number	Package Type	ROM Capacity	RAM Capacity	Remarks
M30855FJGP	PLQP0144KA-A (144P6Q-A)	512K+4K	24K	Flash Memory
M30853FJGP	PLQP0100KB-A (100P6Q-A)			
M30853FJFP	PRQP0100JB-A (100P6S-A)			
M30855FHGP	PLQP0144KA-A (144P6Q-A)	384K+4K		
M30853FHGP	PLQP0100KB-A (100P6Q-A)			
M30853FHFP	PRQP0100JB-A (100P6S-A)			
M30855FWGP	PLQP0144KA-A (144P6Q-A)	320K+4K		
M30853FWGP	PLQP0100KB-A (100P6Q-A)			
M30853FWFP	PRQP0100JB-A (100P6S-A)			
M30855MW-XXXGP	PLQP0144KA-A (144P6Q-A)	320K		Mask ROM
M30853MW-XXXGP	PLQP0100KB-A (100P6Q-A)			
M30853MW-XXXFP	PRQP0100JB-A (100P6S-A)			

Table 1.3 M32C/85 Group (2) (T Version, M32C/85T)

As of July, 2005

Type Number	Package Type	ROM Capacity	RAM Capacity	Remarks
M30855FJTGP	PLQP0144KA-A (144P6Q-A)	512K+4K	24K	Flash Memory T Version (High-reliability 85°C Version)
M30853FJTGP	PLQP0100KB-A (100P6Q-A)			
M30855FHTGP	PLQP0144KA-A (144P6Q-A)	384K+4K		
M30853FHTGP	PLQP0100KB-A (100P6Q-A)			
M30855FWTGP	PLQP0144KA-A (144P6Q-A)	320K+4K		
M30853FWTGP	PLQP0100KB-A (100P6Q-A)			

Table 1.4 Pin Characteristics for 144-Pin Package (Continued)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin ⁽¹⁾
97		P24					AN24	A4(/D4)
98		P23					AN23	A3(/D3)
99		P22					AN22	A2(/D2)
100		P21					AN21	A1(/D1)
101		P20					AN20	A0(/D0)
102		P17	INT5					D15
103		P16	INT4					D14
104		P15	INT3					D13
105		P14						D12
106		P13						D11
107		P12						D10
108		P11						D9
109		P10						D8
110		P07					AN07	D7
111		P06					AN06	D6
112		P05					AN05	D5
113		P04					AN04	D4
114		P114						
115		P113				INPC13/OUTC13		
116		P112				INPC12/OUTC12/ISRxD1/BE1IN		
117		P111				INPC11/OUTC11/ISCLK1		
118		P110				INPC10/OUTC10/ISTxD1/BE1OUT		
119		P03					AN03	D3
120		P02					AN02	D2
121		P01					AN01	D1
122		P00					AN00	D0
123		P157					AN157	
124		P156					AN156	
125		P155					AN155	
126		P154					AN154	
127		P153					AN153	
128		P152				ISRxD0	AN152	
129		P151				ISCLK0	AN151	
130	Vss							
131		P150				ISTxD0	AN150	
132	VCC1							
133		P107	KI3				AN7	
134		P106	KI2				AN6	
135		P105	KI1				AN5	
136		P104	KI0				AN4	
137		P103					AN3	
138		P102					AN2	
139		P101					AN1	
140	AVss							
141		P100					AN0	
142	VREF							
143	AVCC							
144		P97			RxD4/SCL4/STxD4		ADTRG	

NOTES:

1. Bus control pins in M32C/85T cannot be used,

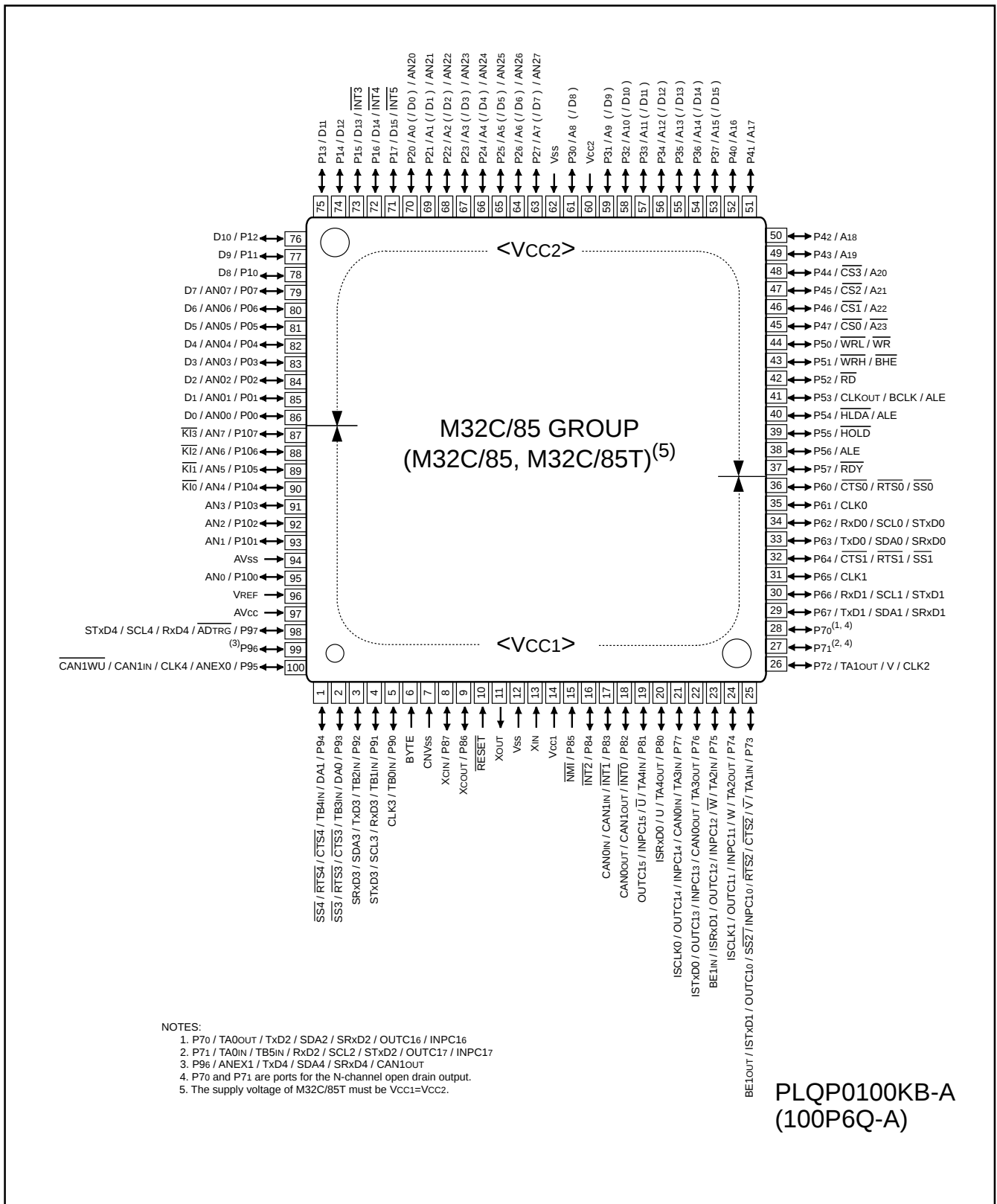


Figure 1.4 Pin Assignment for 100-Pin Package

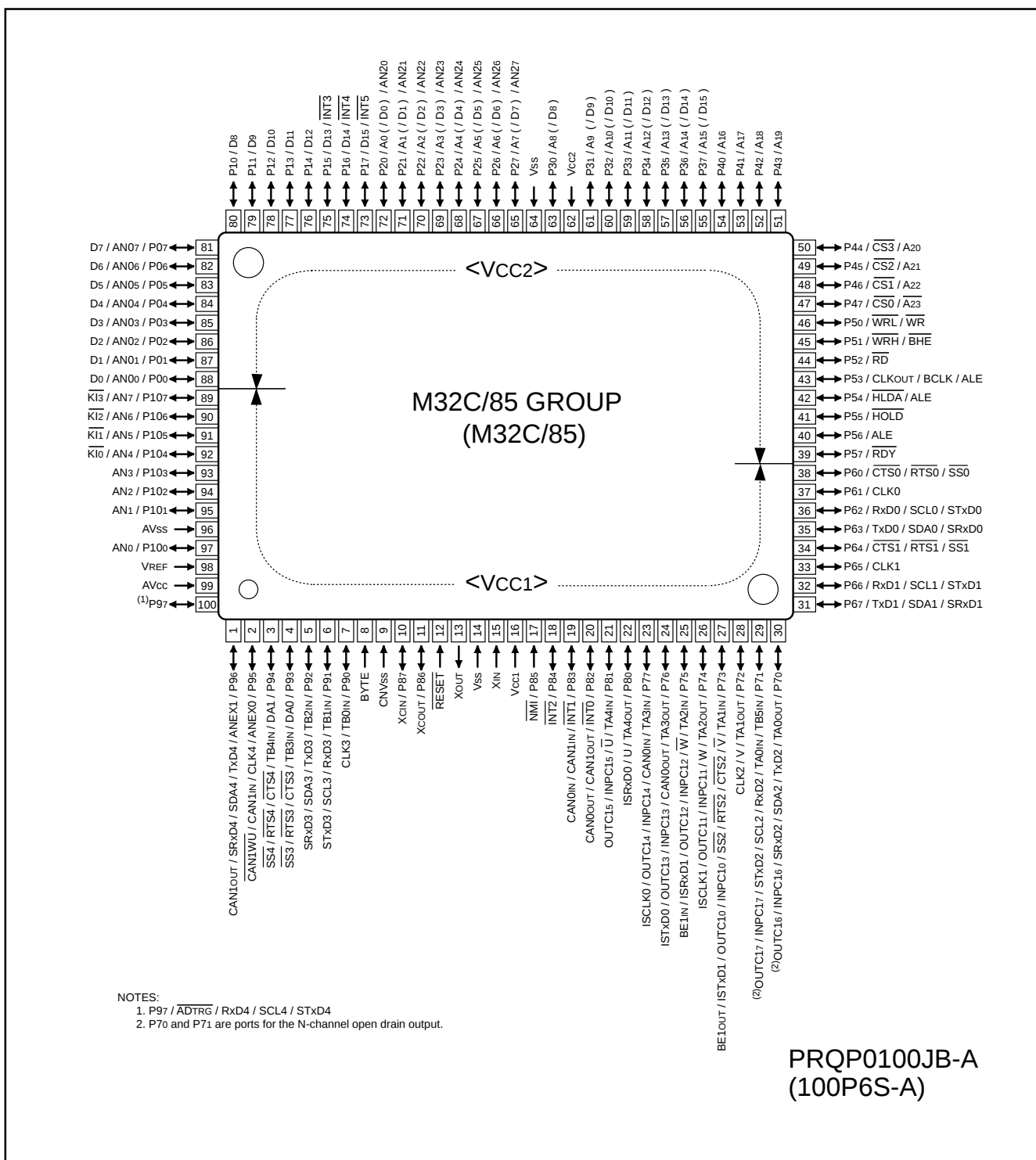


Figure 1.5 Pin Assignment for 100-Pin Package

1.6 Pin Description

Table 1.6 Pin Description (100-Pin and 144-Pin Packages)

Classification	Symbol	I/O Type	Supply Voltage	Function
Power Supply	VCC1, VCC2 VSS	I	–	Apply 3.0 to 5.5V to both VCC1 and VCC2 pins. Apply 0V to the VSS pin. $V_{CC1} \geq V_{CC2}^{(1, 2)}$
Analog Power Supply	AVCC AVSS	I	VCC1	Supplies power to the A/D converter. Connect the AVCC pin to VCC1 and the AVSS pin to VSS
Reset Input	RESET	I	VCC1	The microcomputer is in a reset state when "L" is applied to the RESET pin
CNVss	CNVss	I	VCC1	Switches processor mode. Connect the CNVss pin to VSS to start up in single-chip mode or to VCC1 to start up in microprocessor mode
Input to Switch External Data Bus Width ⁽³⁾	BYTE	I	VCC1	Switches data bus width in external memory space 3. The data bus is 16 bits wide when the BYTE pin is held "L" and 8 bits wide when it is held "H". Set to either. Connect the BYTE pin to VSS to use the microcomputer in single-chip mode
Bus Control Pins ⁽³⁾	D0 to D7	I/O	VCC2	Inputs and outputs data (D0 to D7) while accessing an external memory space with separate bus
	D8 to D15	I/O	VCC2	Inputs and outputs data (D8 to D15) while accessing an external memory space with 16-bit separate bus
	A0 to A22	O	VCC2	Outputs address bits A0 to A22
	A23	O	VCC2	Outputs inversed address bit A23
	A0/D0 to A7/D7	I/O	VCC2	Inputs and outputs data (D0 to D7) and outputs 8 low-order address bits (A0 to A7) by time-sharing while accessing an external memory space with multiplexed bus
	A8/D8 to A15/D15	I/O	VCC2	Inputs and outputs data (D8 to D15) and outputs 8 middle-order address bits (A8 to A15) by time-sharing while accessing an external memory space with 16-bit multiplexed bus
	CS0 to CS3	O	VCC2	Outputs CS0 to CS3 that are chip-select signals specifying an external space
	WRL / WR WRH / BHE RD	O	VCC2	Outputs WRL, WRH, (WR, BHE) and RD signals. WRL and WRH can be switched with WR and BHE by program ■ WRL, WRH and RD selected: If external data bus is 16 bits wide, data is written to an even address in external memory space when WRL is held "L". Data is written to an odd address when WRH is held "L". Data is read when RD is held "L". ■ WR, BHE and RD selected: Data is written to external memory space when WR is held "L". Data in an external memory space is read when RD is held "L". An odd address is accessed when BHE is held "L". Select WR, BHE and RD for external 8-bit data bus.
	ALE	O	VCC2	ALE is a signal latching the address
	HOLD	I	VCC2	The microcomputer is placed in a hold state while the HOLD pin is held "L"
	HLDA	O	VCC2	Outputs an "L" signal while the microcomputer is placed in a hold state
	RDY	I	VCC2	Bus is placed in a wait state while the RDY pin is held "L"

I : Input O : Output I/O : Input and output

NOTES:

1. VCC1 is hereinafter referred to as VCC unless otherwise noted.
2. Apply 4.2 to 5.5V to the VCC1 and VCC2 pins when using M32C/85T. $V_{CC1}=V_{CC2}$.
3. Bus control pins in M32C/85T cannot be used.

Table 1.6 Pin Description (100-Pin and 144-Pin Packages) (Continued)

Classsification	Symbol	I/O Type	Supply Voltage	Function
Main Clock Input	XIN	I	VCC1	I/O pins for the main clock oscillation circuit. Connect a ceramic resonator or crystal oscillator between XIN and XOUT. To apply external clock, apply it to XIN and leave XOUT open
Main Clock Output	XOUT	O	VCC1	
Sub Clock Input	XCIN	I	VCC1	I/O pins for the sub clock oscillation circuit. Connect a crystal oscillator between XCIN and XCOUT. To apply external clock, apply it to XCIN and leave XCOUT open
Sub Clock Output	XCOUT	O	VCC1	
BCLK Output ⁽¹⁾	BCLK	O	VCC2	Outputs BCLK signal
Clock Output	CLKOUT	O	VCC2	Outputs the clock having the same frequency as fc, f8 or f32
INT Interrupt Input	INT0 to INT2	I	VCC1	Input pins for the INT interrupt
	INT3 to INT5		VCC2	
NMI Interrupt Input	NMI	I	VCC1	Input pin for the NMI interrupt
Key Input Interrupt	KI0 to KI3	I	VCC1	Input pins for the key input interrupt
Timer A	TA0OUT to TA4OUT	I/O	VCC1	I/O pins for the timer A0 to A4 (TA0OUT is a pin for the N-channel open drain output.)
	TA0IN to TA4IN	I	VCC1	Input pins for the timer A0 to A4
Timer B	TB0IN to TB5IN	I	VCC1	Input pins for the timer B0 to B5
Three-phase Motor Control Timer Output	U, $\bar{U}$, V, $\bar{V}$, W, $\bar{W}$	O	VCC1	Output pins for the three-phase motor control timer
Serial I/O	CTS0 to CTS4	I	VCC1	Input pins for data transmission control
	RTS0 to RTS4	O	VCC1	Output pins for data reception control
	CLK0 to CLK4	I/O	VCC1	Inputs and outputs the transfer clock
	RxD0 to RxD4	I	VCC1	Inputs serial data
	TxD0 to TxD4	O	VCC1	Outputs serial data (TxD2 is a pin for the N-channel open drain output.)
I ² C Mode	SDA0 to SDA4	I/O	VCC1	Inputs and outputs serial data (SDA2 is a pin for the N-channel open drain output.)
	SCL0 to SCL4			Inputs and outputs the transfer clock (SCL2 is a pin for the N-channel open drain output.)
Serial I/O Special Function	STxD0 to STxD4	O	VCC1	Outputs serial data when slave mode is selected (STxD2 is a pin for the N-channel open drain output.)
	SRxD0 to SRxD4	I		Inputs serial data when slave mode is selected
	SS0 to SS4	I	VCC1	Input pins to control serial I/O special function

I : Input O : Output I/O : Input and output

NOTES:

1. Bus control pins in M32C/85T cannot be used.

Address	Register	Symbol	Value after RESET
0120 ₁₆ 0121 ₁₆	Base Timer Register 1	G1BT	XX ₁₆ XX ₁₆
0122 ₁₆	Base Timer Control Register 10	G1BCR0	00 ₁₆
0123 ₁₆	Base Timer Control Register 11	G1BCR1	X000 000X ₂
0124 ₁₆	Time Measurement Prescaler Register 16	G1TPR6	00 ₁₆
0125 ₁₆	Time Measurement Prescaler Register 17	G1TPR7	00 ₁₆
0126 ₁₆	Function Enable Register 1	G1FE	00 ₁₆
0127 ₁₆	Function Select Register 1	G1FS	00 ₁₆
0128 ₁₆ 0129 ₁₆	SI/O Receive Buffer Register 1	G1RB	XXXX XXXX ₂ X000 XXXX ₂
012A ₁₆ 012B ₁₆	Transmit Buffer/Receive Data Register 1	G1TB/G1DR	XX ₁₆
012C ₁₆	Receive Input Register 1	G1RI	XX ₁₆
012D ₁₆	SI/O Communication Mode Register 1	G1MR	00 ₁₆
012E ₁₆	Transmit Output Register 1	G1TO	XX ₁₆
012F ₁₆	SI/O Communication Control Register 1	G1CR	0000 X011 ₂
0130 ₁₆	Data Compare Register 10	G1CMP0	XX ₁₆
0131 ₁₆	Data Compare Register 11	G1CMP1	XX ₁₆
0132 ₁₆	Data Compare Register 12	G1CMP2	XX ₁₆
0133 ₁₆	Data Compare Register 13	G1CMP3	XX ₁₆
0134 ₁₆	Data Mask Register 10	G1MSK0	XX ₁₆
0135 ₁₆	Data Mask Register 11	G1MSK1	XX ₁₆
0136 ₁₆			
0137 ₁₆			
0138 ₁₆ 0139 ₁₆	Receive CRC Code Register 1	G1RCRC	XX ₁₆ XX ₁₆
013A ₁₆ 013B ₁₆	Transmit CRC Code Register 1	G1TCRC	00 ₁₆ 00 ₁₆
013C ₁₆	SI/O Extended Mode Register 1	G1EMR	00 ₁₆
013D ₁₆	SI/O Extended Receive Control Register 1	G1ERC	00 ₁₆
013E ₁₆	SI/O Special Communication Interrupt Detection Register 1	G1IRF	00 ₁₆
013F ₁₆	SI/O Extended Transmit Control Register 1	G1ETC	0000 0XXX ₂
0140 ₁₆			
0141 ₁₆			
0142 ₁₆			
0143 ₁₆			
0144 ₁₆			
0145 ₁₆			
0146 ₁₆			
0147 ₁₆			
0148 ₁₆			
0149 ₁₆			
014A ₁₆			
014B ₁₆			
014C ₁₆			
014D ₁₆			
014E ₁₆			
014F ₁₆			

X: Indeterminate

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Address	Register	Symbol	Value after RESET
0210 ₁₆	CAN0 Slot Interrupt Mask Register	C0SIMKR	00 ₁₆ ⁽²⁾
0211 ₁₆			00 ₁₆ ⁽²⁾
0212 ₁₆			
0213 ₁₆			
0214 ₁₆	CAN0 Error Interrupt Mask Register	C0EIMKR	XXXX X000 ₂ ⁽²⁾
0215 ₁₆	CAN0 Error Interrupt Status Register	C0EISTR	XXXX X000 ₂ ⁽²⁾
0216 ₁₆	CAN0 Error Cause Register	C0EFR	00 ₁₆ ⁽²⁾
0217 ₁₆	CAN0 Baud Rate Prescaler	C0BRP	0000 0001 ₂ ⁽²⁾
0218 ₁₆			
0219 ₁₆	CAN0 Mode Register	C0MDR	XXXX XX00 ₂ ⁽²⁾
021A ₁₆			
021B ₁₆			
021C ₁₆			
021D ₁₆			
021E ₁₆			
021F ₁₆			
0220 ₁₆	CAN0 Single Shot Control Register	C0SSCTLR	00 ₁₆ ⁽²⁾
0221 ₁₆			00 ₁₆ ⁽²⁾
0222 ₁₆			
0223 ₁₆			
0224 ₁₆	CAN0 Single Shot Status Register	C0SSSTR	00 ₁₆ ⁽²⁾
0225 ₁₆			00 ₁₆ ⁽²⁾
0226 ₁₆			
0227 ₁₆			
0228 ₁₆	CAN0 Global Mask Register Standard ID0	C0GMR0	XXX0 0000 ₂ ⁽²⁾
0229 ₁₆	CAN0 Global Mask Register Standard ID1	C0GMR1	XX00 0000 ₂ ⁽²⁾
022A ₁₆	CAN0 Global Mask Register Extended ID0	C0GMR2	XXXX 0000 ₂ ⁽²⁾
022B ₁₆	CAN0 Global Mask Register Extended ID1	C0GMR3	00 ₁₆ ⁽²⁾
022C ₁₆	CAN0 Global Mask Register Extended ID2	C0GMR4	XX00 0000 ₂ ⁽²⁾
022D ₁₆			
022E ₁₆			
022F ₁₆			
0230 ₁₆	CAN0 Message Slot 0 Control Register / CAN0 Local Mask Register A Standard ID0	C0MCTL0/ C0LMAR0	0000 0000 ₂ ⁽²⁾ XXX0 0000 ₂ ⁽²⁾
0231 ₁₆	CAN0 Message Slot 1 Control Register / CAN0 Local Mask Register A Standard ID1	C0MCTL1/ C0LMAR1	0000 0000 ₂ ⁽²⁾ XX00 0000 ₂ ⁽²⁾
0232 ₁₆	CAN0 Message Slot 2 Control Register / CAN0 Local Mask Register A Extended ID0	C0MCTL2/ C0LMAR2	0000 0000 ₂ ⁽²⁾ XXXX 0000 ₂ ⁽²⁾
0233 ₁₆	CAN0 Message Slot 3 Control Register / CAN0 local Mask Register A Extended ID1	C0MCTL3/ C0LMAR3	00 ₁₆ ⁽²⁾ 00 ₁₆ ⁽²⁾
0234 ₁₆	CAN0 Message Slot 4 Control Register / CAN0 Local Mask Register A Extended ID2	C0MCTL4/ C0LMAR4	0000 0000 ₂ ⁽²⁾ XX00 0000 ₂ ⁽²⁾
0235 ₁₆	CAN0 Message Slot 5 Control Register	C0MCTL5	00 ₁₆ ⁽²⁾
0236 ₁₆	CAN0 Message Slot 6 Control Register	C0MCTL6	00 ₁₆ ⁽²⁾
0237 ₁₆	CAN0 Message Slot 7 Control Register	C0MCTL7	00 ₁₆ ⁽²⁾
0238 ₁₆	CAN0 Message Slot 8 Control Register / CAN0 Local Mask Register B Standard ID0	C0MCTL8/ C0LMBR0	0000 0000 ₂ ⁽²⁾ XXX0 0000 ₂ ⁽²⁾
0239 ₁₆	CAN0 Message Slot 9 Control Register / CAN0 Local Mask Register B Standard ID1	C0MCTL9/ C0LMBR1	0000 0000 ₂ ⁽²⁾ XX00 0000 ₂ ⁽²⁾

(Note 1)

X: Indeterminate

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NOTES:

1. The BANKSEL bit in the C0CTLR1 register switches functions for addresses 0220₁₆ to 023F₁₆.
2. Values are obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) after reset and applying the clock to the CAN module.

Address	Register	Symbol	Value after RESET	
023A ₁₆	CAN0 Message Slot 10 Control Register / CAN0 Local Mask Register B Extended ID0	C0MCTL10/ C0LMBR2	0000 0000 ₂ ⁽²⁾ XXXX 0000 ₂ ⁽²⁾	(Note 1)
023B ₁₆	CAN0 Message Slot 11 Control Register / CAN0 Local Mask Register B Extended ID1	C0MCTL11/ C0LMBR3	00 ₁₆ ⁽²⁾ 00 ₁₆ ⁽²⁾	
023C ₁₆	CAN0 Message Slot 12 Control Register / CAN0 Local Mask Register B Extended ID2	C0MCTL12/ C0LMBR4	0000 0000 ₂ ⁽²⁾ XX00 0000 ₂ ⁽²⁾	
023D ₁₆	CAN0 Message Slot 13 Control Register	C0MCTL13	00 ₁₆ ⁽²⁾	
023E ₁₆	CAN0 Message Slot 14 Control Register	C0MCTL14	00 ₁₆ ⁽²⁾	
023F ₁₆	CAN0 Message Slot 15 Control Register	C0MCTL15	00 ₁₆ ⁽²⁾	
0240 ₁₆	CAN0 Slot Buffer Select Register	C0SBS	00 ₁₆ ⁽²⁾	
0241 ₁₆	CAN0 Control Register 1	C0CTLR1	X000 00XX ₂ ⁽²⁾	
0242 ₁₆	CAN0 Sleep Control Register	C0SLPR	XXXX XXX0 ₂	
0243 ₁₆				
0244 ₁₆ 0245 ₁₆	CAN0 Acceptance Filter Support Register	C0AFS	00 ₁₆ ⁽²⁾ 01 ₁₆ ⁽²⁾	
0246 ₁₆				
0247 ₁₆				
0248 ₁₆				
0249 ₁₆				
024A ₁₆				
024B ₁₆				
024C ₁₆				
024D ₁₆				
024E ₁₆				
024F ₁₆				
0250 ₁₆	CAN1 Slot Buffer Select Register	C1SBS	00 ₁₆ ⁽³⁾	
0251 ₁₆	CAN1 Control Register 1	C1CTLR1	X000 00XX ₂ ⁽³⁾	
0252 ₁₆	CAN1 Sleep Control Register	C1SLPR	XXXX XXX0 ₂	
0253 ₁₆				
0254 ₁₆ 0255 ₁₆	CAN1 Acceptance Filter Support Register	C1AFS	00 ₁₆ ⁽³⁾ 01 ₁₆ ⁽³⁾	
0256 ₁₆				
0257 ₁₆				
0258 ₁₆				
0259 ₁₆				
025A ₁₆				
025B ₁₆				
025C ₁₆				
025D ₁₆				
025E ₁₆				
025F ₁₆				

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTES:

1. The BANKSEL bit in the C0CTLR1 register switches functions for addresses 0220₁₆ to 023F₁₆.
2. Values are obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) after reset and applying the clock to the CAN module.
3. Values are obtained by setting the SLEEP bit in the C1SLPR register to "1" (sleep mode exited) after reset and applying the clock to the CAN module.

Address	Register	Symbol	Value after RESET
0260 ₁₆	CAN1 Message Slot Buffer 0 Standard ID0	C1SLOT0_0	XX ₁₆
0261 ₁₆	CAN1 Message Slot Buffer 0 Standard ID1	C1SLOT0_1	XX ₁₆
0262 ₁₆	CAN1 Message Slot Buffer 0 Extended ID0	C1SLOT0_2	XX ₁₆
0263 ₁₆	CAN1 Message Slot Buffer 0 Extended ID1	C1SLOT0_3	XX ₁₆
0264 ₁₆	CAN1 Message Slot Buffer 0 Extended ID2	C1SLOT0_4	XX ₁₆
0265 ₁₆	CAN1 Message Slot Buffer 0 Data Length Code	C1SLOT0_5	XX ₁₆
0266 ₁₆	CAN1 Message Slot Buffer 0 Data 0	C1SLOT0_6	XX ₁₆
0267 ₁₆	CAN1 Message Slot Buffer 0 Data 1	C1SLOT0_7	XX ₁₆
0268 ₁₆	CAN1 Message Slot Buffer 0 Data 2	C1SLOT0_8	XX ₁₆
0269 ₁₆	CAN1 Message Slot Buffer 0 Data 3	C1SLOT0_9	XX ₁₆
026A ₁₆	CAN1 Message Slot Buffer 0 Data 4	C1SLOT0_10	XX ₁₆
026B ₁₆	CAN1 Message Slot Buffer 0 Data 5	C1SLOT0_11	XX ₁₆
026C ₁₆	CAN1 Message Slot Buffer 0 Data 6	C1SLOT0_12	XX ₁₆
026D ₁₆	CAN1 Message Slot Buffer 0 Data 7	C1SLOT0_13	XX ₁₆
026E ₁₆	CAN1 Message Slot Buffer 0 Time Stamp High-Order	C1SLOT0_14	XX ₁₆
026F ₁₆	CAN1 Message Slot Buffer 0 Time Stamp Low-Order	C1SLOT0_15	XX ₁₆
0270 ₁₆	CAN1 Message Slot Buffer 1 Standard ID0	C1SLOT1_0	XX ₁₆
0271 ₁₆	CAN1 Message Slot Buffer 1 Standard ID1	C1SLOT1_1	XX ₁₆
0272 ₁₆	CAN1 Message Slot Buffer 1 Extended ID0	C1SLOT1_2	XX ₁₆
0273 ₁₆	CAN1 Message Slot Buffer 1 Extended ID1	C1SLOT1_3	XX ₁₆
0274 ₁₆	CAN1 Message Slot Buffer 1 Extended ID2	C1SLOT1_4	XX ₁₆
0275 ₁₆	CAN1 Message Slot Buffer 1 Data Length Code	C1SLOT1_5	XX ₁₆
0276 ₁₆	CAN1 Message Slot Buffer 1 Data 0	C1SLOT1_6	XX ₁₆
0277 ₁₆	CAN1 Message Slot Buffer 1 Data 1	C1SLOT1_7	XX ₁₆
0278 ₁₆	CAN1 Message Slot Buffer 1 Data 2	C1SLOT1_8	XX ₁₆
0279 ₁₆	CAN1 Message Slot Buffer 1 Data 3	C1SLOT1_9	XX ₁₆
027A ₁₆	CAN1 Message Slot Buffer 1 Data 4	C1SLOT1_10	XX ₁₆
027B ₁₆	CAN1 Message Slot Buffer 1 Data 5	C1SLOT1_11	XX ₁₆
027C ₁₆	CAN1 Message Slot Buffer 1 Data 6	C1SLOT1_12	XX ₁₆
027D ₁₆	CAN1 Message Slot Buffer 1 Data 7	C1SLOT1_13	XX ₁₆
027E ₁₆	CAN1 Message Slot Buffer 1 Time Stamp High-Order	C1SLOT1_14	XX ₁₆
027F ₁₆	CAN1 Message Slot Buffer 1 Time Stamp Low-Order	C1SLOT1_15	XX ₁₆
0280 ₁₆ 0281 ₁₆	CAN1 Control Register 0	C1CTLR0	XX01 0X01 ₂ ⁽¹⁾ XXXX 0000 ₂ ⁽¹⁾
0282 ₁₆ 0283 ₁₆	CAN1 Status Register	C1STR	0000 0000 ₂ ⁽¹⁾ X000 0X01 ₂ ⁽¹⁾
0284 ₁₆ 0285 ₁₆	CAN1 Extended ID Register	C1IDR	00 ₁₆ ⁽¹⁾ 00 ₁₆ ⁽¹⁾
0286 ₁₆ 0287 ₁₆	CAN1 Configuration Register	C1CONR	0000 XXXX ₂ ⁽¹⁾ 0000 0000 ₂ ⁽¹⁾
0288 ₁₆ 0289 ₁₆	CAN1 Time Stamp Register	C1TSR	00 ₁₆ ⁽¹⁾ 00 ₁₆ ⁽¹⁾
028A ₁₆	CAN1 Transmit Error Count Register	C1TEC	00 ₁₆ ⁽¹⁾
028B ₁₆	CAN1 Receive Error Count Register	C1REC	00 ₁₆ ⁽¹⁾
028C ₁₆ 028D ₁₆	CAN1 Slot Interrupt Status Register	C1SISTR	00 ₁₆ ⁽¹⁾ 00 ₁₆ ⁽¹⁾
028E ₁₆			
028F ₁₆			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTES:

1. Values are obtained by setting the SLEEP bit in the C1SLPR register to "1" (sleep mode exited) after reset and supplying the clock to the CAN module.

Address	Register	Symbol	Value after RESET
0370 ₁₆			
0371 ₁₆			
0372 ₁₆			
0373 ₁₆			
0374 ₁₆			
0375 ₁₆			
0376 ₁₆			
0377 ₁₆			
0378 ₁₆	DMA0 Request Source Select Register	DM0SL	0X00 0000 ₂
0379 ₁₆	DMA1 Request Source Select Register	DM1SL	0X00 0000 ₂
037A ₁₆	DMA2 Request Source Select Register	DM2SL	0X00 0000 ₂
037B ₁₆	DMA3 Request Source Select Register	DM3SL	0X00 0000 ₂
037C ₁₆	CRC Data Register	CRCD	XX ₁₆
037D ₁₆			XX ₁₆
037E ₁₆	CRC Input Register	CRCIN	XX ₁₆
037F ₁₆			
0380 ₁₆	A/D0 Register 0	AD00	XXXX XXXX ₂
0381 ₁₆			0000 0000 ₂
0382 ₁₆	A/D0 Register 1	AD01	XX ₁₆
0383 ₁₆			XX ₁₆
0384 ₁₆	A/D0 Register 2	AD02	XX ₁₆
0385 ₁₆			XX ₁₆
0386 ₁₆	A/D0 Register 3	AD03	XX ₁₆
0387 ₁₆			XX ₁₆
0388 ₁₆	A/D0 Register 4	AD04	XX ₁₆
0389 ₁₆			XX ₁₆
038A ₁₆	A/D0 Register 5	AD05	XX ₁₆
038B ₁₆			XX ₁₆
038C ₁₆	A/D0 Register 6	AD06	XX ₁₆
038D ₁₆			XX ₁₆
038E ₁₆	A/D0 Register 7	AD07	XX ₁₆
038F ₁₆			XX ₁₆
0390 ₁₆			
0391 ₁₆			
0392 ₁₆	A/D0 Control Register 4	AD0CON4	XXXX 00XX ₂
0393 ₁₆			
0394 ₁₆	A/D0 Control Register 2	AD0CON2	XX0X X000 ₂
0395 ₁₆	A/D0 Control Register 3	AD0CON3	XXXX X000 ₂
0396 ₁₆	A/D0 Control Register 0	AD0CON0	00 ₁₆
0397 ₁₆	A/D0 Control Register 1	AD0CON1	00 ₁₆
0398 ₁₆	D/A Register 0	DA0	XX ₁₆
0399 ₁₆			
039A ₁₆	D/A Register 1	DA1	XX ₁₆
039B ₁₆			
039C ₁₆	D/A Control Register	DACON	XXXX XX00 ₂
039D ₁₆			
039E ₁₆			
039F ₁₆			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

$$V_{CC1}=V_{CC2}=5V$$

Table 5.3 Electrical Characteristics

($V_{CC1}=V_{CC2}=4.2$ to $5.5V$, $V_{SS}=0V$ at $T_{opr}=-20$ to $85^{\circ}C$, $f(BCLK)=32MHz$ unless otherwise specified)

Symbol		Parameter	Condition	Standard			Unit	
				Min.	Typ.	Max.		
V _{OH}	Output High ("H") Voltage	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P110-P114, P120-P127, P130-P137	I _{OH} =-5mA	V _{CC2} -2.0		V _{CC2}	V	
		P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107, P140-P146, P150-P157 ⁽¹⁾	I _{OH} =-5mA	V _{CC1} -2.0		V _{CC1}		
		P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P110-P114, P120-P127, P130-P137	I _{OH} =-200μA	V _{CC2} -0.3		V _{CC2}	V	
		P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107,P140-P146, P150-P157 ⁽¹⁾	I _{OH} =-200μA	V _{CC1} -0.3		V _{CC1}		
		X _{OUT}	I _{OH} =-1mA	3.0		V _{CC1}	V	
		X _{COUT}	High Power	No load applied		2.5		V
			Low Power	No load applied		1.6		
V _{OL}	Output Low ("L") Voltage	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽¹⁾	I _{OL} =5mA			2.0	V	
		P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽¹⁾	I _{OL} =200μA			0.45	V	
		X _{OUT}	I _{OL} =1mA			2.0	V	
		X _{COUT}	High Power	No load applied		0		V
			Low Power	No load applied		0		
V _{T+} -V _{T-}	Hysteresis	HOLD, RDY, TA0IN-TA4IN, TB0IN-TB5IN, INT0-INT5, ADTRG, CTS0-CTS4, CLK0-CLK4, TA0OUT-TA4OUT, NMI, K10-K13, RxD0-RxD4, SCL0-SCL4, SDA0-SDA4		0.2		1.0	V	
		RESET		0.2		1.8	V	
I _{IH}	Input High ("H") Current	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽¹⁾ , X _{IN} , RESET, CNVSS, BYTE	V _I =5V			5.0	μA	
I _{IL}	Input Low ("L") Current	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽¹⁾ , X _{IN} , RESET, CNVSS, BYTE	V _I =0V			-5.0	μA	
R _{PULLUP}	Pull-up Resistance	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽¹⁾	V _I =0V	Flash Memory	30	50	167	kΩ
				Masked ROM	20	40	167	
R _{FXIN}	Feedback Resistance	X _{IN}				1.5		MΩ
R _{FXCIN}	Feedback Resistance	X _{CIN}				10		MΩ
V _{RAM}	RAM Standby Voltage	In stop mode			2.0			V

NOTES:

1. P11 to P15 are provided in the 144-pin package only.

$$V_{CC1}=V_{CC2}=5V$$

Table 5.4 A/D Conversion Characteristics ($V_{CC1}=V_{CC2}=AV_{CC}=V_{REF}=4.2$ to $5.5V$, $V_{SS}=AV_{SS}=0V$ at $T_{opr}=-20$ to $85^{\circ}C$, $f(BCLK) = 32MHz$ unless otherwise specified)

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min.	Typ.	Max.	
-	Resolution	$V_{REF}=V_{CC1}$			10	Bits
INL	Integral Nonlinearity Error	$V_{REF}=V_{CC1}=V_{CC2}=5V$ AN ₀ to AN ₇ , AN ₀₀ to AN ₀₇ , AN ₂₀ to AN ₂₇ , AN ₁₅₀ to AN ₁₅₇ , ANEX ₀ , ANEX ₁			±3	LSB
		External op-amp connection mode			±7	LSB
					±7	LSB
DNL	Differential Nonlinearity Error				±1	LSB
-	Offset Error				±3	LSB
-	Gain Error				±3	LSB
RLADDER	Resistor Ladder	$V_{REF}=V_{CC1}$	8		40	kΩ
t _{CONV}	10-bit Conversion Time ^(1, 2)		2.06			μs
t _{CONV}	8-bit Conversion Time ^(1, 2)		1.75			μs
t _{SAMP}	Sampling Time ⁽¹⁾		0.188			μs
V _{REF}	Reference Voltage		2		V _{CC1}	V
V _{IA}	Analog Input Voltage		0		V _{REF}	V

NOTES:

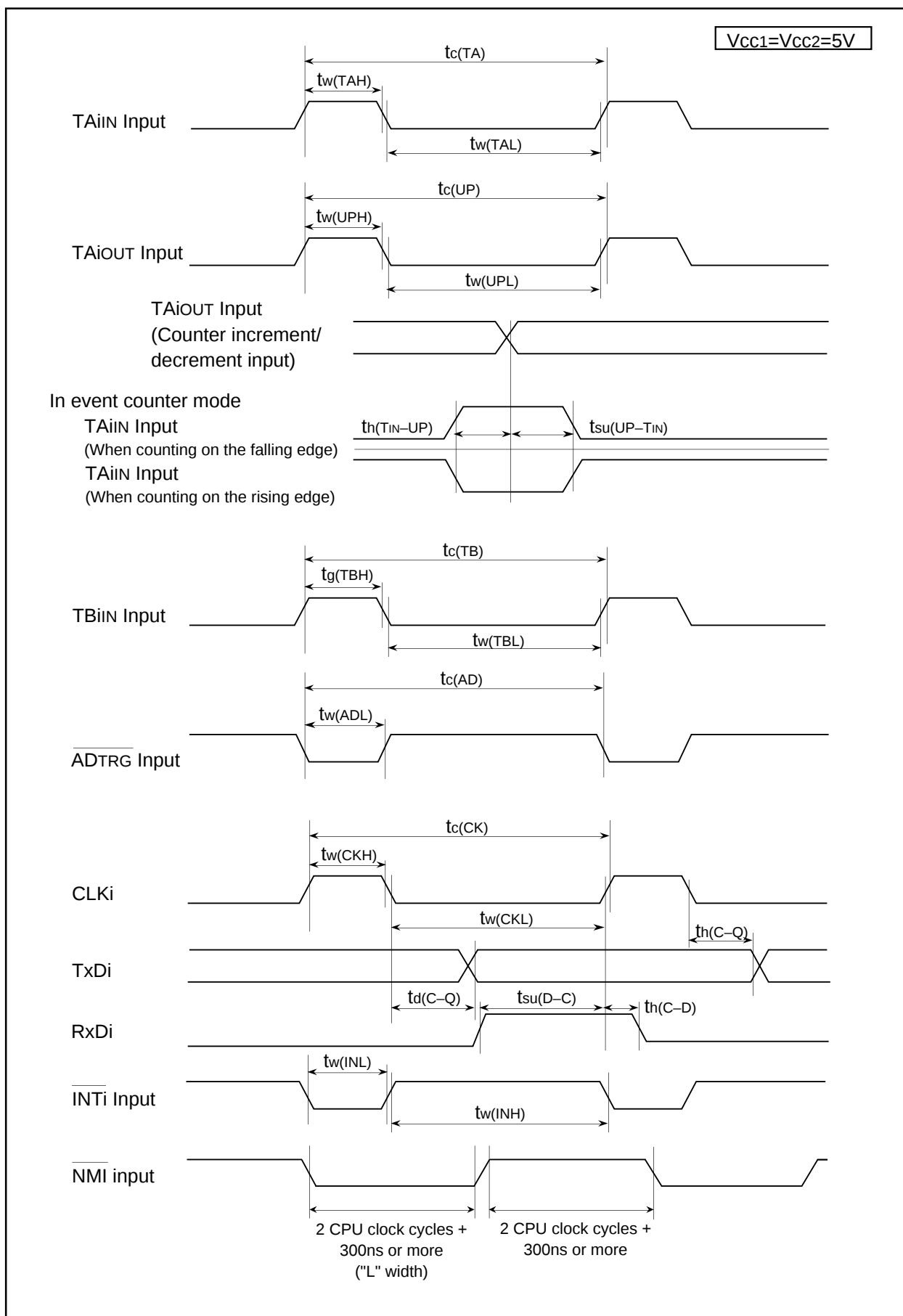
1. Divide f(X_{IN}), if exceeding 16 MHz, to keep φ_{AD} frequency at 16 MHz or less.
2. With using the sample and hold function.

Table 5.5 D/A Conversion Characteristics ($V_{CC1}=V_{CC2}=V_{REF}=4.2$ to $5.5V$, $V_{SS}=AV_{SS}=0V$ at $T_{opr}=-20$ to $85^{\circ}C$, $f(BCLK) = 32MHz$ unless otherwise specified)

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min.	Typ.	Max.	
-	Resolution				8	Bits
-	Absolute Accuracy				1.0	%
t _{SU}	Setup Time				3	μs
R _O	Output Resistance		4	10	20	kΩ
I _{VREF}	Reference Power Supply Input Current	(Note 1)			1.5	mA

NOTES:

1. Measurement when using one D/A converter. The DA_i register (i=0, 1) of the D/A converter, not being used, is set to "00₁₆". The resistor ladder in the A/D converter is excluded.
I_{VREF} flows even if the VCUT bit in the AD0CON1 register is set to "0" (no V_{REF} connection).

Figure 5.5 $V_{CC1}=V_{CC2}=5V$ Timing Diagram (3)

5.2 Electrical Characteristics (M32C/85T)

Table 5.42 Absolute Maximum Ratings

Symbol	Parameter		Condition	Value	Unit
V _{CC1} , V _{CC2}	Supply Voltage		V _{CC1} =V _{CC2} =AV _{CC}	-0.3 to 6.0	V
AV _{CC}	Analog Supply Voltage		V _{CC1} =V _{CC2} =AV _{CC}	-0.3 to 6.0	V
V _I	Input Voltage	RESET, CNV _{SS} , BYTE, P60-P67, P72-P77, P80-P87, P90-P97, P100-P107, P140-P146, P150-P157 ⁽¹⁾ , V _{REF} , X _{IN}		-0.3 to V _{CC1} +0.3	V
		P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P110-P114, P120-P127, P130-P137 ⁽¹⁾		-0.3 to V _{CC2} +0.3	
		P70, P71		-0.3 to 6.0	
V _O	Output Voltage	P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107, P140-P146, P150-P157 ⁽¹⁾ , X _{OUT}		-0.3 to V _{CC1} +0.3	V
		P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P110-P114, P120-P127, P130-P137 ⁽¹⁾		-0.3 to V _{CC2} +0.3	
		P70, P71		-0.3 to 6.0	
P _d	Power Dissipation		T _{opr} =25° C	500	mW
T _{opr}	Operating Ambient Temperature	during CPU operation	T version	-40 to 85	° C
		during flash memory program and erase operation		0 to 60	
T _{stg}	Storage Temperature			-65 to 150	° C

NOTES:

1. P11 to P15 are provided in the 144-pin package only.

$$V_{CC1}=V_{CC2}=5V$$

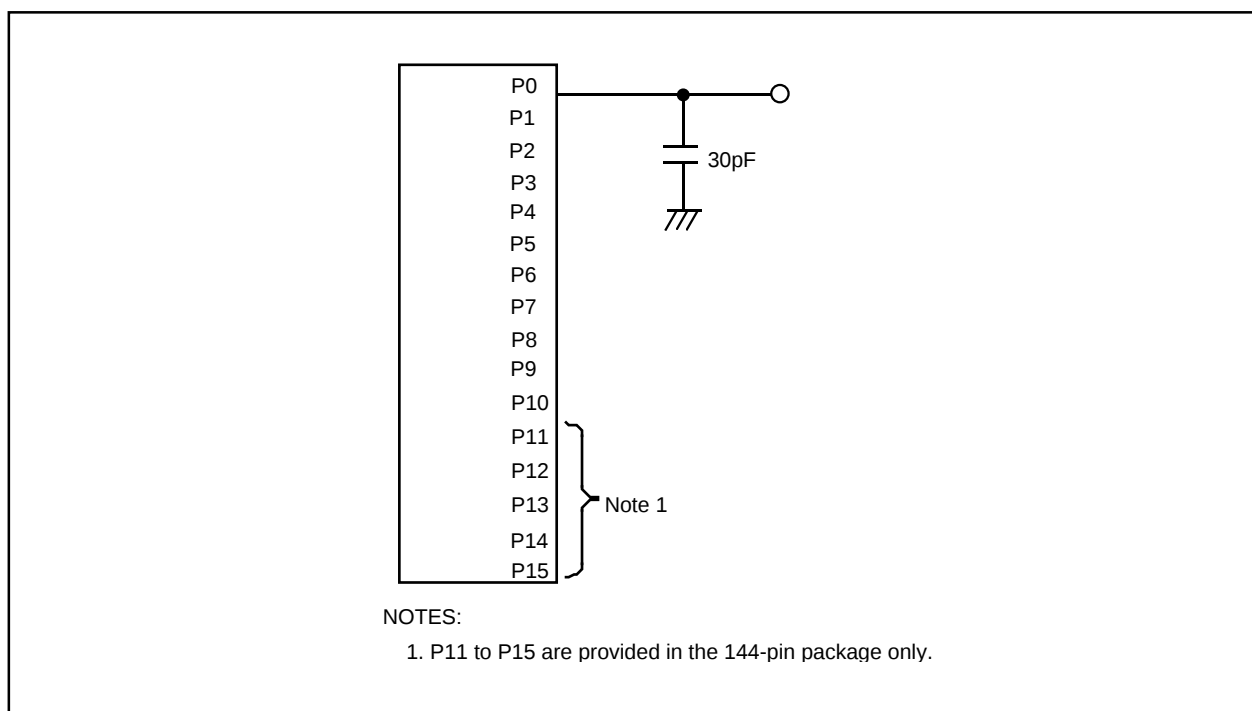


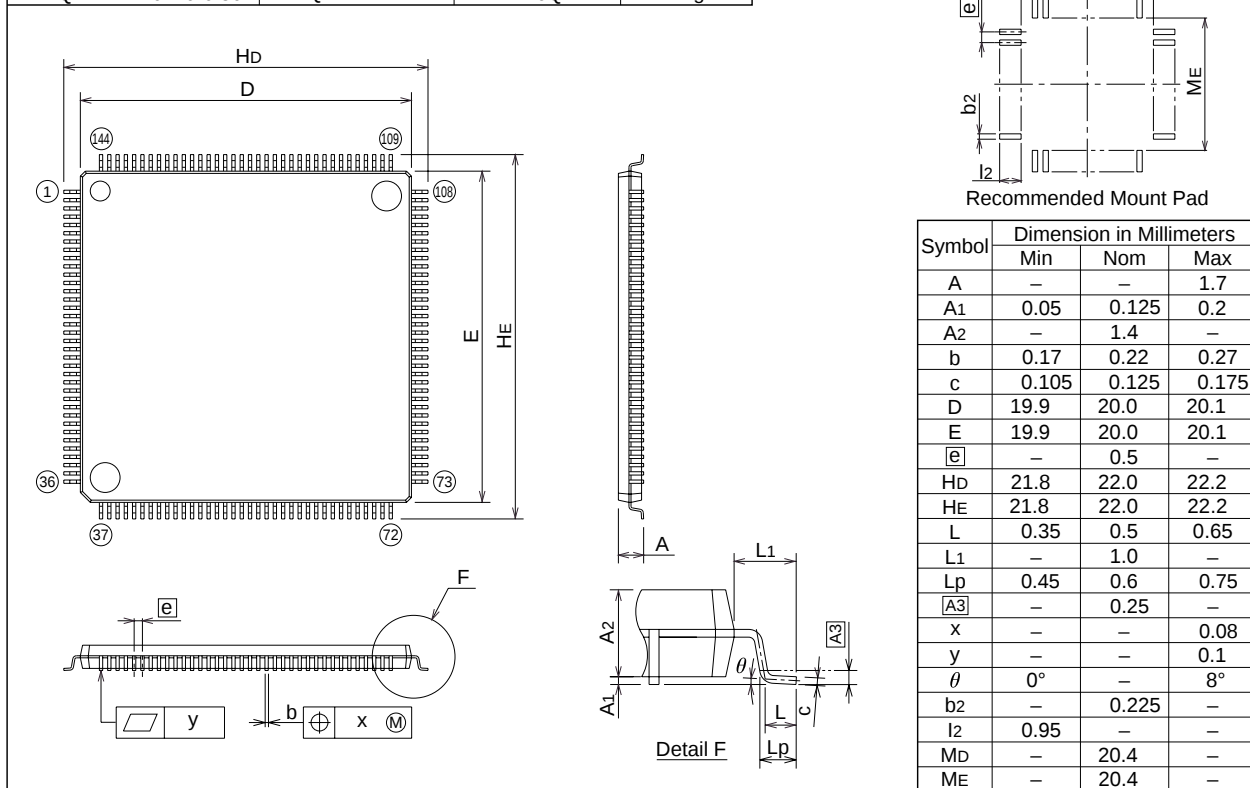
Figure 5.12 P0 to P15 Measurement Circuit

Package Dimensions

PLQP0144KA-A (144P6Q-A)

Plastic 144pin 20X20mm body LQFP

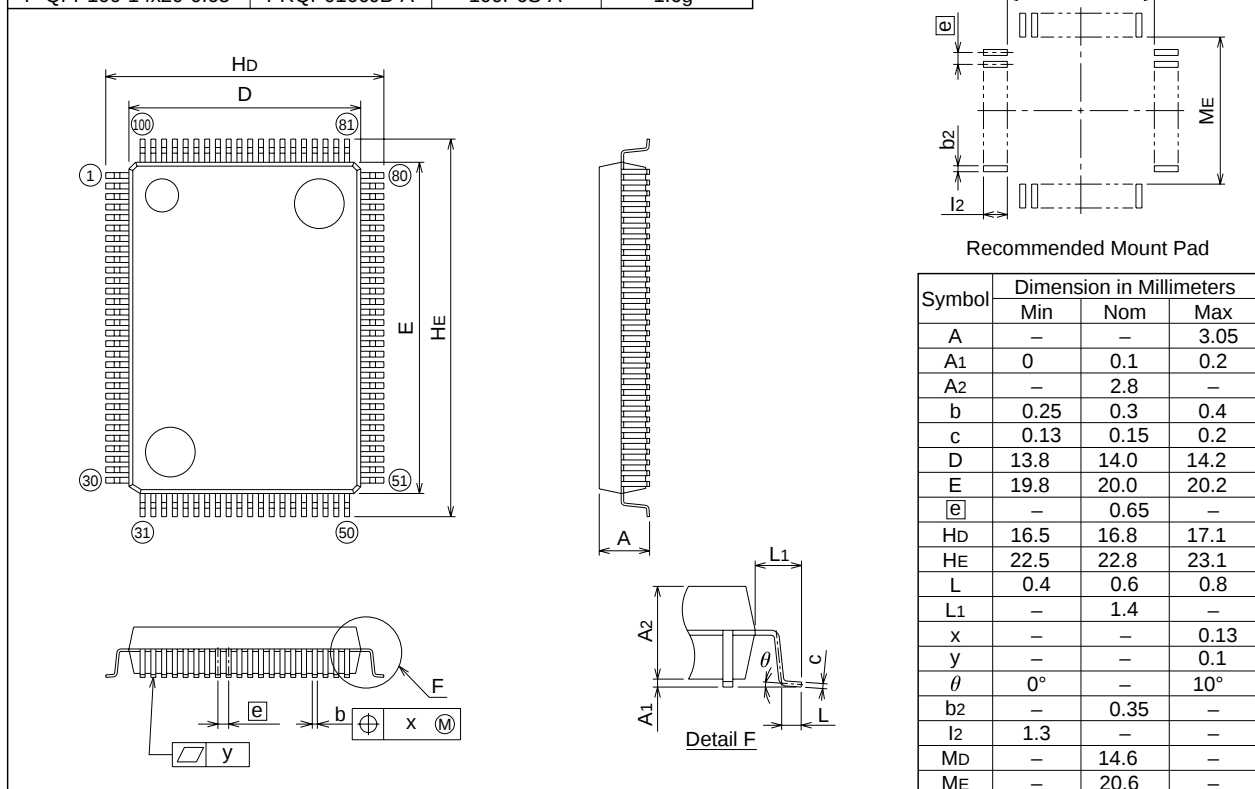
JEITA Package Code	RENESAS Code	Previous Code	Mass[Typ.]
P-LQFP144-20x20-0.50	PLQP0144KA-A	144P6Q-A	1.2g



PRQP0100JB-A (100P6S-A)

Plastic 100pin 14X20mm body QFP

JEITA Package Code	RENESAS Code	Previous Code	Mass[Typ.]
P-QFP100-14x20-0.65	PRQP0100JB-A	100P6S-A	1.6g



REVISION HISTORY	M32C/85 Group (M32C/85, M32C/85T) Datasheet
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Rev.	Date	Description	
		Page	Summary
		50	Electrical Characteristics • Table 5.3 Electrical Characteristics Maximum values for Power Supply Current modified
		52	• Table 5.6 Flash Memory Version Electrical Characteristics Note 1. 100-cycle Products (D3, D5, U3, U5) deleted; Note 4 modified
			• Table 5.7 Flash Memory Version Program and Erase Voltage and Read Operation Voltage Characteristics (at Topr=0 to 60°C) deleted
		63	• Table 5.22 Electrical Characteristics Maximum values for Power Supply Consumption modified and standard values when “Topr=85°C while clock is stopped” deleted
1.00	Jun.01, 2004	-	M32C/85T (High-reliability version) added
		All Pages	Words standardized: On-chip oscillator, A/D converter and D/A converter
			Overview
		1	• 1.1 Applications Automobiles added
		2, 3	• Table 1.1 and Table 1.2 M32C/85 Group (M32C/85, M32C/85T) Performance M32C/85T added; note 3 added
		4	• Figure 1.1 M32C/85 Group (M32C/85, M32C/85T) Block Diagram Note 3 added
		5	• 1.4 Product Information Description modified
			• Figure 1.2 ROM/RAM Capacity figure modified
		5, 6	• Table 1.3 M32C/85 Group M32C/85T added
		6	• Figure 1.3 Product Numbering System M32C/85T added
		7	• Figure 1.4 Pin Assignment for 144-Pin Package Note 3 added
		12	• Figure 1.6 Pin Assignment for 100-Pin Package Note 5 added
		8 to 10	• Table 1.5 Pin Characteristics for 144-Pin Package Note 1 added
		13, 14	• Table 1.6 Pin Characteristics for 100-Pin Package Note 1 added
		15 to 18	• Table 1.7 Pin Description Notes added
			Memory
		22	• Figure 3.1 Memory Map Tables of internal ROM/internal RAM modified; note 2 modified; notes 4 and 5 added
			SFR
		23	• Note 2 added
		24	• PWCR0 and PWCR1 registers deleted
			• “Values after RESET” of the masked ROM version added to the FMR0 register
			• Note 1 added
			Electrical Characteristics
		46	• Table 5.2 Recommended Operating Conditions f(ripple), Vp-p(ripple), VCC, SVCC and note 1 deleted
		47	• Table 5.3 Electrical Characteristics RPULLUP value for the masked ROM version added

REVISION HISTORY	M32C/85 Group (M32C/85, M32C/85T) Datasheet
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Rev.	Date	Description	
		Page	Summary
		65	• Table 5.28 Memory Expansion Mode and Microprocessor Mode $t_{AC1}(AD-DB)$ expression modified
		77	• Table 5.44 Electrical Characteristics I_{CC} standard value revised
		80	• Table 5.47 Flash Memory Electrical Characteristics T_{opr} value modified
1.21	Jul.01, 2005	All pages	Package code changed: 144P6Q-A to PLQP0144KA-A, 100P6Q-A to PLQP0100KB-A, 100P6S-A to PRQP0100JB-A
		All pages	"Low Voltage Detection Reset" changed to "Brown-out Detection Reset"
			Special Function Register (SFR)
		27	• The G0RB register Value after reset modified
		39	• The TCSPR register Value after reset modified
			Electrical Characteristics
		47	• Table 5.2 Electrical Characteristics Parameter $f(BCLK)$ and its values added
		51	• Table 5.6 Flash Memory Version Electrical Characteristics Measurement condition changed
		53	• Table 5.10 Memory Expansion Mode and Microprocessor Mode $t_{AC1}(RD-DB)$ expression on Note 1 modified; $t_{AC2}(RD-DB)$ expression on Note 1 added
		59	• Figure 5.3 Vcc1=Vcc2=5V Timing Diagram (1) $t_{W(ER)}$ expression on Note 3 modified; t_{CYC} expression added
		60	• Figure 5.4 Vcc1=Vcc2=5V Timing Diagram (2) $t_{AC2}(AD-DB)$ expression on Note 1 modified; $t_{H(ALE-AD)}$ expressions on Notes 1 and 2 modified; t_{CYC} expression added
		65	• Table 5.28 Memory Expansion Mode and Microprocessor Mode $t_{AC1}(RD-DB)$ expression on Note 1 modified; $t_{AC2}(RD-DB)$ expression on Note 1 added
		70	• Figure 5.7 Vcc1=Vcc2=3.3V Timing Diagram (1) $t_{W(ER)}$ expression on Note 3 modified; t_{CYC} expression added
		71	• Figure 5.8 Vcc1=Vcc2=3.3V Timing Diagram (2) $t_{AC2}(RD-DB)$ expression on Note 1 modified; $t_{H(ALE-AD)}$ expressions on Notes 1 and 2 modified; $t_{H(WR-CS)}$ expression on Note 2 modified; t_{CYC} expression added
		76	• Table 5.43 Electrical Characteristics Parameter $f(BCLK)$ and its values added
		80	• Table 5.47 Flash Memory Version Electrical Characteristics Measurement condition changed