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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Not For New Designs
Core Processor	M32C/80
Core Size	16/32-Bit
Speed	32MHz
Connectivity	CANbus, I ² C, IEBus, SIO, UART/USART
Peripherals	DMA, WDT
Number of I/O	85
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 26x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m30853fjfp-u3

1. Overview

The M32C/85 group (M32C/85, M32C/85T) microcomputer is a single-chip control unit that utilizes high-performance silicon gate CMOS technology with the M32C/80 series CPU core. The M32C/85 group (M32C/85, M32C/85T) is available in 144-pin and 100-pin plastic molded LQFP/QFP packages.

With a 16-Mbyte address space, this microcomputer combines advanced instruction manipulation capabilities to process complex instructions by less bytes and execute instructions at higher speed.

It includes a multiplier and DMAC adequate for office automation, communication devices and industrial equipments, and other high-speed processing applications.

1.1 Applications

Automobiles, audio, cameras, office equipment, communications equipment, portable equipment, etc.

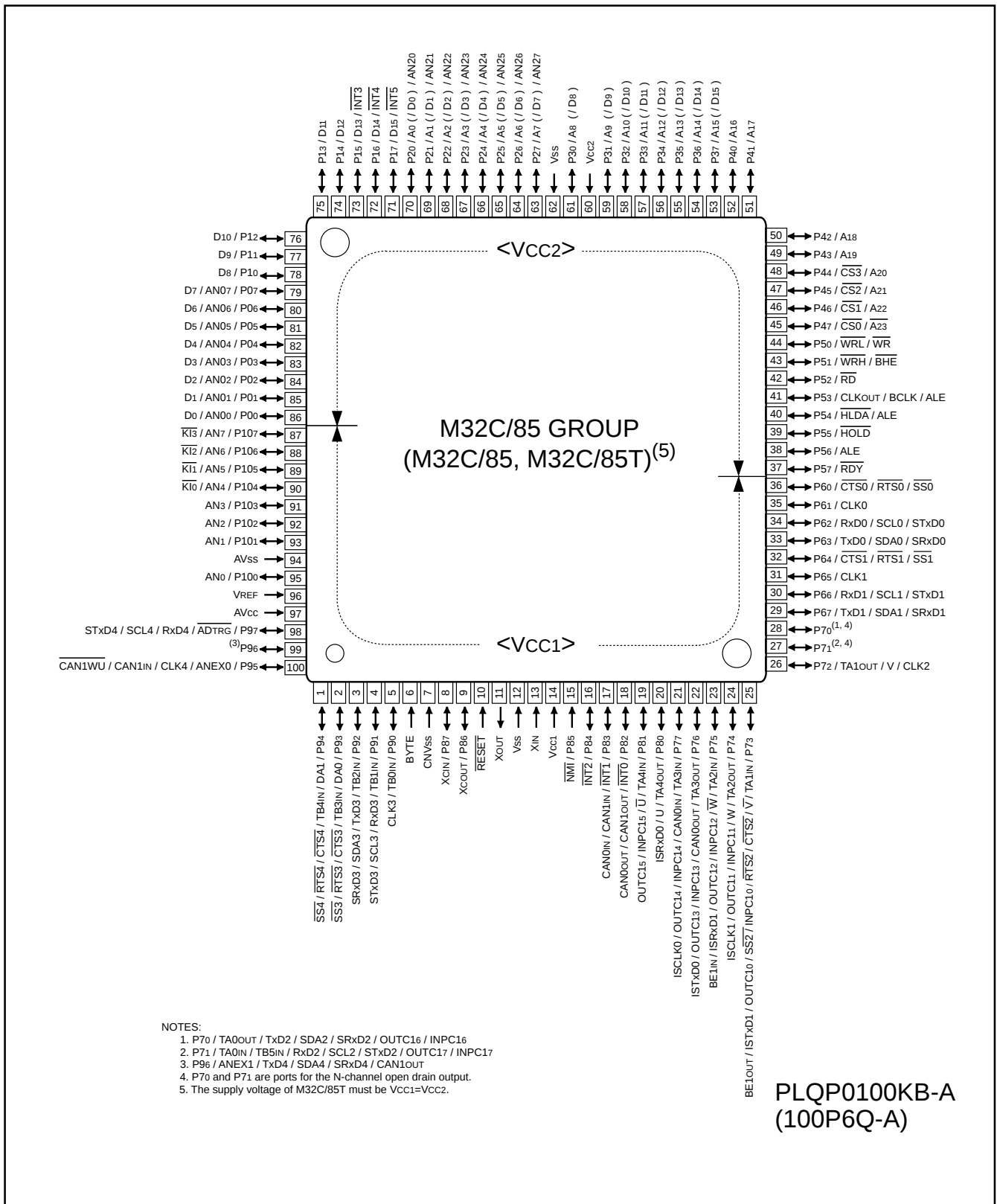


Figure 1.4 Pin Assignment for 100-Pin Package

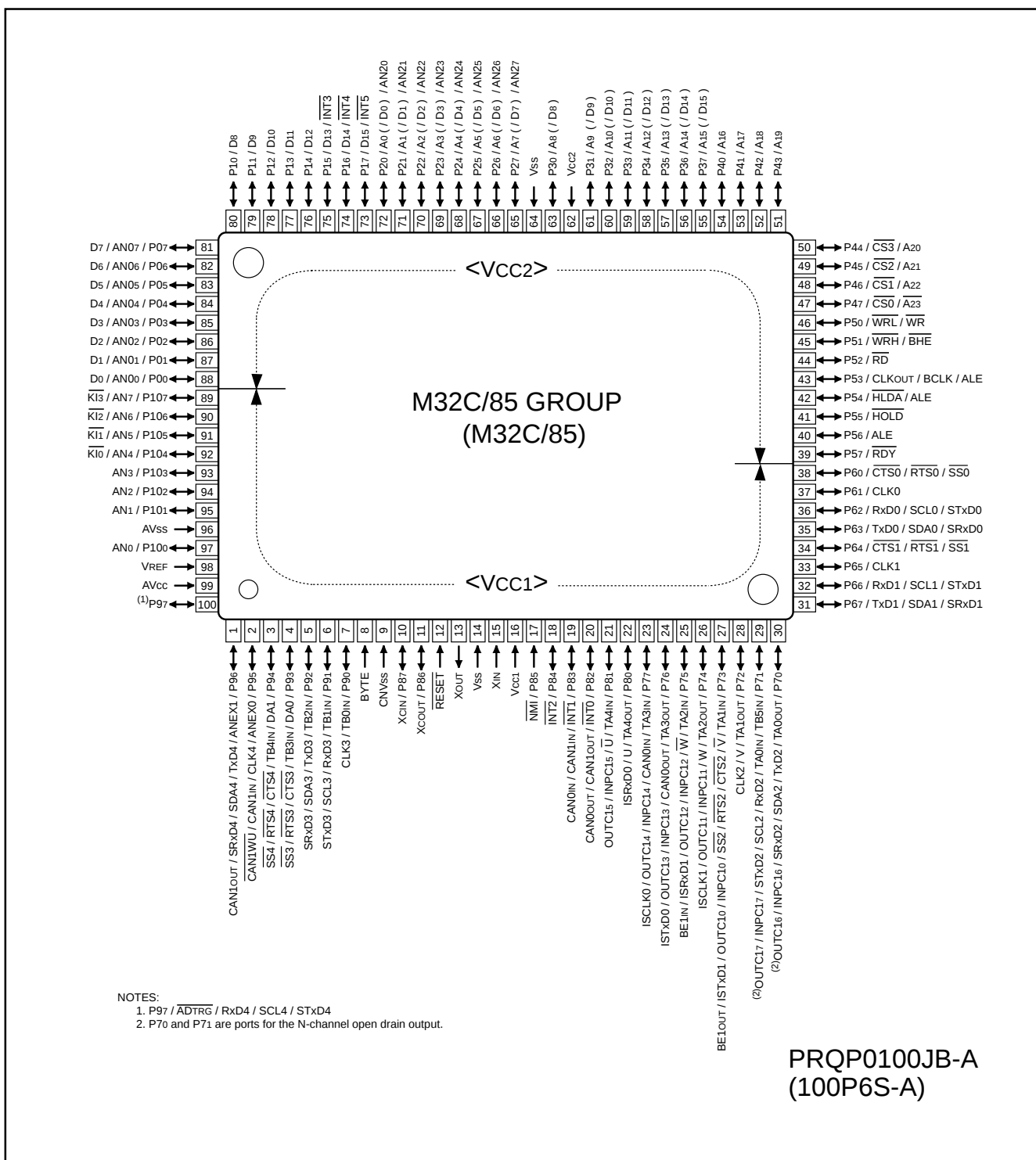


Figure 1.5 Pin Assignment for 100-Pin Package

2.1.8.5 Register Bank Select Flag (B)

The register bank 0 is selected when the B flag is set to "0". The register bank 1 is selected when this flag is set to "1".

2.1.8.6 Overflow Flag (O)

The O flag is set to "1" when the result of an arithmetic operation overflows; otherwise "0".

2.1.8.7 Interrupt Enable Flag (I)

The I flag enables a maskable interrupt.

Interrupt is disabled when the I flag is set to "0" and enabled when the I flag is set to "1". The I flag is set to "0" when an interrupt is acknowledged.

2.1.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to "0". USP is selected when this flag is set to "1".

The U flag is set to "0" when a hardware interrupt is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.1.8.9 Processor Interrupt Priority Level (IPL)

IPL, 3 bits wide, assigns processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has greater priority than IPL, the interrupt is enabled.

2.1.8.10 Reserved Space

When writing to a reserved space, set to "0". When reading, its content is indeterminate.

2.2 High-Speed Interrupt Registers

Registers associated with the high-speed interrupt are as follows:

- Flag save register (SVF)
- PC save register (SVP)
- Vector register (VCT)

2.3 DMAC-Associated Registers

Registers associated with DMAC are as follows:

- DMA mode register (DMD0, DMD1)
- DMA transfer count register (DCT0, DCT1)
- DMA transfer count reload register (DRC0, DRC1)
- DMA memory address register (DMA0, DMA1)
- DMA SFR address register (DSA0, DSA1)
- DMA memory address reload register (DRA0, DRA1)

3. Memory

Figure 3.1 shows a memory map of the M32C/85 group (M32C/85, M32C/85T).

The M32C/85 group (M32C/85, M32C/85T) provides 16-Mbyte address space from addresses 000000₁₆ to FFFFFFF₁₆.

The internal ROM is allocated lower addresses beginning with address FFFFFFF₁₆. For example, a 64-Kbyte internal ROM is allocated addresses FF0000₁₆ to FFFFFFF₁₆.

The fixed interrupt vectors are allocated addresses FFFFDC₁₆ to FFFFFFF₁₆. It stores the starting address of each interrupt routine.

The internal RAM is allocated higher addresses beginning with address 000400₁₆. For example, a 10-Kbyte internal RAM is allocated addresses 000400₁₆ to 002BFF₁₆. Besides storing data, it becomes stacks when the subroutine is called or an interrupt is acknowledged.

SFR, consisting of control registers for peripheral functions such as I/O port, A/D converter, serial I/O, timers, is allocated addresses 000000₁₆ to 0003FF₁₆. All blank spaces within SFR are reserved and cannot be accessed by users.

The special page vectors are allocated addresses FFFE00₁₆ to FFFFDB₁₆. It is used for the JMPS instruction and JSRS instruction. Refer to the Renesas publication **M32C/80 Series Software Manual** for details. In memory expansion mode and microprocessor mode, some spaces are reserved and cannot be accessed by users.

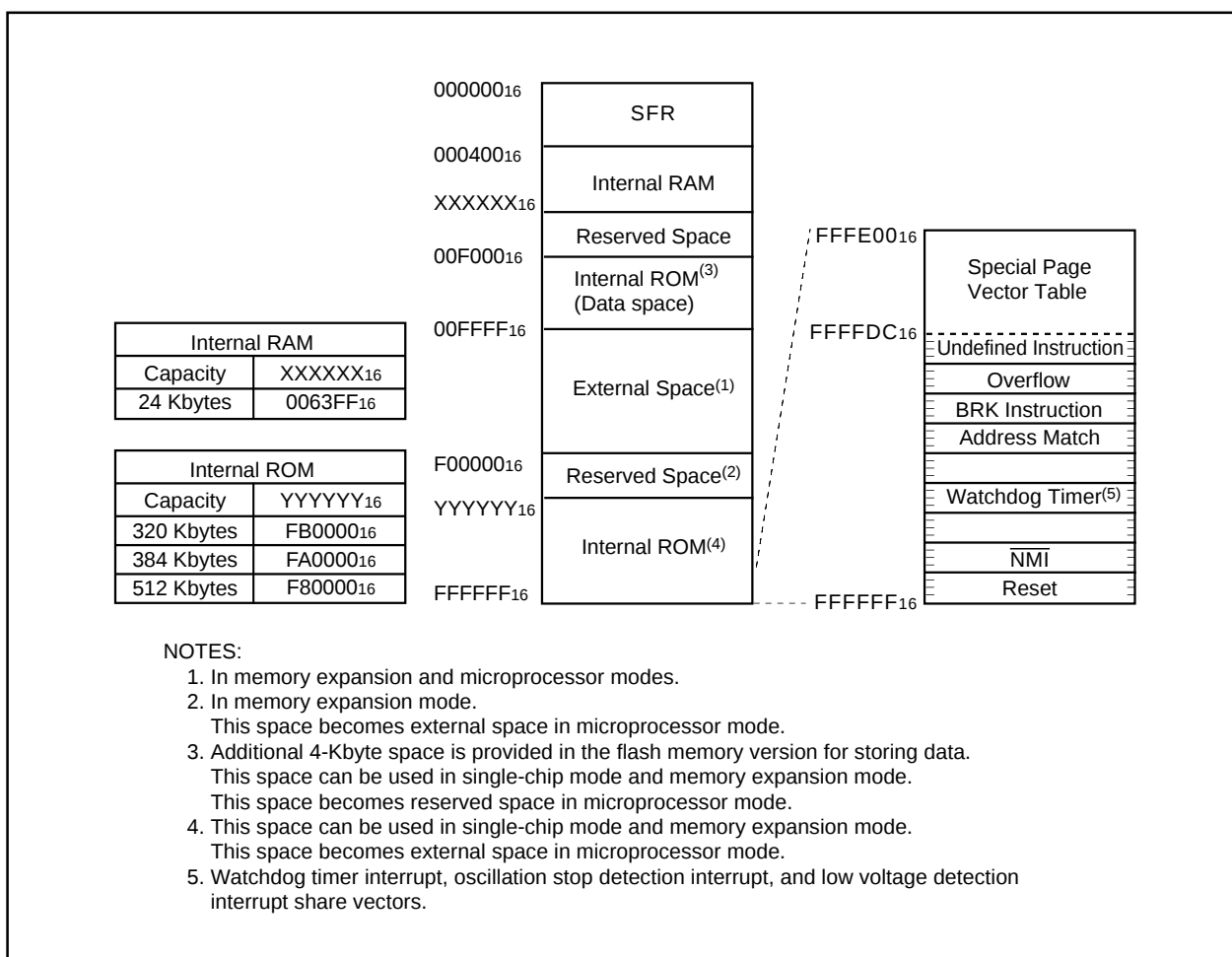


Figure 3.1 Memory Map

Address	Register	Symbol	Value after RESET
0090 ₁₆	UART0 Transmit /NACK Interrupt Control Register	S0TIC	XXXX X000 ₂
0091 ₁₆	UART1/UART4 Bus Conflict Detect Interrupt Control Register	BCN1IC/BCN4IC	XXXX X000 ₂
0092 ₁₆	UART1 Transmit/NACK Interrupt Control Register	S1TIC	XXXX X000 ₂
0093 ₁₆	Key Input Interrupt Control Register	KUPIC	XXXX X000 ₂
0094 ₁₆	Timer B0 Interrupt Control Register	TB0IC	XXXX X000 ₂
0095 ₁₆	Intelligent I/O Interrupt Control Register 1/ CAN Interrupt 4 Control Register	IIO1IC/ CAN4IC	XXXX X000 ₂
0096 ₁₆	Timer B2 Interrupt Control Register	TB2IC	XXXX X000 ₂
0097 ₁₆	Intelligent I/O Interrupt Control Register 3	IIO3IC	XXXX X000 ₂
0098 ₁₆	Timer B4 Interrupt Control Register	TB4IC	XXXX X000 ₂
0099 ₁₆	CAN Interrupt 5 Control Register	CAN5IC	XXXX X000 ₂
009A ₁₆	INT4 Interrupt Control Register	INT4IC	XX00 X000 ₂
009B ₁₆			
009C ₁₆	INT2 Interrupt Control Register	INT2IC	XX00 X000 ₂
009D ₁₆	Intelligent I/O Interrupt Control Register 9/ CAN Interrupt 0 Control Register	IIO9IC/ CAN0IC	XXXX X000 ₂
009E ₁₆	INT0 Interrupt Control Register	INT0IC	XX00 X000 ₂
009F ₁₆	Exit Priority Control Register	RLVL	XXXX 0000 ₂
00A0 ₁₆	Interrupt Request Register 0	IIO0IR	0000 000X ₂
00A1 ₁₆	Interrupt Request Register 1	IIO1IR	0000 000X ₂
00A2 ₁₆	Interrupt Request Register 2	IIO2IR	0000 000X ₂
00A3 ₁₆	Interrupt Request Register 3	IIO3IR	0000 000X ₂
00A4 ₁₆	Interrupt Request Register 4	IIO4IR	0000 000X ₂
00A5 ₁₆	Interrupt Request Register 5	IIO5IR	0000 000X ₂
00A6 ₁₆			
00A7 ₁₆			
00A8 ₁₆	Interrupt Request Register 8	IIO8IR	0000 000X ₂
00A9 ₁₆	Interrupt Request Register 9	IIO9IR	0000 000X ₂
00AA ₁₆	Interrupt Request Register 10	IIO10IR	0000 000X ₂
00AB ₁₆	Interrupt Request Register 11	IIO11IR	0000 000X ₂
00AC ₁₆			
00AD ₁₆			
00AE ₁₆			
00AF ₁₆			
00B0 ₁₆	Interrupt Enable Register 0	IIO0IE	00 ₁₆
00B1 ₁₆	Interrupt Enable Register 1	IIO1IE	00 ₁₆
00B2 ₁₆	Interrupt Enable Register 2	IIO2IE	00 ₁₆
00B3 ₁₆	Interrupt Enable Register 3	IIO3IE	00 ₁₆
00B4 ₁₆	Interrupt Enable Register 4	IIO4IE	00 ₁₆
00B5 ₁₆	Interrupt Enable Register 5	IIO5IE	00 ₁₆
00B6 ₁₆			
00B7 ₁₆			
00B8 ₁₆	Interrupt Enable Register 8	IIO8IE	00 ₁₆
00B9 ₁₆	Interrupt Enable Register 9	IIO9IE	00 ₁₆
00BA ₁₆	Interrupt Enable Register 10	IIO10IE	00 ₁₆
00BB ₁₆	Interrupt Enable Register 11	IIO11IE	00 ₁₆
00BC ₁₆			
00BD ₁₆			
00BE ₁₆			
00BF ₁₆			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
00C0 ₁₆			
00C1 ₁₆			
00C2 ₁₆			
00C3 ₁₆			
00C4 ₁₆			
00C5 ₁₆			
00C6 ₁₆			
00C7 ₁₆			
00C8 ₁₆			
00C9 ₁₆			
00CA ₁₆			
00CB ₁₆			
00CC ₁₆			
00CD ₁₆			
00CE ₁₆			
00CF ₁₆			
00D0 ₁₆			
00D1 ₁₆			
00D2 ₁₆			
00D3 ₁₆			
00D4 ₁₆			
00D5 ₁₆			
00D6 ₁₆			
00D7 ₁₆			
00D8 ₁₆			
00D9 ₁₆			
00DA ₁₆			
00DB ₁₆			
00DC ₁₆			
00DD ₁₆			
00DE ₁₆			
00DF ₁₆			
00E0 ₁₆			
00E1 ₁₆			
00E2 ₁₆			
00E3 ₁₆			
00E4 ₁₆			
00E5 ₁₆			
00E6 ₁₆			
00E7 ₁₆			
00E8 ₁₆ 00E9 ₁₆	SI/O Receive Buffer Register 0	G0RB	XXXX XXXX ₂ X000 XXXX ₂
00EA ₁₆ 00EB ₁₆	Transmit Buffer/Receive Data Register 0	G0TB/G0DR	XX ₁₆
00EC ₁₆	Receive Input Register 0	G0RI	XX ₁₆
00ED ₁₆	SI/O Communication Mode Register 0	G0MR	00 ₁₆
00EE ₁₆	Transmit Output Register 0	G0TO	XX ₁₆
00EF ₁₆	SI/O Communication Control Register 0	G0CR	0000 X011 ₂

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
0210 ₁₆	CAN0 Slot Interrupt Mask Register	C0SIMKR	00 ₁₆ ⁽²⁾
0211 ₁₆			00 ₁₆ ⁽²⁾
0212 ₁₆			
0213 ₁₆			
0214 ₁₆	CAN0 Error Interrupt Mask Register	C0EIMKR	XXXX X000 ₂ ⁽²⁾
0215 ₁₆	CAN0 Error Interrupt Status Register	C0EISTR	XXXX X000 ₂ ⁽²⁾
0216 ₁₆	CAN0 Error Cause Register	C0EFR	00 ₁₆ ⁽²⁾
0217 ₁₆	CAN0 Baud Rate Prescaler	C0BRP	0000 0001 ₂ ⁽²⁾
0218 ₁₆			
0219 ₁₆	CAN0 Mode Register	C0MDR	XXXX XX00 ₂ ⁽²⁾
021A ₁₆			
021B ₁₆			
021C ₁₆			
021D ₁₆			
021E ₁₆			
021F ₁₆			
0220 ₁₆	CAN0 Single Shot Control Register	C0SSCTLR	00 ₁₆ ⁽²⁾
0221 ₁₆			00 ₁₆ ⁽²⁾
0222 ₁₆			
0223 ₁₆			
0224 ₁₆	CAN0 Single Shot Status Register	C0SSSTR	00 ₁₆ ⁽²⁾
0225 ₁₆			00 ₁₆ ⁽²⁾
0226 ₁₆			
0227 ₁₆			
0228 ₁₆	CAN0 Global Mask Register Standard ID0	C0GMR0	XXX0 0000 ₂ ⁽²⁾
0229 ₁₆	CAN0 Global Mask Register Standard ID1	C0GMR1	XX00 0000 ₂ ⁽²⁾
022A ₁₆	CAN0 Global Mask Register Extended ID0	C0GMR2	XXXX 0000 ₂ ⁽²⁾
022B ₁₆	CAN0 Global Mask Register Extended ID1	C0GMR3	00 ₁₆ ⁽²⁾
022C ₁₆	CAN0 Global Mask Register Extended ID2	C0GMR4	XX00 0000 ₂ ⁽²⁾
022D ₁₆			
022E ₁₆			
022F ₁₆			
0230 ₁₆	CAN0 Message Slot 0 Control Register / CAN0 Local Mask Register A Standard ID0	C0MCTL0/ C0LMAR0	0000 0000 ₂ ⁽²⁾ XXX0 0000 ₂ ⁽²⁾
0231 ₁₆	CAN0 Message Slot 1 Control Register / CAN0 Local Mask Register A Standard ID1	C0MCTL1/ C0LMAR1	0000 0000 ₂ ⁽²⁾ XX00 0000 ₂ ⁽²⁾
0232 ₁₆	CAN0 Message Slot 2 Control Register / CAN0 Local Mask Register A Extended ID0	C0MCTL2/ C0LMAR2	0000 0000 ₂ ⁽²⁾ XXXX 0000 ₂ ⁽²⁾
0233 ₁₆	CAN0 Message Slot 3 Control Register / CAN0 local Mask Register A Extended ID1	C0MCTL3/ C0LMAR3	00 ₁₆ ⁽²⁾ 00 ₁₆ ⁽²⁾
0234 ₁₆	CAN0 Message Slot 4 Control Register / CAN0 Local Mask Register A Extended ID2	C0MCTL4/ C0LMAR4	0000 0000 ₂ ⁽²⁾ XX00 0000 ₂ ⁽²⁾
0235 ₁₆	CAN0 Message Slot 5 Control Register	C0MCTL5	00 ₁₆ ⁽²⁾
0236 ₁₆	CAN0 Message Slot 6 Control Register	C0MCTL6	00 ₁₆ ⁽²⁾
0237 ₁₆	CAN0 Message Slot 7 Control Register	C0MCTL7	00 ₁₆ ⁽²⁾
0238 ₁₆	CAN0 Message Slot 8 Control Register / CAN0 Local Mask Register B Standard ID0	C0MCTL8/ C0LMBR0	0000 0000 ₂ ⁽²⁾ XXX0 0000 ₂ ⁽²⁾
0239 ₁₆	CAN0 Message Slot 9 Control Register / CAN0 Local Mask Register B Standard ID1	C0MCTL9/ C0LMBR1	0000 0000 ₂ ⁽²⁾ XX00 0000 ₂ ⁽²⁾

(Note 1)

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTES:

1. The BANKSEL bit in the C0CTLR1 register switches functions for addresses 0220₁₆ to 023F₁₆.
2. Values are obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) after reset and applying the clock to the CAN module.

Address	Register	Symbol	Value after RESET
0340 ₁₆	Count Start Flag	TABSR	00 ₁₆
0341 ₁₆	Clock Prescaler Reset Flag	CPSRF	0XXX XXXX ₂
0342 ₁₆	One-Shot Start Flag	ONSF	00 ₁₆
0343 ₁₆	Trigger Select Register	TRGSR	00 ₁₆
0344 ₁₆	Up/Down Flag	UDF	00 ₁₆
0345 ₁₆			
0346 ₁₆ 0347 ₁₆	Timer A0 Register	TA0	XX ₁₆ XX ₁₆
0348 ₁₆ 0349 ₁₆	Timer A1 Register	TA1	XX ₁₆ XX ₁₆
034A ₁₆ 034B ₁₆	Timer A2 Register	TA2	XX ₁₆ XX ₁₆
034C ₁₆ 034D ₁₆	Timer A3 Register	TA3	XX ₁₆ XX ₁₆
034E ₁₆ 034F ₁₆	Timer A4 Register	TA4	XX ₁₆ XX ₁₆
0350 ₁₆ 0351 ₁₆	Timer B0 Register	TB0	XX ₁₆ XX ₁₆
0352 ₁₆ 0353 ₁₆	Timer B1 Register	TB1	XX ₁₆ XX ₁₆
0354 ₁₆ 0355 ₁₆	Timer B2 Register	TB2	XX ₁₆ XX ₁₆
0356 ₁₆	Timer A0 Mode Register	TA0MR	00 ₁₆
0357 ₁₆	Timer A1 Mode Register	TA1MR	00 ₁₆
0358 ₁₆	Timer A2 Mode Register	TA2MR	00 ₁₆
0359 ₁₆	Timer A3 Mode Register	TA3MR	00 ₁₆
035A ₁₆	Timer A4 Mode Register	TA4MR	00 ₁₆
035B ₁₆	Timer B0 Mode Register	TB0MR	00XX 0000 ₂
035C ₁₆	Timer B1 Mode Register	TB1MR	00XX 0000 ₂
035D ₁₆	Timer B2 Mode Register	TB2MR	00XX 0000 ₂
035E ₁₆	Timer B2 Special Mode Register	TB2SC	XXXX XXX0 ₂
035F ₁₆	Count Source Prescaler Register ⁽¹⁾	TCSPPR	0XXX 0000 ₂
0360 ₁₆			
0361 ₁₆			
0362 ₁₆			
0363 ₁₆			
0364 ₁₆	UART0 Special Mode Register 4	U0SMR4	00 ₁₆
0365 ₁₆	UART0 Special Mode Register 3	U0SMR3	00 ₁₆
0366 ₁₆	UART0 Special Mode Register 2	U0SMR2	00 ₁₆
0367 ₁₆	UART0 Special Mode Register	U0SMR	00 ₁₆
0368 ₁₆	UART0 Transmit/Receive Mode Register	U0MR	00 ₁₆
0369 ₁₆	UART0 Bit Rate Register	U0BRG	XX ₁₆
036A ₁₆ 036B ₁₆	UART0 Transmit Buffer Register	U0TB	XX ₁₆ XX ₁₆
036C ₁₆	UART0 Transmit/Receive Control Register 0	U0C0	0000 1000 ₂
036D ₁₆	UART0 Transmit/Receive Control Register 1	U0C1	0000 0010 ₂
036E ₁₆ 036F ₁₆	UART0 Receive Buffer Register	U0RB	XX ₁₆ XX ₁₆

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTES:

1. The TCSPPR register maintains values set before reset, even after software reset or watchdog timer reset has been performed.

<100-pin package>

Address	Register	Symbol	Value after RESET
03A0 ₁₆			
03A1 ₁₆			
03A2 ₁₆			
03A3 ₁₆			
03A4 ₁₆			
03A5 ₁₆			
03A6 ₁₆			
03A7 ₁₆	Function Select Register D1	PSD1	X0XX XX00 ₂
03A8 ₁₆			
03A9 ₁₆			
03AA ₁₆			
03AB ₁₆			
03AC ₁₆	Function Select Register C2	PSC2	XXXX X00X ₂
03AD ₁₆	Function Select Register C3	PSC3	X0XX XXXX ₂
03AE ₁₆			
03AF ₁₆	Function Select Register C	PSC	00X0 0000 ₂
03B0 ₁₆	Function Select Register A0	PS0	00 ₁₆
03B1 ₁₆	Function Select Register A1	PS1	00 ₁₆
03B2 ₁₆	Function Select Register B0	PSL0	00 ₁₆
03B3 ₁₆	Function Select Register B1	PSL1	00 ₁₆
03B4 ₁₆	Function Select Register A2	PS2	00X0 0000 ₂
03B5 ₁₆	Function Select Register A3	PS3	00 ₁₆
03B6 ₁₆	Function Select Register B2	PSL2	00X0 0000 ₂
03B7 ₁₆	Function Select Register B3	PSL3	00 ₁₆
03B8 ₁₆			
03B9 ₁₆			
03BA ₁₆			
03BB ₁₆			
03BC ₁₆			
03BD ₁₆			
03BE ₁₆			
03BF ₁₆			
03C0 ₁₆	Port P6 Register	P6	XX ₁₆
03C1 ₁₆	Port P7 Register	P7	XX ₁₆
03C2 ₁₆	Port P6 Direction Register	PD6	00 ₁₆
03C3 ₁₆	Port P7 Direction Register	PD7	00 ₁₆
03C4 ₁₆	Port P8 Register	P8	XX ₁₆
03C5 ₁₆	Port P9 Register	P9	XX ₁₆
03C6 ₁₆	Port P8 Direction Register	PD8	00X0 0000 ₂
03C7 ₁₆	Port P9 Direction Register	PD9	00 ₁₆
03C8 ₁₆	Port P10 Register	P10	XX ₁₆
03C9 ₁₆			
03CA ₁₆	Port P10 Direction Register	PD10	00 ₁₆
03CB ₁₆	Set default value to "FF ₁₆ "		
03CC ₁₆			
03CD ₁₆			
03CE ₁₆	Set default value to "FF ₁₆ "		
03CF ₁₆	Set default value to "FF ₁₆ "		

X: Indeterminate

Blank spaces are reserved. No access is allowed.

<100-pin package>

Address	Register	Symbol	Value after RESET
03D0 ₁₆			
03D1 ₁₆			
03D2 ₁₆	Set default value to "FF ₁₆ "		
03D3 ₁₆	Set default value to "FF ₁₆ "		
03D4 ₁₆			
03D5 ₁₆			
03D6 ₁₆			
03D7 ₁₆			
03D8 ₁₆			
03D9 ₁₆			
03DA ₁₆	Pull-Up Control Register 2	PUR2	00 ₁₆
03DB ₁₆	Pull-Up Control Register 3	PUR3	00 ₁₆
03DC ₁₆	Set default value to "00 ₁₆ "		
03DD ₁₆			
03DE ₁₆			
03DF ₁₆			
03E0 ₁₆	Port P0 Register	P0	XX ₁₆
03E1 ₁₆	Port P1 Register	P1	XX ₁₆
03E2 ₁₆	Port P0 Direction Register	PD0	00 ₁₆
03E3 ₁₆	Port P1 Direction Register	PD1	00 ₁₆
03E4 ₁₆	Port P2 Register	P2	XX ₁₆
03E5 ₁₆	Port P3 Register	P3	XX ₁₆
03E6 ₁₆	Port P2 Direction Register	PD2	00 ₁₆
03E7 ₁₆	Port P3 Direction Register	PD3	00 ₁₆
03E8 ₁₆	Port P4 Register	P4	XX ₁₆
03E9 ₁₆	Port P5 Register	P5	XX ₁₆
03EA ₁₆	Port P4 Direction Register	PD4	00 ₁₆
03EB ₁₆	Port P5 Direction Register	PD5	00 ₁₆
03EC ₁₆			
03ED ₁₆			
03EE ₁₆			
03EF ₁₆			
03F0 ₁₆	Pull-up Control Register 0	PUR0	00 ₁₆
03F1 ₁₆	Pull-up Control Register 1	PUR1	XXXX 0000 ₂
03F2 ₁₆			
03F3 ₁₆			
03F4 ₁₆			
03F5 ₁₆			
03F6 ₁₆			
03F7 ₁₆			
03F8 ₁₆			
03F9 ₁₆			
03FA ₁₆			
03FB ₁₆			
03FC ₁₆			
03FD ₁₆			
03FE ₁₆			
03FF ₁₆	Port Control Register	PCR	XXXX XXX0 ₂

X: Indeterminate

Blank spaces are reserved. No access is allowed.

$$V_{CC1}=V_{CC2}=5V$$

Table 5.3 Electrical Characteristics (Continued)(V_{CC1}=V_{CC2}=4.2 to 5.5V, V_{SS}=0V at T_{opr}= -20 to 85°C, f(BCLK)=32MHz unless otherwise specified)

Symbol	Parameter	Measurement Condition		Standard			Unit
				Min.	Typ.	Max.	
I _{CC}	Power Supply Current	In single-chip mode, output pins are left open and other pins are connected to V _{SS} .	f(BCLK)=32 MHz, Square wave, No division		28	45	mA
			f(BCLK)=32 kHz, In low-power consumption mode, Program running on ROM		430		μA
			Flash Memory		25		
			Masked ROM				
			f(BCLK)=32 kHz, In low-power consumption mode, Program running on RAM ⁽¹⁾		25		μA
			f(BCLK)=32 kHz, In wait mode, T _{opr} =25° C		10		μA
			While clock stops, T _{opr} =25° C		0.8	5	μA
			While clock stops, T _{opr} =85° C			50	μA

NOTES:

- Value is obtained when setting the FMSTP bit in the FMR0 register to "1" (flash memory stopped).

$$V_{CC1}=V_{CC2}=5V$$

Switching Characteristics

($V_{CC1} = V_{CC2} = 4.2$ to $5.5V$, $V_{SS} = 0V$ at $T_{opr} = -20$ to $85^{\circ}C$ unless otherwise specified)

Table 5.22 Memory Expansion Mode and Microprocessor Mode
(when accessing external memory space)

Symbol	Parameter	Measurement Condition	Standard		Unit
			Min.	Max.	
td(BCLK-AD)	Address Output Delay Time	See Figure 5.2		18	ns
th(BCLK-AD)	Address Output Hold Time (BCLK standard)		-3		ns
th(RD-AD)	Address Output Hold Time (RD standard) ⁽³⁾		0		ns
th(WR-AD)	Address Output Hold Time (WR standard) ⁽³⁾		(Note 1)		ns
td(BCLK-CS)	Chip-Select Signal Output Delay Time			18	ns
th(BCLK-CS)	Chip-Select Signal Output Hold Time (BCLK standard)		-3		ns
th(RD-CS)	Chip-Select Signal Output Hold Time (RD standard) ⁽³⁾		0		ns
th(WR-CS)	Chip-Select Signal Output Hold Time (WR standard) ⁽³⁾		(Note 1)		ns
td(BCLK-RD)	RD Signal Output Delay Time			18	ns
th(BCLK-RD)	RD Signal Output Hold Time		-5		ns
td(BCLK-WR)	WR Signal Output Delay Time			18	ns
th(BCLK-WR)	WR Signal Output Hold Time		-5		ns
td(DB-WR)	Data Output Delay Time (WR standard)		(Note 2)		ns
th(WR-DB)	Data Output Hold Time (WR standard) ⁽³⁾		(Note 1)		ns
tW(WR)	WR Output Width		(Note 2)		ns

NOTES:

1. Values can be obtained from the following equations, according to BCLK frequency.

$$t_{h(WR-DB)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$t_{h(WR-AD)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

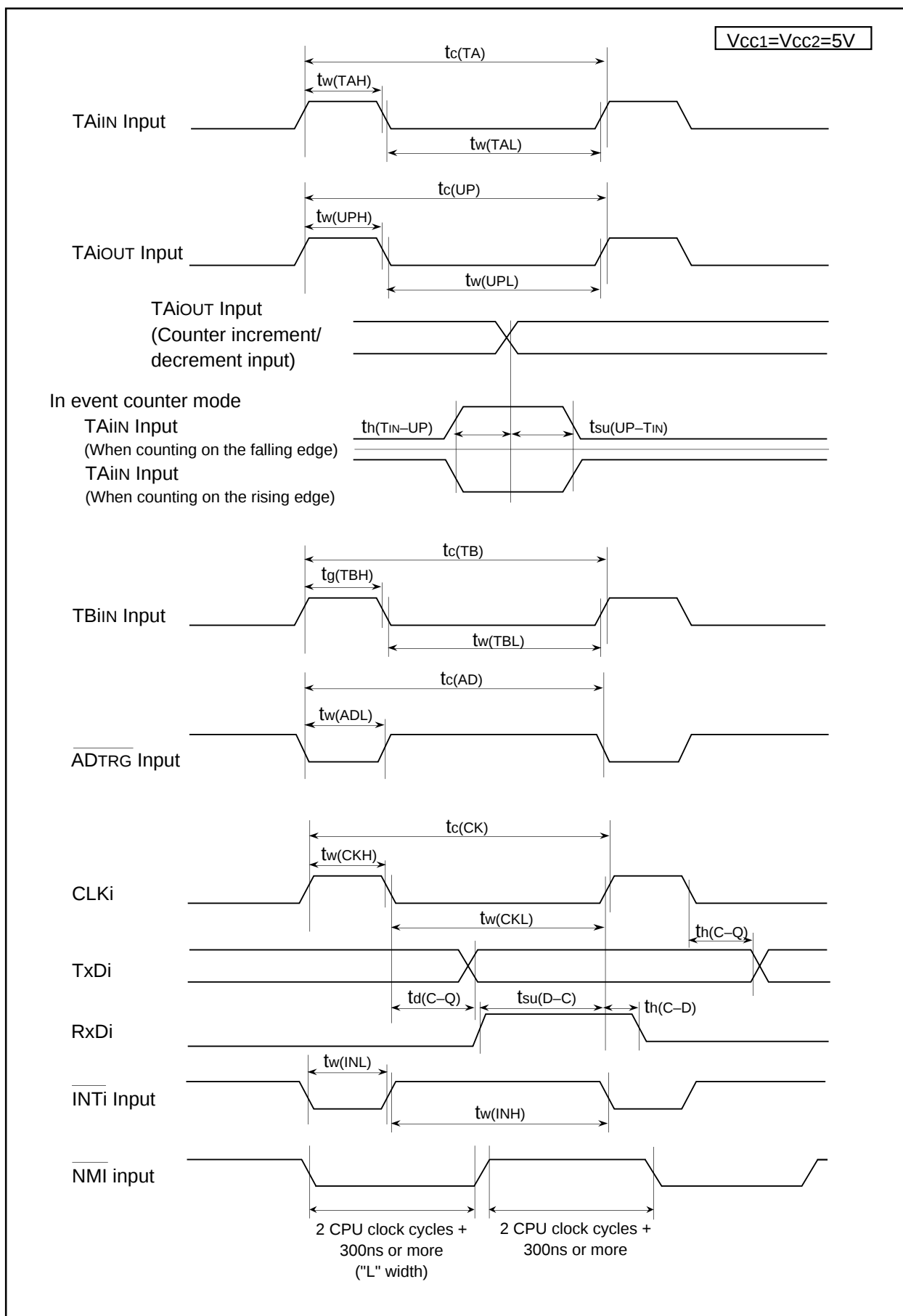
$$t_{h(WR-CS)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

2. Values can be obtained from the following equations, according to BCLK frequency and external bus cycles.

$$t_{W(WR)} = \frac{10^9 \times n}{f_{(BCLK)} \times 2} - 15 \quad [ns] \quad (\text{if external bus cycle is } a\phi + b\phi, n=(bx2)-1)$$

$$t_{d(DB-WR)} = \frac{10^9 \times m}{f_{(BCLK)}} - 20 \quad [ns] \quad (\text{if external bus cycle is } a\phi + b\phi, m=b)$$

3. tc ns is added when recovery cycle is inserted.

Figure 5.5 $V_{CC1}=V_{CC2}=5V$ Timing Diagram (3)

$$V_{CC1}=V_{CC2}=3.3V$$

Timing Requirements

($V_{CC1}=V_{CC2}=3.0$ to $3.6V$, $V_{SS}=0V$ at $T_{opr}=-20$ to $85^{\circ}C$ unless otherwise specified)

Table 5.34 Timer B Input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{C(TB)}$	TBiIN Input Cycle Time (counted on one edge)	100		ns
$t_{W(TBH)}$	TBiIN Input High ("H") Width (counted on one edge)	40		ns
$t_{W(TBL)}$	TBiIN Input Low ("L") Width (counted on one edge)	40		ns
$t_{C(TB)}$	TBiIN Input Cycle Time (counted on both edges)	200		ns
$t_{W(TBH)}$	TBiIN Input High ("H") Width (counted on both edges)	80		ns
$t_{W(TBL)}$	TBiIN Input Low ("L") Width (counted on both edges)	80		ns

Table 5.35 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{C(TB)}$	TBiIN Input Cycle Time	400		ns
$t_{W(TBH)}$	TBiIN Input High ("H") Width	200		ns
$t_{W(TBL)}$	TBiIN Input Low ("L") Width	200		ns

Table 5.36 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{C(TB)}$	TBiIN Input Cycle Time	400		ns
$t_{W(TBH)}$	TBiIN Input High ("H") Width	200		ns
$t_{W(TBL)}$	TBiIN Input Low ("L") Width	200		ns

Table 5.37 A/D Trigger Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{C(AD)}$	$\overline{AD_{TRG}}$ Input Cycle Time (required for trigger)	1000		ns
$t_{W(ADL)}$	$\overline{AD_{TRG}}$ Input Low ("L") Width	125		ns

Table 5.38 Serial I/O

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{C(CK)}$	CLKi Input Cycle Time	200		ns
$t_{W(CKH)}$	CLKi Input High ("H") Width	100		ns
$t_{W(CKL)}$	CLKi Input Low ("L") Width	100		ns
$t_{d(C-Q)}$	TxDi Output Delay Time		80	ns
$t_{h(C-Q)}$	TxDi Hold Time	0		ns
$t_{su(D-C)}$	RxDi Input Setup Time	30		ns
$t_{h(C-Q)}$	RxDi Input Hold Time	90		ns

Table 5.39 External Interrupt $\overline{INTi}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INTi}$ Input High ("H") Width	250		ns
$t_{W(INL)}$	$\overline{INTi}$ Input Low ("L") Width	250		ns

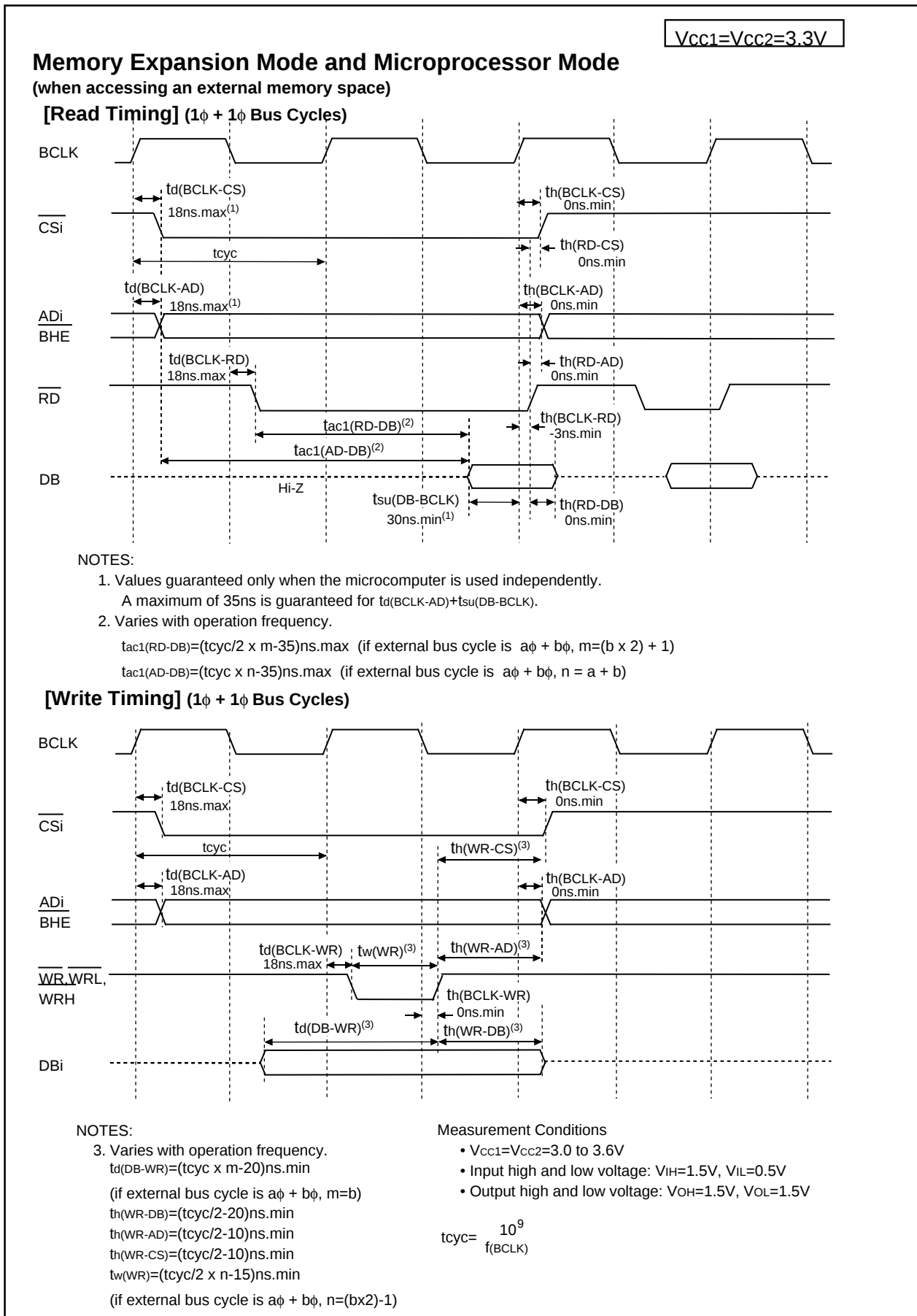
Figure 5.7 V_{CC1}=V_{CC2}=3.3V Timing Diagram (1)

Table 5.43 Recommended Operating Conditions (Continued)**(V_{CC1}=V_{CC2}=4.2 to 5.5V, V_{SS}=0V at T_{opr} = -40 to 85°C (T version) unless otherwise specified)**

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
f(BCLK)	CPU Input Frequency	V _{CC1} =4.2 to 5.5V	0		32	MHz
f(X _{IN})	Main Clock Input Frequency	V _{CC1} =4.2 to 5.5V	0		32	MHz
f(X _{CIN})	Sub Clock Frequency			32.768	50	kHz
f(Ring)	On-chip Oscillator Frequency (V _{CC1} =V _{CC2} =5.0V, T _{opr} =25° C)		0.5	1	2	MHz
f(PLL)	PLL Clock Frequency	V _{CC1} =4.2 to 5.5V	10		32	MHz
t _{SU(PLL)}	Wait Time to Stabilize PLL Frequency Synthesizer	V _{CC1} =5.0V			5	ms

$$V_{CC1}=V_{CC2}=5V$$

Table 5.45 A/D Conversion Characteristics ($V_{CC1}=V_{CC2}=4.2$ to $5.5V$, $V_{SS}=0V$ at $T_{opr}= -40$ to $85^{\circ}C$ (T version), $f(BCLK)=32MHz$ unless otherwise specified)

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min.	Typ.	Max.	
-	Resolution	$V_{REF}=V_{CC1}$			10	Bits
INL	Integral Nonlinearity Error	$V_{REF}=V_{CC1}=V_{CC2}=5V$			± 3	LSB
						LSB
		External op-amp connection mode			± 7	LSB
DNL	Differential Nonlinearity Error				± 1	LSB
-	Offset Error				± 3	LSB
-	Gain Error				± 3	LSB
RLADDER	Resistor Ladder	$V_{REF}=V_{CC1}$	8		40	k Ω
t _{CONV}	10-bit Conversion Time ^(1, 2)		2.06			μs
t _{CONV}	8-bit Conversion Time ^(1, 2)		1.75			μs
t _{SAMP}	Sampling Time ⁽¹⁾		0.188			μs
V _{REF}	Reference Voltage		2		V_{CC1}	V
V _{IA}	Analog Input Voltage		0		V_{REF}	V

NOTES:

1. Divide $f(X_{IN})$, if exceeding 16 MHz, to keep ϕ_{AD} frequency at 16 MHz or less.
2. With using the sample and hold function.

Table 5.46 D/A Conversion Characteristics ($V_{CC1}=V_{CC2}=4.2$ to $5.5V$, $V_{SS}=0V$ at $T_{opr}= -40$ to $85^{\circ}C$ (T version), $f(BCLK)=32MHz$ unless otherwise specified)

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min.	Typ.	Max.	
-	Resolution				8	Bits
-	Absolute Accuracy				1.0	%
t _{SU}	Setup Time				3	μs
R _O	Output Resistance		4	10	20	k Ω
I _{VREF}	Reference Power Supply Input Current	(Note 1)			1.5	mA

NOTES:

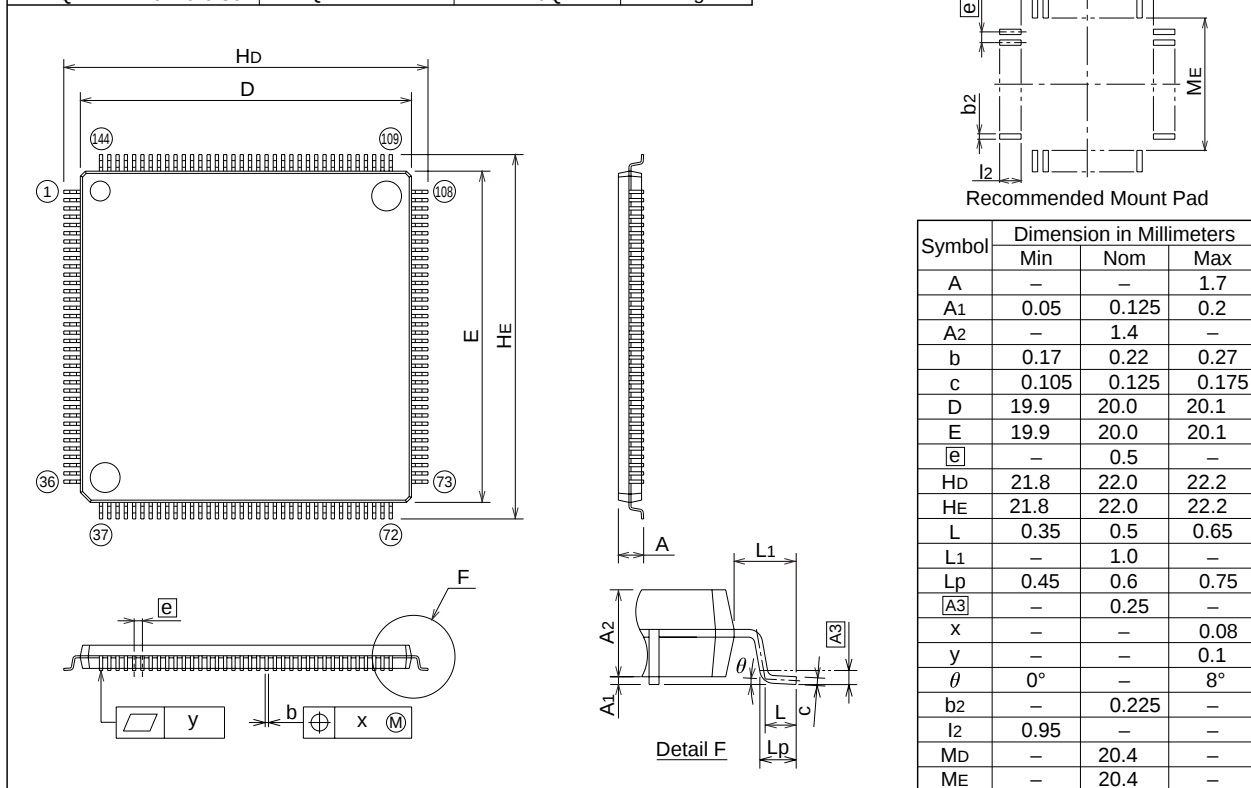
1. Measurement when using one D/A converter. The DA_i register (i=0, 1) of the D/A converter, not being used, is set to "00₁₆". The resistor ladder in the A/D converter is excluded.
I_{VREF} flows even if the VCUT bit in the AD0CON1 register is set to "0" (no V_{REF} connection).

Package Dimensions

PLQP0144KA-A (144P6Q-A)

Plastic 144pin 20X20mm body LQFP

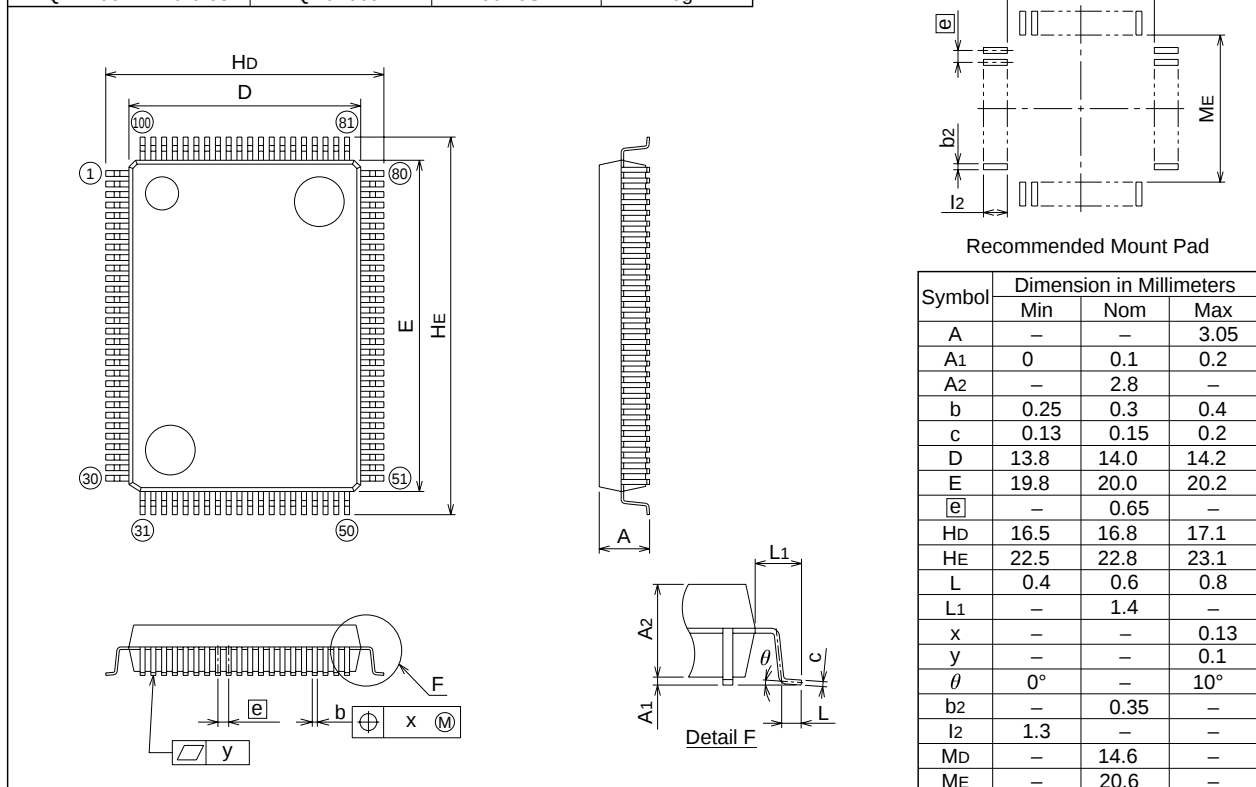
JEITA Package Code	RENESAS Code	Previous Code	Mass[Typ.]
P-LQFP144-20x20-0.50	PLQP0144KA-A	144P6Q-A	1.2g



PRQP0100JB-A (100P6S-A)

Plastic 100pin 14X20mm body QFP

JEITA Package Code	RENESAS Code	Previous Code	Mass[Typ.]
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