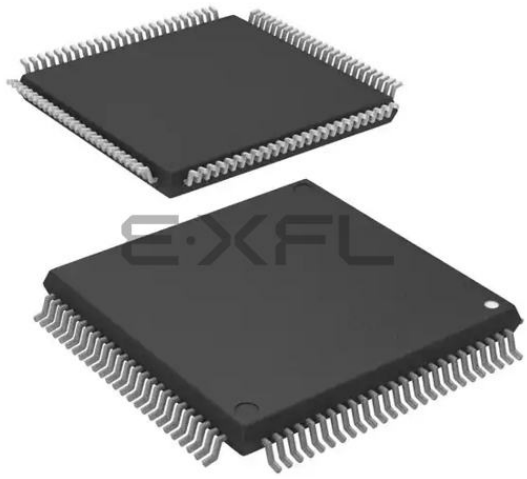
Renesas Electronics America Inc - M30853FWGP#U3 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	M32C/80
Core Size	16/32-Bit
Speed	32MHz
Connectivity	CANbus, I²C, IEBus, SIO, UART/USART
Peripherals	DMA, WDT
Number of I/O	85
Program Memory Size	320KB (320K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 26x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m30853fwgp-u3

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1. Overview

The M32C/85 group (M32C/85, M32C/85T) microcomputer is a single-chip control unit that utilizes high-performance silicon gate CMOS technology with the M32C/80 series CPU core. The M32C/85 group (M32C/85, M32C/85T) is available in 144-pin and 100-pin plastic molded LQFP/QFP packages.

With a 16-Mbyte address space, this microcomputer combines advanced instruction manipulation capabilities to process complex instructions by less bytes and execute instructions at higher speed.

It includes a multiplier and DMAC adequate for office automation, communication devices and industrial equipments, and other high-speed processing applications.

1.1 Applications

Automobiles, audio, cameras, office equipment, communications equipment, portable equipment, etc.

Table 1.2 M32C/85 Group (M32C/85, M32C/85T) Performance (100-Pin Package)

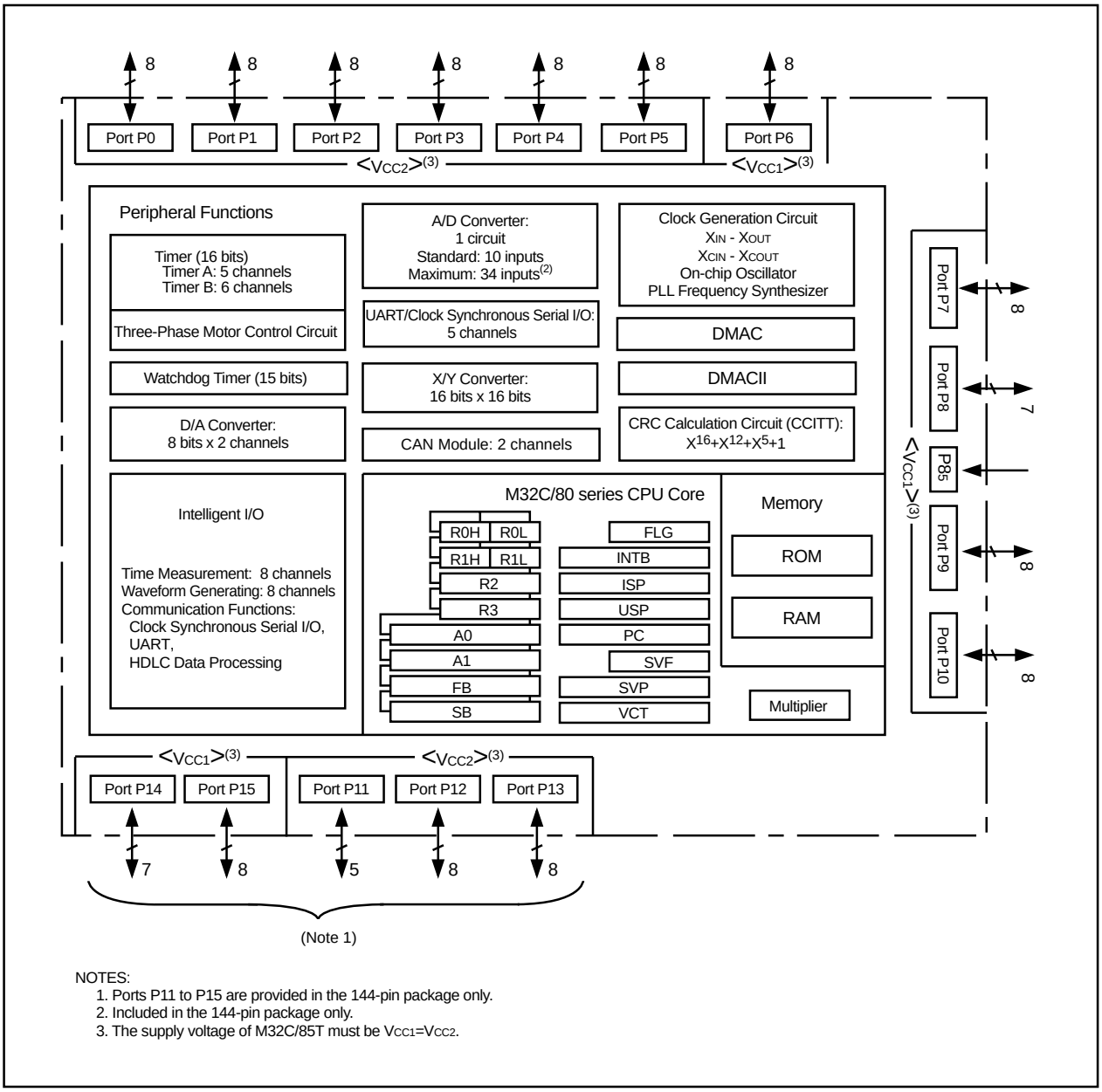
Characteristic		Performance	
		M32C/85	M32C/85T
CPU	Basic Instructions	108 instructions	
	Minimum Instruction Execution Time	31.3 ns (f(BCLK)=32 MHz, V_{CC1}=4.2 V to 5.5 V) 41.7 ns (f(BCLK)=24 MHz, V_{CC1}=3.0 V to 5.5 V)	31.3 ns (f(BCLK)=32 MHz, V_{CC1}=4.2 V to 5.5 V)
	Operating Mode	Single-chip mode, Memory expansion mode and Microprocessor mode	Single-chip mode
	Address Space	16 Mbytes	
	Memory Capacity	See Table 1.3	
Peripheral Function	I/O Port	87 I/O pins and 1 input pin	
	Multifunction Timer	Timer A: 16 bits x 5 channels, Timer B: 16 bits x 6 channels Three-phase motor control circuit	
	Intelligent I/O	Time measurement function or Waveform generating function: 16 bits x 8 channels Communication function (Clock synchronous serial I/O, Clock asynchronous serial I/O, HDLC data processing)	
	Serial I/O	5 Channels Clock synchronous serial I/O, Clock asynchronous serial I/O, IEBus(1), I^2C bus(2)	
	CAN Module	2 channels Supporting CAN 2.0B specification	
	A/D Converter	10-bit A/D converter: 1 circuit, 26 channels	
	D/A Converter	8 bits x 2 channels	
	DMAC	4 channels	
	DMAC II	Can be activated by all peripheral function interrupt sources Immediate transfer, Calculation transfer and Chain transfer functions	
	CRC Calculation Circuit	CRC-CCITT	
	X/Y Converter	16 bits x 16 bits	
	Watchdog Timer	15 bits x 1 channel (with prescaler)	
	Interrupt	39 internal and 8 external sources, 5 software sources Interrupt priority level: 7	
	Clock Generation Circuit	4 circuits Main clock oscillation circuit(*), Sub clock oscillation circuit(*), On-chip oscillator, PLL frequency synthesizer (*)Equipped with a built-in feedback resistor. Ceramic resonator or crystal oscillator must be connected externally	
	Oscillation Stop Detect Function	Main clock oscillation stop detect function	
	Voltage Detection Circuit	Available (optional)	Not available(4)
Electrical Characteristics	Supply Voltage	V_{CC1}=4.2 V to 5.5 V, V_{CC2}=3.0 V to V_{CC1} (f(BCLK)=32 MHz) V_{CC1}=3.0 V to 5.5 V, V_{CC2}=3.0 V to V_{CC1} (f(BCLK)=24 MHz)	V_{CC1}=V_{CC2}=4.2 V to 5.5 V, (f(BCLK)=32 MHz)(3)
	Power Consumption	28 mA (V_{CC1}=V_{CC2}=5 V, f(BCLK)=32 MHz) 22 mA (V_{CC1}=V_{CC2}=3.3 V, f(BCLK)=24 MHz) 10µA (V_{CC1}=V_{CC2}=5 V, f(BCLK)=32 kHz, in wait mode)	28 mA (V_{CC1}=V_{CC2}=5 V, f(BCLK)=32 MHz) 10µA (V_{CC1}=V_{CC2}=5 V, f(BCLK)=32 kHz, in wait mode)
Flash Memory	Program/Erase Supply Voltage	3.3 V ± 0.3 V or 5.0 V ± 0.5 V	5.0 V ± 0.5 V
	Program and Erase Endurance	100 times (all space)	
Operating Ambient Temperature		–20 to 85°C –40 to 85°C (optional)	–40 to 85°C (T version)
Package		100-pin plastic molded LQFP/QFP	

NOTES:
1. IEBus is a trademark of NEC Electronics Corporation.
2. I^2C bus is a trademark of Koninklijke Philips Electronics N. V.
3. The supply voltage of M32C/85T (High-reliability version) must be V_{CC1}=V_{CC2}.
4. The cold start-up/warm start-up determine function is available only at the user's option.

All options are on a request basis.

1.3 Block Diagram

Figure 1.1 shows a block diagram of the M32C/85 group (M32C/85, M32C/85T) microcomputer.



NOTES:
1. Ports P11 to P15 are provided in the 144-pin package only.
2. Included in the 144-pin package only.
3. The supply voltage of M32C/85T must be V_{CC1}=V_{CC2}.

Figure 1.1 M32C/85 Group (M32C/85, M32C/85T) Block Diagram

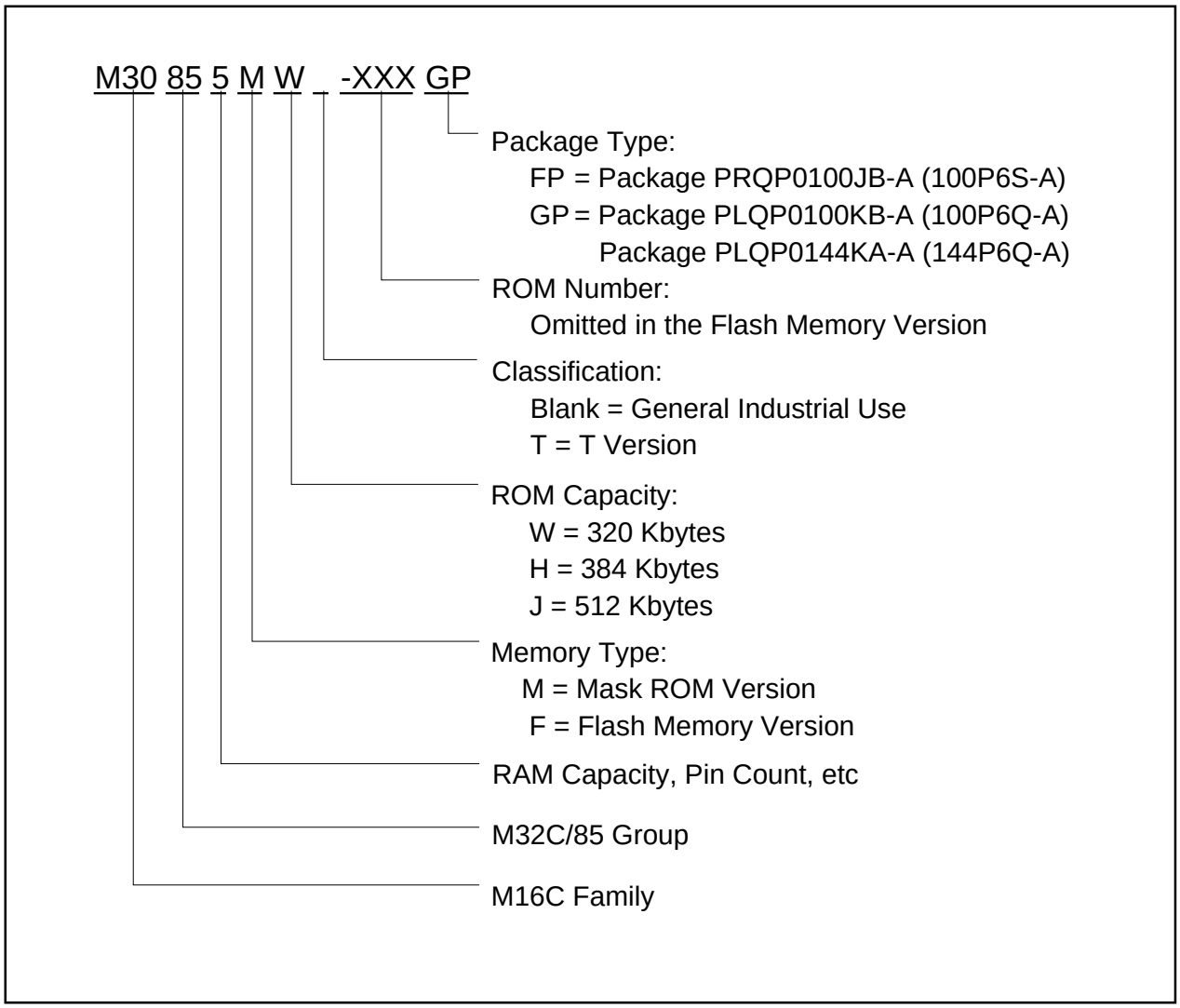


Figure 1.2 Product Numbering System

Table 1.4 Pin Characteristics for 144-Pin Package

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin(1)
1		P96			TxD4/SDA4/SRxD4/CAN1OUT		ANEX1	
2		P95			CLK4/CAN1IN/$\overline{\text{CAN1WU}}$		ANEX0	
3		P94		TB4IN	$\overline{\text{CTS4}}$/$\overline{\text{RTS4}}$/$\overline{\text{SS4}}$		DA1	
4		P93		TB3IN	$\overline{\text{CTS3}}$/$\overline{\text{RTS3}}$/$\overline{\text{SS3}}$		DA0	
5		P92		TB2IN	TxD3/SDA3/SRxD3			
6		P91		TB1IN	RxD3/SCL3/STxD3			
7		P90		TB0IN	CLK3			
8		P146						
9		P145						
10		P144						
11		P143				INPC17/OUTC17		
12		P142				INPC16/OUTC16		
13		P141				INPC15/OUTC15		
14		P140				INPC14/OUTC14		
15	BYTE							
16	CNVSS							
17	XCIN	P87						
18	XCOUT	P86						
19	$\overline{\text{RESET}}$							
20	XOUT							
21	VSS							
22	XIN							
23	VCC1							
24		P85	$\overline{\text{NMI}}$					
25		P84	$\overline{\text{INT2}}$					
26		P83	$\overline{\text{INT1}}$		CAN0IN/CAN1IN			
27		P82	$\overline{\text{INT0}}$		CAN0OUT/CAN1OUT			
28		P81		TA4IN/$\overline{\text{U}}$		INPC15/OUTC15		
29		P80		TA4OUT/U		ISRxD0		
30		P77		TA3IN	CAN0IN	INPC14/OUTC14/ISCLK0		
31		P76		TA3OUT	CAN0OUT	INPC13/OUTC13/ISTxD0		
32		P75		TA2IN/$\overline{\text{W}}$		INPC12/OUTC12/ISRxD1/BE1IN		
33		P74		TA2OUT/W		INPC11/OUTC11/ISCLK1		
34		P73		TA1IN/$\overline{\text{V}}$	$\overline{\text{CTS2}}$/$\overline{\text{RTS2}}$/$\overline{\text{SS2}}$	INPC10/OUTC10/ISTxD1/BE1OUT		
35		P72		TA1OUT/V	CLK2			
36		P71		TB5IN/TA0IN	RxD2/SCL2/STxD2	INPC17/OUTC17		
37		P70		TA0OUT	TxD2/SDA2/SRxD2	INPC16/OUTC16		
38		P67			TxD1/SDA1/SRxD1			
39	VCC1							
40		P66			RxD1/SCL1/STxD1			
41	VSS							
42		P65			CLK1			
43		P64			$\overline{\text{CTS1}}$/$\overline{\text{RTS1}}$/$\overline{\text{SS1}}$			
44		P63			TxD0/SDA0/SRxD0			
45		P62			RxD0/SCL0/STxD0			
46		P61			CLK0			
47		P60			$\overline{\text{CTS0}}$/$\overline{\text{RTS0}}$/$\overline{\text{SS0}}$			
48		P137						

NOTES:
1. Bus control pins in M32C/85T cannot be used.

Table 1.6 Pin Description (100-Pin and 144-Pin Packages) (Continued)

Classsfication	Symbol	I/O Type	Supply Voltage	Function
Main Clock Input	XIN	I	VCC1	I/O pins for the main clock oscillation circuit. Connect a ceramic resonator or crystal oscillator between XIN and XOUT. To apply external clock, apply it to XIN and leave XOUT open
Main Clock Output	XOUT	O	VCC1	
Sub Clock Input	XCIN	I	VCC1	I/O pins for the sub clock oscillation circuit. Connect a crystal oscillator between XCIN and XCOUT. To apply external clock, apply it to XCIN and leave XCOUT open
Sub Clock Output	XCOUT	O	VCC1	
BCLK Output(1)	BCLK	O	VCC2	Outputs BCLK signal
Clock Output	CLKOUT	O	VCC2	Outputs the clock having the same frequency as fC, f8 or f32
$\overline{\text{INT}}$ Interrupt Input	$\overline{\text{INT0}}$ to $\overline{\text{INT2}}$	I	VCC1	Input pins for the $\overline{\text{INT}}$ interrupt
	$\overline{\text{INT3}}$ to $\overline{\text{INT5}}$		VCC2	
$\overline{\text{NMI}}$ Interrupt Input	$\overline{\text{NMI}}$	I	VCC1	Input pin for the $\overline{\text{NMI}}$ interrupt
Key Input Interrupt	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	I	VCC1	Input pins for the key input interrupt
Timer A	TA0OUT to TA4OUT	I/O	VCC1	I/O pins for the timer A0 to A4 (TA0OUT is a pin for the N-channel open drain output.)
	TA0IN to TA4IN	I	VCC1	Input pins for the timer A0 to A4
Timer B	TB0IN to TB5IN	I	VCC1	Input pins for the timer B0 to B5
Three-phase Motor Control Timer Output	U, $\overline{\text{U}}$, V, $\overline{\text{V}}$, W, $\overline{\text{W}}$	O	VCC1	Output pins for the three-phase motor control timer
Serial I/O	$\overline{\text{CTS0}}$ to $\overline{\text{CTS4}}$	I	VCC1	Input pins for data transmission control
	$\overline{\text{RTS0}}$ to $\overline{\text{RTS4}}$	O	VCC1	Output pins for data reception control
	CLK0 to CLK4	I/O	VCC1	Inputs and outputs the transfer clock
	RxD0 to RxD4	I	VCC1	Inputs serial data
	TxD0 to TxD4	O	VCC1	Outputs serial data (TxD2 is a pin for the N-channel open drain output.)
I^2C Mode	SDA0 to SDA4	I/O	VCC1	Inputs and outputs serial data (SDA2 is a pin for the N-channel open drain output.)
	SCL0 to SCL4			Inputs and outputs the transfer clock (SCL2 is a pin for the N-channel open drain output.)
Serial I/O Special Function	STxD0 to STxD4	O	VCC1	Outputs serial data when slave mode is selected (STxD2 is a pin for the N-channel open drain output.)
	SRxD0 to SRxD4	I		Inputs serial data when slave mode is selected
	$\overline{\text{SS0}}$ to $\overline{\text{SS4}}$	I	VCC1	Input pins to control serial I/O special function

I : Input O : Output I/O : Input and output

NOTES:

1. Bus control pins in M32C/85T cannot be used.

4. Special Function Registers (SFR)

Address	Register	Symbol	Value after RESET
000016			
000116			
000216			
000316			
000416	Processor Mode Register(1)	PM0	1000 00002(CNVss pin ="L") 0000 00112(CNVss pin ="H")
000516	Processor Mode Register 1	PM1	0016
000616	System Clock Control Register 0	CM0	0000 10002
000716	System Clock Control Register 1	CM1	0010 00002
000816			
000916	Address Match Interrupt Enable Register	AIER	0016
000A16	Protect Register	PRCR	XXXX 00002
000B16	External Data Bus Width Control Register(2)	DS	XXXX 10002(BYTE pin ="L") XXXX 00002(BYTE pin ="H")
000C16	Main Clock Division Register	MCD	XXX0 10002
000D16	Oscillation Stop Detection Register	CM2	0016
000E16	Watchdog Timer Start Register	WDTS	XX16
000F16	Watchdog Timer Control Register	WDC	000X XXXX2
001016 001116 001216	Address Match Interrupt Register 0	RMAD0	00000016
001316	Processor Mode Register 2	PM2	0016
001416 001516 001616	Address Match Interrupt Register 1	RMAD1	00000016
001716	Voltage Detection Register 2(2)	VCR2	0016
001816 001916 001A16	Address Match Interrupt Register 2	RMAD2	00000016
001B16	Voltage Detection Register 1(2)	VCR1	0000 10002
001C16 001D16 001E16	Address Match Interrupt Register 3	RMAD3	00000016
001F16			
002016			
002116			
002216			
002316			
002416			
002516			
002616	PLL Control Register 0	PLC0	0001 X0102
002716	PLL Control Register 1	PLC1	000X 00002
002816 002916 002A16	Address Match Interrupt Register 4	RMAD4	00000016
002B16			
002C16 002D16 002E16	Address Match Interrupt Register 5	RMAD5	00000016
002F16	Low Voltage Detection Interrupt Register(2)	D4INT	0016

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTES:

1. The PM01 and PM00 bits in the PM0 register maintain values set before reset, even after software reset or watch-dog timer reset has been performed.
2. These registers in M32C/85T cannot be used.

Address	Register	Symbol	Value after RESET
026016	CAN1 Message Slot Buffer 0 Standard ID0	C1SLOT0_0	XX16
026116	CAN1 Message Slot Buffer 0 Standard ID1	C1SLOT0_1	XX16
026216	CAN1 Message Slot Buffer 0 Extended ID0	C1SLOT0_2	XX16
026316	CAN1 Message Slot Buffer 0 Extended ID1	C1SLOT0_3	XX16
026416	CAN1 Message Slot Buffer 0 Extended ID2	C1SLOT0_4	XX16
026516	CAN1 Message Slot Buffer 0 Data Length Code	C1SLOT0_5	XX16
026616	CAN1 Message Slot Buffer 0 Data 0	C1SLOT0_6	XX16
026716	CAN1 Message Slot Buffer 0 Data 1	C1SLOT0_7	XX16
026816	CAN1 Message Slot Buffer 0 Data 2	C1SLOT0_8	XX16
026916	CAN1 Message Slot Buffer 0 Data 3	C1SLOT0_9	XX16
026A16	CAN1 Message Slot Buffer 0 Data 4	C1SLOT0_10	XX16
026B16	CAN1 Message Slot Buffer 0 Data 5	C1SLOT0_11	XX16
026C16	CAN1 Message Slot Buffer 0 Data 6	C1SLOT0_12	XX16
026D16	CAN1 Message Slot Buffer 0 Data 7	C1SLOT0_13	XX16
026E16	CAN1 Message Slot Buffer 0 Time Stamp High-Order	C1SLOT0_14	XX16
026F16	CAN1 Message Slot Buffer 0 Time Stamp Low-Order	C1SLOT0_15	XX16
027016	CAN1 Message Slot Buffer 1 Standard ID0	C1SLOT1_0	XX16
027116	CAN1 Message Slot Buffer 1 Standard ID1	C1SLOT1_1	XX16
027216	CAN1 Message Slot Buffer 1 Extended ID0	C1SLOT1_2	XX16
027316	CAN1 Message Slot Buffer 1 Extended ID1	C1SLOT1_3	XX16
027416	CAN1 Message Slot Buffer 1 Extended ID2	C1SLOT1_4	XX16
027516	CAN1 Message Slot Buffer 1 Data Length Code	C1SLOT1_5	XX16
027616	CAN1 Message Slot Buffer 1 Data 0	C1SLOT1_6	XX16
027716	CAN1 Message Slot Buffer 1 Data 1	C1SLOT1_7	XX16
027816	CAN1 Message Slot Buffer 1 Data 2	C1SLOT1_8	XX16
027916	CAN1 Message Slot Buffer 1 Data 3	C1SLOT1_9	XX16
027A16	CAN1 Message Slot Buffer 1 Data 4	C1SLOT1_10	XX16
027B16	CAN1 Message Slot Buffer 1 Data 5	C1SLOT1_11	XX16
027C16	CAN1 Message Slot Buffer 1 Data 6	C1SLOT1_12	XX16
027D16	CAN1 Message Slot Buffer 1 Data 7	C1SLOT1_13	XX16
027E16	CAN1 Message Slot Buffer 1 Time Stamp High-Order	C1SLOT1_14	XX16
027F16	CAN1 Message Slot Buffer 1 Time Stamp Low-Order	C1SLOT1_15	XX16
028016 028116	CAN1 Control Register 0	C1CTLR0	XX01 0X012(1) XXXX 00002(1)
028216 028316	CAN1 Status Register	C1STR	0000 00002(1) X000 0X012(1)
028416 028516	CAN1 Extended ID Register	C1IDR	0016(1) 0016(1)
028616 028716	CAN1 Configuration Register	C1CONR	0000 XXXX2(1) 0000 00002(1)
028816 028916	CAN1 Time Stamp Register	C1TSR	0016(1) 0016(1)
028A16	CAN1 Transmit Error Count Register	C1TEC	0016(1)
028B16	CAN1 Receive Error Count Register	C1REC	0016(1)
028C16 028D16	CAN1 Slot Interrupt Status Register	C1SISTR	0016(1) 0016(1)
028E16			
028F16			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTES:

1. Values are obtained by setting the SLEEP bit in the C1SLPR register to "1" (sleep mode exited) after reset and supplying the clock to the CAN module.

Address	Register	Symbol	Value after RESET
029016 029116	CAN1 Slot Interrupt Mask Register	C1SIMKR	0016 0016
029216			
029316			
029416	CAN1 Error Interrupt Mask Register	C1EIMKR	XXXX X0002(2)
029516	CAN1 Error Interrupt Status Register	C1EISTR	XXXX X0002(2)
029616	CAN1 Error Factor Register	C1EFR	0016(2)
029716	CAN1 Baud Rate Prescaler	C1BRP	0000 00012(2)
029816			
029916	CAN1 Mode Register	C1MDR	XXXX XX002(2)
029A16			
029B16			
029C16			
029D16			
029E16			
029F16			
02A016 02A116	CAN1 Single Shot Control Register	C1SSCTLR	0016(2) 0016(2)
02A216			
02A316			
02A416 02A516	CAN1 Single Shot Status Register	C1SSSTR	0016(2) 0016(2)
02A616			
02A716			
02A816	CAN1 Global Mask Register Standard ID0	C1GMR0	XXX0 00002(2)
02A916	CAN1 Global Mask Register Standard ID1	C1GMR1	XX00 00002(2)
02AA16	CAN1 Global Mask Register Extended ID0	C1GMR2	XXXX 00002(2)
02AB16	CAN1 Global Mask Register Extended ID1	C1GMR3	0016(2)
02AC16	CAN1 Global Mask Register Extended ID2	C1GMR4	XX00 00002(2)
02AD16			
02AE16			
02AF16			
02B016	CAN1 Message Slot 0 Control Register / CAN1 Local Mask Register A Standard ID0	C1MCTL0/ C1LMAR0	0000 00002(2) XXX0 00002(2)
02B116	CAN1 Message Slot 1 Control Register / CAN1 Local Mask Register A Standard ID1	C1MCTL1/ C1LMAR1	0000 00002(2) XX00 00002(2)
02B216	CAN1 Message Slot 2 Control Register / CAN1 Local Mask Register A Extended ID0	C1MCTL2/ C1LMAR2	0000 00002(2) XXXX 00002(2)
02B316	CAN1 Message Slot 3 Control Register / CAN1 Local Mask Register A Extended ID1	C1MCTL3/ C1LMAR3	0016(2) 0016(2)
02B416	CAN1 Message Slot 4 Control Register / CAN1 Local Mask Register A Extended ID2	C1MCTL4/ C1LMAR4	0000 00002(2) XX00 00002(2)
02B516	CAN1 Message Slot 5 Control Register	C1MCTL5	0016(2)
02B616	CAN1 Message Slot 6 Control Register	C1MCTL6	0016(2)
02B716	CAN1 Message Slot 7 Control Register	C1MCTL7	0016(2)
02B816	CAN1 Message Slot 8 Control Register / CAN1 Local Mask Register B Standard ID0	C1MCTL8/ C1LMBR0	0000 00002(2) XXX0 00002(2)
02B916	CAN1 Message Slot 9 Control Register / CAN1 Local Mask Register B Standard ID1	C1MCTL9/ C1LMBR1	0000 00002(2) XX00 00002(2)

(Note 1)

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTES:

1. The BANKSEL bit in the C1CTLR1 register switches functions for addresses 02A016 to 02BF16.
2. Values are obtained by setting the SLEEP bit in the C1SLPR register to "1" (sleep mode exited) after reset and applying the clock to the CAN module.

<100-pin package>

Address	Register	Symbol	Value after RESET
03A0$_{16}$			
03A1$_{16}$			
03A2$_{16}$			
03A3$_{16}$			
03A4$_{16}$			
03A5$_{16}$			
03A6$_{16}$			
03A7$_{16}$	Function Select Register D1	PSD1	X0XX XX00$_2$
03A8$_{16}$			
03A9$_{16}$			
03AA$_{16}$			
03AB$_{16}$			
03AC$_{16}$	Function Select Register C2	PSC2	XXXX X00X$_2$
03AD$_{16}$	Function Select Register C3	PSC3	X0XX XXXX$_2$
03AE$_{16}$			
03AF$_{16}$	Function Select Register C	PSC	00X0 0000$_2$
03B0$_{16}$	Function Select Register A0	PS0	00$_{16}$
03B1$_{16}$	Function Select Register A1	PS1	00$_{16}$
03B2$_{16}$	Function Select Register B0	PSL0	00$_{16}$
03B3$_{16}$	Function Select Register B1	PSL1	00$_{16}$
03B4$_{16}$	Function Select Register A2	PS2	00X0 0000$_2$
03B5$_{16}$	Function Select Register A3	PS3	00$_{16}$
03B6$_{16}$	Function Select Register B2	PSL2	00X0 0000$_2$
03B7$_{16}$	Function Select Register B3	PSL3	00$_{16}$
03B8$_{16}$			
03B9$_{16}$			
03BA$_{16}$			
03BB$_{16}$			
03BC$_{16}$			
03BD$_{16}$			
03BE$_{16}$			
03BF$_{16}$			
03C0$_{16}$	Port P6 Register	P6	XX$_{16}$
03C1$_{16}$	Port P7 Register	P7	XX$_{16}$
03C2$_{16}$	Port P6 Direction Register	PD6	00$_{16}$
03C3$_{16}$	Port P7 Direction Register	PD7	00$_{16}$
03C4$_{16}$	Port P8 Register	P8	XX$_{16}$
03C5$_{16}$	Port P9 Register	P9	XX$_{16}$
03C6$_{16}$	Port P8 Direction Register	PD8	00X0 0000$_2$
03C7$_{16}$	Port P9 Direction Register	PD9	00$_{16}$
03C8$_{16}$	Port P10 Register	P10	XX$_{16}$
03C9$_{16}$			
03CA$_{16}$	Port P10 Direction Register	PD10	00$_{16}$
03CB$_{16}$	Set default value to "FF$_{16}$"		
03CC$_{16}$			
03CD$_{16}$			
03CE$_{16}$	Set default value to "FF$_{16}$"		
03CF$_{16}$	Set default value to "FF$_{16}$"		

X: Indeterminate

Blank spaces are reserved. No access is allowed.

$V_{CC1}=V_{CC2}=5V$

Table 5.3 Electrical Characteristics (Continued)

($V_{CC1}=V_{CC2}=4.2$ to 5.5V, $V_{SS}=0V$ at Topr= –20 to 85°C, f(BCLK)=32MHz unless otherwise specified)

Symbol	Parameter	Measurement Condition		Standard			Unit
				Min.	Typ.	Max.	
I_{CC}	Power Supply Current	In single-chip mode, output pins are left open and other pins are connected to V_{SS}.	f(BCLK)=32 MHz, Square wave, No division		28	45	mA
			f(BCLK)=32 kHz, In low-power consumption mode, Program running on ROM — Flash Memory		430		µA
			f(BCLK)=32 kHz, In low-power consumption mode, Program running on ROM — Masked ROM		25		µA
			f(BCLK)=32 kHz, In low-power consumption mode, Program running on RAM(1)		25		µA
			f(BCLK)=32 kHz, In wait mode, Topr=25° C		10		µA
			While clock stops, Topr=25° C		0.8	5	µA
			While clock stops, Topr=85° C			50	µA

NOTES:

1. Value is obtained when setting the FMSTP bit in the FMR0 register to "1" (flash memory stopped).

$V_{CC1}=V_{CC2}=5V$

Switching Characteristics

(V_{CC1} = V_{CC2} = 4.2 to 5.5V, V_{SS} = 0V at Topr = –20 to 85°C unless otherwise specified)

Table 5.22 Memory Expansion Mode and Microprocessor Mode (when accessing external memory space)

Symbol	Parameter	Measurement Condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address Output Delay Time	See Figure 5.2		18	ns
$t_{h(BCLK-AD)}$	Address Output Hold Time (BCLK standard)		-3		ns
$t_{h(RD-AD)}$	Address Output Hold Time (RD standard)(3)		0		ns
$t_{h(WR-AD)}$	Address Output Hold Time (WR standard)(3)		(Note 1)		ns
$t_{d(BCLK-CS)}$	Chip-Select Signal Output Delay Time			18	ns
$t_{h(BCLK-CS)}$	Chip-Select Signal Output Hold Time (BCLK standard)		-3		ns
$t_{h(RD-CS)}$	Chip-Select Signal Output Hold Time (RD standard)(3)		0		ns
$t_{h(WR-CS)}$	Chip-Select Signal Output Hold Time (WR standard)(3)		(Note 1)		ns
$t_{d(BCLK-RD)}$	RD Signal Output Delay Time			18	ns
$t_{h(BCLK-RD)}$	RD Signal Output Hold Time		-5		ns
$t_{d(BCLK-WR)}$	WR Signal Output Delay Time			18	ns
$t_{h(BCLK-WR)}$	WR Signal Output Hold Time		-5		ns
$t_{d(DB-WR)}$	Data Output Delay Time (WR standard)		(Note 2)		ns
$t_{h(WR-DB)}$	Data Output Hold Time (WR standard)(3)		(Note 1)		ns
$t_{w(WR)}$	WR Output Width		(Note 2)		ns

NOTES:

1. Values can be obtained from the following equations, according to BCLK frequency.

$$t_{h(WR-DB)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$t_{h(WR-AD)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$t_{h(WR-CS)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

2. Values can be obtained from the following equations, according to BCLK frequency and external bus cycles.

$$t_{w(WR)} = \frac{10^9 \times n}{f_{(BCLK)} \times 2} - 15 \quad [ns]$$ (if external bus cycle is aϕ + bϕ, n=(bx2)-1)

$$t_{d(DB-WR)} = \frac{10^9 \times m}{f_{(BCLK)}} - 20 \quad [ns]$$ (if external bus cycle is aϕ + bϕ, m= b)

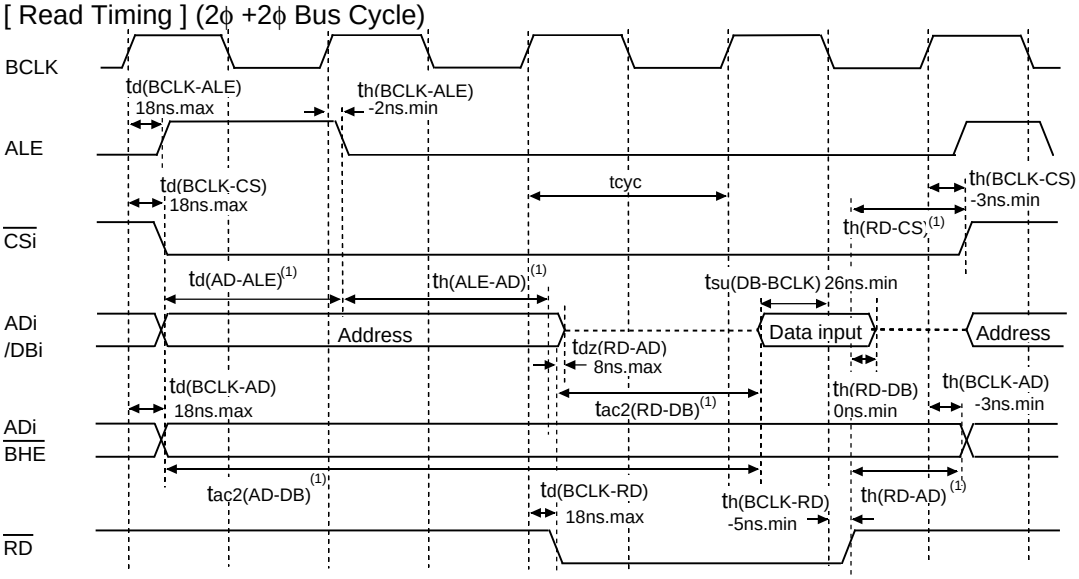
3. *tc* ns is added when recovery cycle is inserted.

$V_{CC1}=V_{CC2}=5V$

Memory Expansion Mode and Microprocessor Mode

(when accessing an external memory space with the multiplexed bus)

[Read Timing] (2φ +2φ Bus Cycle)



NOTES:

1. Varies with operation frequency:

$t_{d(AD-ALE)}$=(tcyc/2 x n-20)ns.min (if external bus cycle is aφ + bφ, n=a)

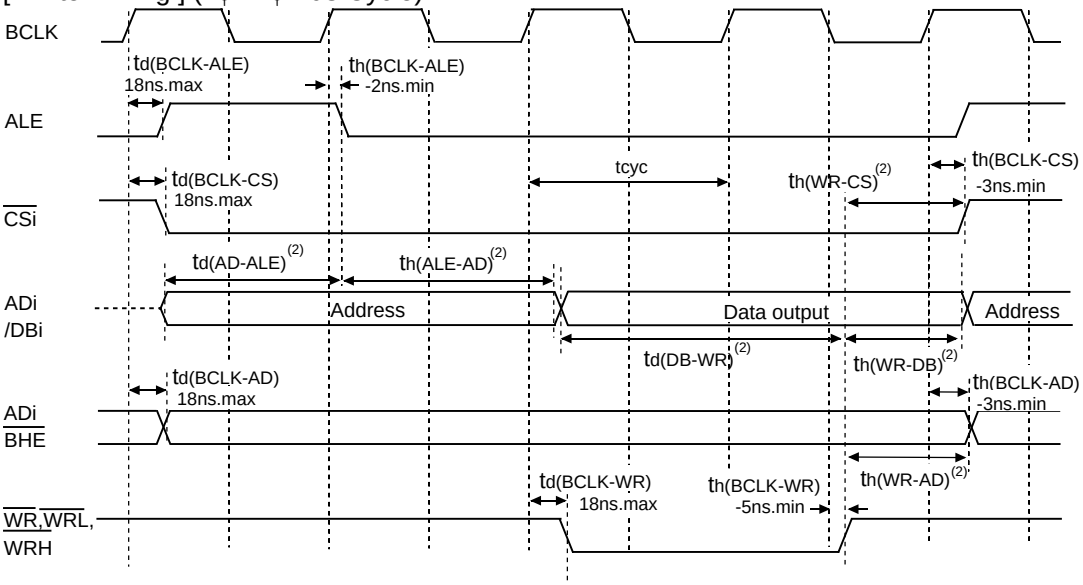
$t_{h(ALE-AD)}$=(tcyc/2 x n-10)ns.min (if external bus cycle is aφ + bφ, n=a)

$t_{h(RD-AD)}$=(tcyc/2-10)ns.min, $t_{h(RD-CS)}$=(tcyc/2-10)ns.min

$t_{ac2(RD-DB)}$=(tcyc/2 x m-35)ns.max (if external bus cycle is aφ + bφ, m=(b x 2)-1)

$t_{ac2(AD-DB)}$=(tcyc/2 x p-35)ns.max (if external bus cycle is aφ + bφ, p={(a+b-1) x 2}+1)

[Write Timing] (2φ +2φ Bus Cycle)



NOTES:

2. Varies with operation frequency:

$t_{d(AD-ALE)}$=(tcyc/2 x n - 20)ns.min

(if external bus cycle is aφ + bφ, n=a)

$t_{h(ALE-AD)}$=(tcyc/2 x n -10)ns.min

(if external bus cycle is aφ + bφ, n=a)

$t_{h(WR-AD)}$=(tcyc/2-10)ns.min,

$t_{h(WR-CS)}$=(tcyc/2-10)ns.min, $t_{h(WR-DB)}$=(tcyc/2-10)ns.min

$t_{d(DB-WR)}$=(tcyc/2 x m-25)ns.min

(if external bus cycle is aφ + bφ, m=(b x 2)-1)

Measurement Conditions:

- $V_{CC1}=V_{CC2}$=4.2 to 5.5V
- Input high and low voltage: V_{IH}=2.5V, V_{IL}=0.8V
- Output high and low voltage: V_{OH}=2.0V, V_{OL}=0.8V

$$tcyc=\frac{10^9}{f_{(BCLK)}}$$

Figure 5.4 $V_{CC1}=V_{CC2}$=5V Timing Diagram (2)

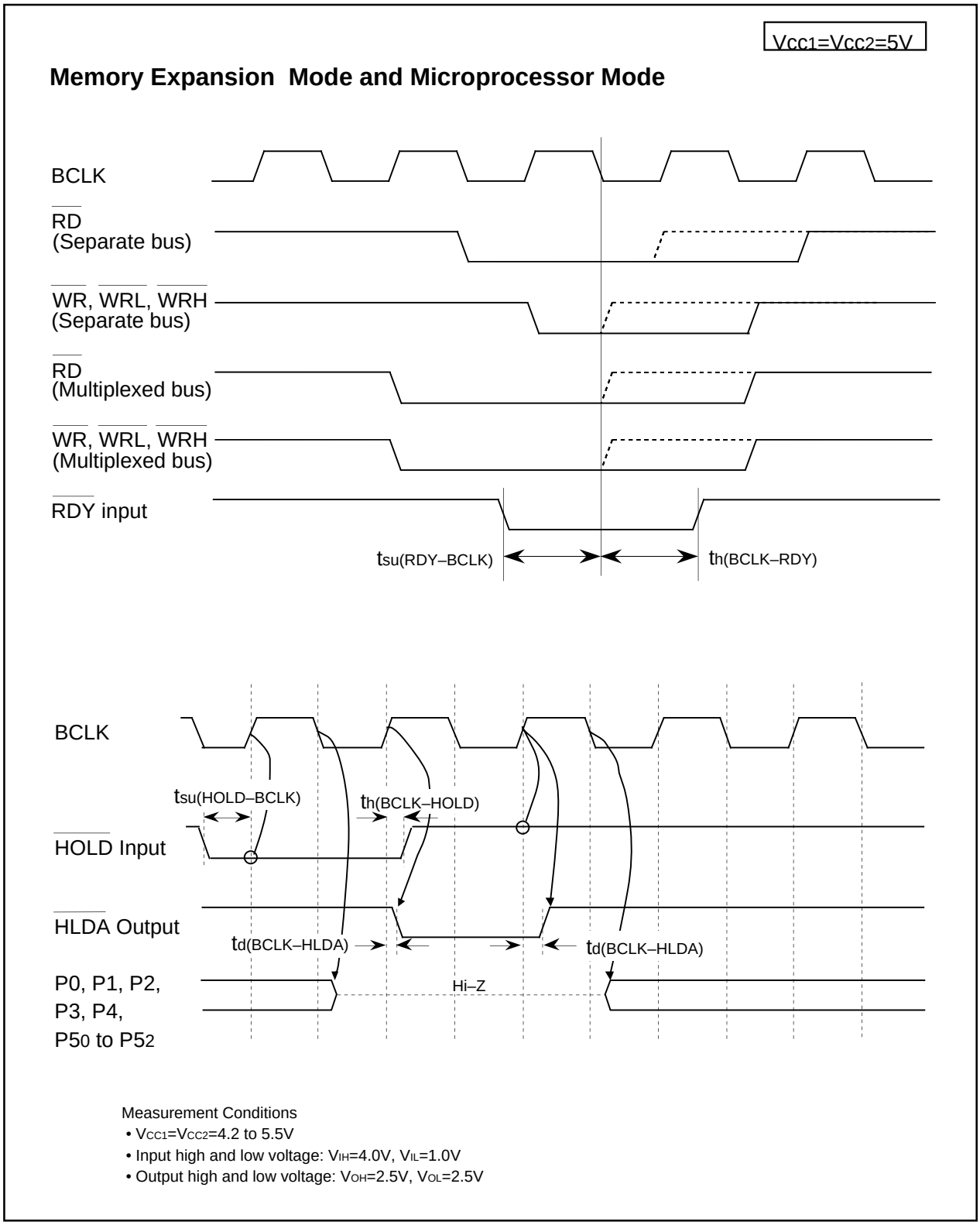


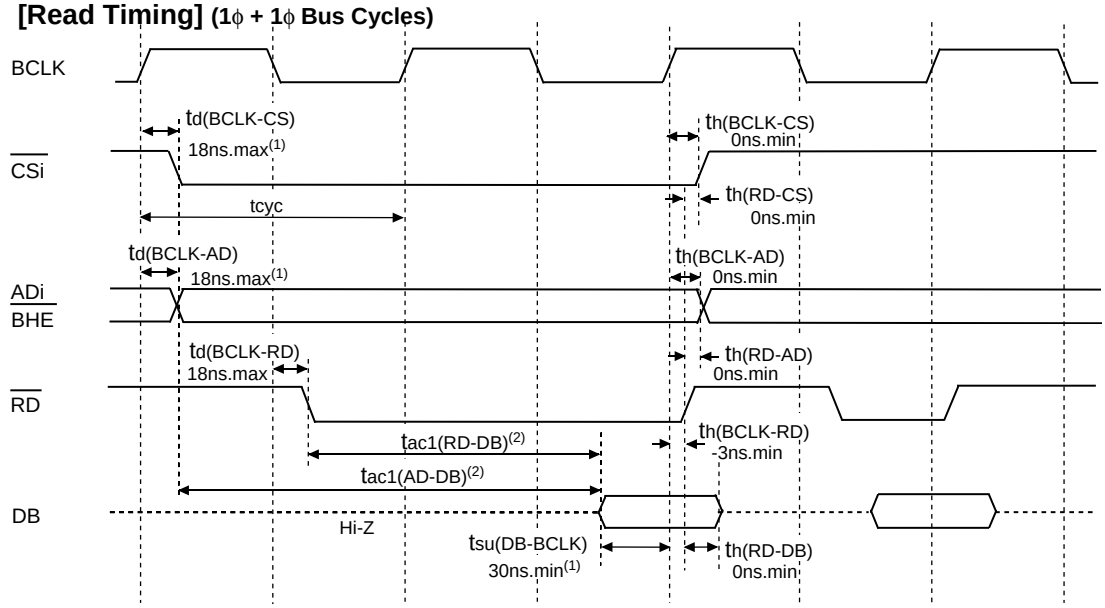
Figure 5.6 Vcc1=Vcc2=5V Timing Diagram (4)

Vcc1=Vcc2=3.3V

Memory Expansion Mode and Microprocessor Mode

(when accessing an external memory space)

[Read Timing] (1φ + 1φ Bus Cycles)



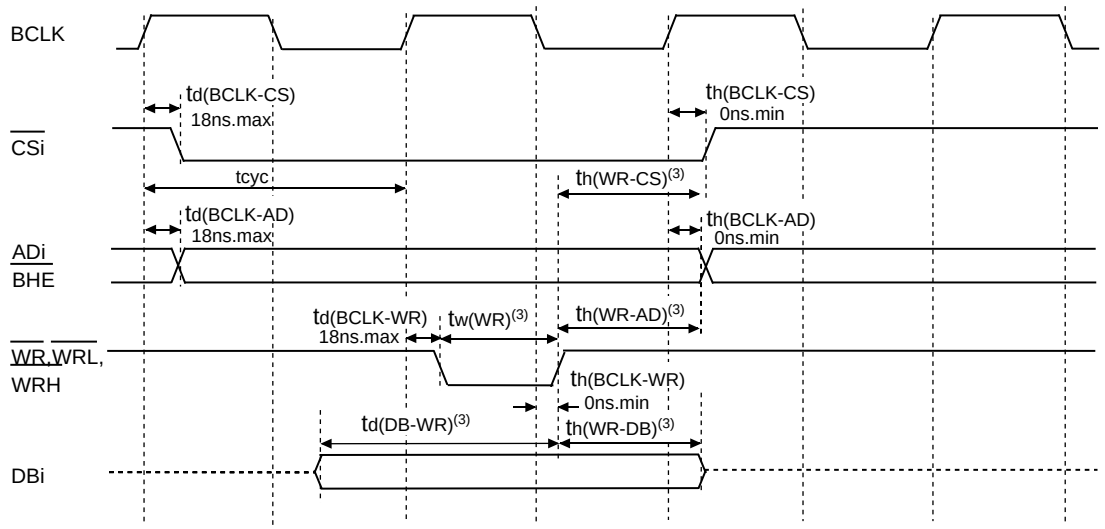
NOTES:

1. Values guaranteed only when the microcomputer is used independently.
   A maximum of 35ns is guaranteed for $t_{d(BCLK-AD)}+t_{su(DB-BCLK)}$.
2. Varies with operation frequency.

   $t_{ac1(RD-DB)}$=(tcyc/2 x m-35)ns.max (if external bus cycle is aφ + bφ, m=(b x 2) + 1)

   $t_{ac1(AD-DB)}$=(tcyc x n-35)ns.max (if external bus cycle is aφ + bφ, n = a + b)

[Write Timing] (1φ + 1φ Bus Cycles)



NOTES:

3. Varies with operation frequency.

   $t_{d(DB-WR)}$=(tcyc x m-20)ns.min

   (if external bus cycle is aφ + bφ, m=b)

   $t_{h(WR-DB)}$=(tcyc/2-20)ns.min

   $t_{h(WR-AD)}$=(tcyc/2-10)ns.min

   $t_{h(WR-CS)}$=(tcyc/2-10)ns.min

   $t_{w(WR)}$=(tcyc/2 x n-15)ns.min

   (if external bus cycle is aφ + bφ, n=(bx2)-1)

Measurement Conditions

- V_{CC1}=V_{CC2}=3.0 to 3.6V
- Input high and low voltage: V_{IH}=1.5V, V_{IL}=0.5V
- Output high and low voltage: V_{OH}=1.5V, V_{OL}=1.5V

$$tcyc = \frac{10^9}{f(BCLK)}$$

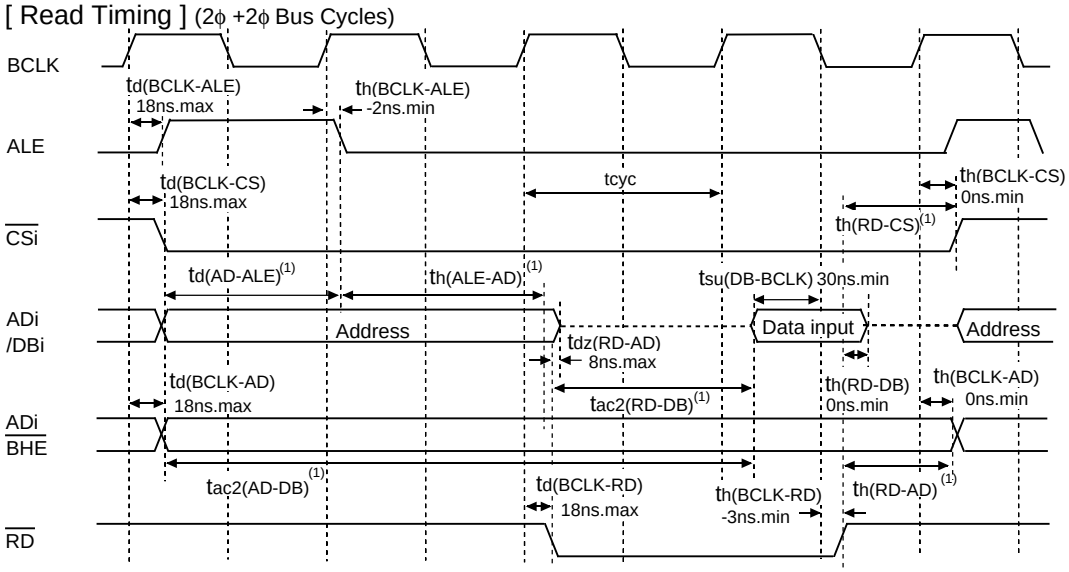
Figure 5.7 V_{CC1}=V_{CC2}=3.3V Timing Diagram (1)

Memory Expansion Mode and Microprocessor Mode

Vcc1=Vcc2=3.3V

(when accessing external memory space and using the multiplexed bus)

[Read Timing] (2ϕ +2ϕ Bus Cycles)



NOTES:

1. Varies with operation frequency:

$t_{d(AD-ALE)}$=(tcyc/2 x n-20)ns.min (if external bus cycle is aϕ + bϕ, n=a)

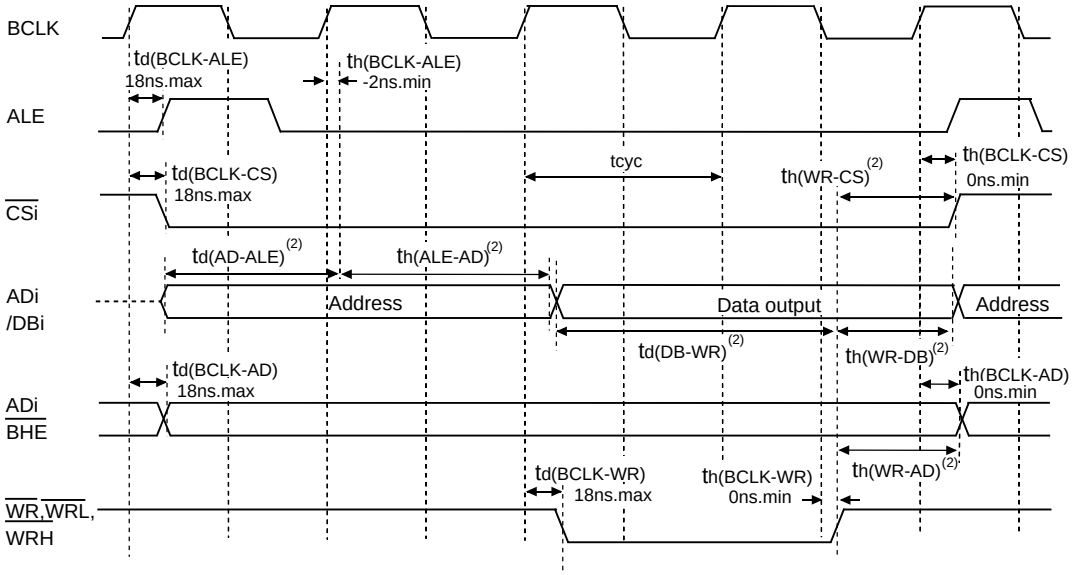
$t_{h(ALE-AD)}$=(tcyc/2 x n-10)ns.min (if external bus cycle is aϕ + bϕ, n=a)

$t_{h(RD-AD)}$=(tcyc/2-10)ns.min, $t_{h(RD-CS)}$=(tcyc/2-10)ns.min

$t_{ac2(RD-DB)}$=(tcyc/2 x m-35)ns.max (if external bus cycle is aϕ + bϕ, m=(b x 2)-1)

$t_{ac2(AD-DB)}$=(tcyc/2 x p-35)ns.max (if external bus cycle is aϕ + bϕ, p={(a+b-1) x 2}+1)

[Write Timing] (2ϕ +2ϕ Bus Cycles)



NOTES:

2. Varies with operation frequency:

$t_{d(AD-ALE)}$=(tcyc/2 x n - 20)ns.min

(if external bus cycle is aϕ + bϕ, n=a)

$t_{h(ALE-AD)}$=(tcyc/2 x n -10)ns.min

(if external bus cycle is aϕ + bϕ, n=a)

$t_{h(WR-AD)}$=(tcyc/2-10)ns.min,

$t_{h(WR-CS)}$=(tcyc/2-10)ns.min, $t_{h(WR-DB)}$=(tcyc/2-20)ns.min

$t_{d(DB-WR)}$=(tcyc/2 x m-25)ns.min

(if external bus cycle is aϕ + bϕ, m=(b x 2)-1)

Measurement Conditions:

- V_{CC1}=V_{CC2}=3.0 to 3.6V
- Input high and low voltage:
  V_{IH}=1.5V, V_{IL}=0.5V
- Output high and low voltage:
  V_{OH}=1.5V, V_{OL}=1.5V

$$tcyc = \frac{10^9}{f_{(BCLK)}}$$

Figure 5.8 V_{CC1}=V_{CC2}=3.3V Timing Diagram (2)

$V_{CC1}=V_{CC2}=5V$

Table 5.45 A/D Conversion Characteristics ($V_{CC1}=V_{CC2}=4.2$ to 5.5V, $V_{SS}=0V$ at Topr= -40 to 85°C (T version), f(BCLK)=32MHz unless otherwise specified)

Symbol	Parameter	Measurement Condition		Standard			Unit
				Min.	Typ.	Max.	
-	Resolution	$V_{REF}=V_{CC1}$				10	Bits
INL	Integral Nonlinearity Error	$V_{REF}=V_{CC1}=V_{CC2}=5V$	AN_0 to AN_7, $AN0_0$ to $AN0_7$, $AN2_0$ to $AN2_7$, $AN15_0$ to $AN15_7$, ANEX0, ANEX1			±3	LSB
							LSB
			External op-amp connection mode			±7	LSB
							LSB
DNL	Differential Nonlinearity Error					±1	LSB
-	Offset Error					±3	LSB
-	Gain Error					±3	LSB
R_{LADDER}	Resistor Ladder	$V_{REF}=V_{CC1}$		8		40	kΩ
t_{CONV}	10-bit Conversion Time(1, 2)			2.06			µs
t_{CONV}	8-bit Conversion Time(1, 2)			1.75			µs
t_{SAMP}	Sampling Time(1)			0.188			µs
V_{REF}	Reference Voltage			2		V_{CC1}	V
V_{IA}	Analog Input Voltage			0		V_{REF}	V

NOTES:
1. Divide f(X_{IN}), if exceeding 16 MHz, to keep ϕAD frequency at 16 MHz or less.
2. With using the sample and hold function.

Table 5.46 D/A Conversion Characteristics ($V_{CC1}=V_{CC2}=4.2$ to 5.5V, $V_{SS}=0V$ at Topr= -40 to 85°C (T version), f(BCLK)=32MHz unless otherwise specified)

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min.	Typ.	Max.	
-	Resolution				8	Bits
-	Absolute Accuracy				1.0	%
t_{SU}	Setup Time				3	µs
R_O	Output Resistance		4	10	20	kΩ
I_{VREF}	Reference Power Supply Input Current	(Note 1)			1.5	mA

NOTES:
1. Measurement when using one D/A converter. The DAi register (i=0, 1) of the D/A converter, not being used, is set to "00_{16}". The resistor ladder in the A/D converter is excluded.
I_{VREF} flows even if the VCUT bit in the AD0CON1 register is set to "0" (no V_{REF} connection).

$V_{CC1}=V_{CC2}=5V$

Timing Requirements

($V_{CC1}=V_{CC2}=4.2$ to 5.5V, $V_{SS}=0V$ at Topr= -40 to 85°C (T version) unless otherwise specified)

Table 5.49 External Clock Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc	External Clock Input Cycle Time	31.25		ns
$tw_{(H)}$	External Clock Input High ("H") Width	13.75		ns
$tw_{(L)}$	External Clock Input Low ("L") Width	13.75		ns
tr	External Clock Rise Time		5	ns
tf	External Clock Fall Time		5	ns

REVISION HISTORY	M32C/85 Group (M32C/85, M32C/85T) Datasheet

Rev.	Date	Description	
		Page	Summary
0.30	Jul.18, 2003	–	New Document
0.40	Sep.30, 2003		**Overview**
		2 to 3	• **Tables 1.1 and 1.2 M32C/85 Performance** "Oscillator Stop Detect Function" added
		5	• **Figure 1.2 ROM/RAM Capacity** and **Table 1.3. M32C/85 Group** M30852ME-XXXGP and M30850ME-XXXGP/FP deleted
		6	• ROM capacity "192 Kbytes" deleted
		7, 11, 12	• **Figures 1.4** to **1.6 Pin Assignments** Note 2 added
		10,14	- VREF pin changed from analog input pins to control pins.
		16 to 18	- SDA0 to SDA4 pins changed from output pins to I/O pins.
		17	- TA4OUT changed from input pin to I/O pin. - TA4IN pin changed from output pin to input pin. - ISRxD1 pin modified to ISRxD0 pin in port P8.
		18	- DA0 and DA1 pins changed from input pins to output pins.
		19	- Symbol "P117" modified to "P114" and description from "8-bit" to "5-bit". - Descriptions of ISTxD1 and BE1IN modified from "received data" to "transmit data".
			SFR
		44,45	- Notes written directly in the Tables.
0.50	Feb.05, 2004		**Overview**
		2, 3	• **Tables 1.1 and 1.2 M32C/85 Performance** "Shortest Instruction Execution Time" and "Power Comsumption" values modified
			Memory
		23	• **Figure 3.1 Memory Map** Diagram modified
			SFR
		24	• "After RESET" values of PM 1, PM 2, D4INT, G0IRF, G1IRF, IDB0 to IDB1, TA0MR to TA4MR, TCSPR, DM0SL to DM3SL registers corrected • NOTES added to PM0 and TCSPR registers
			Electrical Characteristics
			• Newly added
0.51	Feb.09, 2004		**Electrical Characteristics**
		52	• **Table 5.6 Flash Memory Version Electrical Characteristics** Note 4 changed
		59	• **Figure 5.2 Vcc1=Vcc2=5V Timing Diagram (1)** Notes 1 and 2 changed
		60	• **Figure 5.3 Vcc1=Vcc2=5V Timing Diagram (2)** Notes 1, 2, and 3 changed
		70	• **Figure 5.6 Vcc1=Vcc2=3.3V Timing Diagram (1)** Notes 1, 2, and 3 changed
		71	• **Figure 5.7 Vcc1=Vcc2=3.3V Timing Diagram (2)** Notes 1 and 2 changed
0.52	Mar.12, 2004		**Overview**
		2, 3	• **Table 1.1 and 1.2 M32C/85 Group Performance** Value of Power Consumption modified

REVISION HISTORY	M32C/85 Group (M32C/85, M32C/85T) Datasheet

Rev.	Date	Description	
		Page	Summary
		49	• **Table 5.3 Electrical Characteristics** Maximum ICC value modified
		50	• **Table 5.4 A/D Conversion Characteristics** tSMP value modified; note 1 added
		52	• **Table 5.7 Low Voltage Detect Circuit Electrical Characteristics** added
			• **Table 5.8 Power Supply Timing** added
			• **Figure 5.1 Power Supply Timing Diagram** added
		57	• **Table 5.23 Memory Expassion Mode and Microprocessor Mode** th(BCLK-ALE) value modified
		63	• **Table 5.24 Electrical Characteristics** Maximum ICC value modified
		61	• **Table 5.24 Electrical Characteristics** RPULLUP value for the masked ROM version added
		64	• **Table 5.25 A/D Conversion Characteristics** tCONV value modified
		65	• **Table 5.28 Memory Expassion Mode and Microprocessor Mode** tsu(DB-BCLK), tsu(RDY-BCLK) and tsu(HOLD-BCLK) value modified
		68	• **Table 5.40 Memory Expassion Mode and Microprocessor Mode** equetion of th(WR-DB) modified
		69	• **Table 5.41 Memory Expassion Mode and Microprocessor Mode** th(BCLK-ALE) value modified; equetion of th(WR-DB) modified
		74	• **5.2 Electrical Characteristics (M32C/85T)** added
1.10	Jun.28, 2004	-	**High-reliability version (U version)** deleted
			Overview
		5	• **Table 1.3 M32C/85 Group (1) (2)** development status modified
		6	• **Figure 1.2 Product Numbering System** figure modified
1.20	Mar.30, 2005		**Memory**
			• **Figure 3.1 Memory Map** A sentence added to Note 3
			SFR
		24	• Value after reset of the RLVL register revised
		27	• Value after reset of the G0RB register revised
		29	• Value after reset of the G1BCR1 register revised
			• Value after reset of the G1RB register revised
		37	• Value after reset of the IDB0 register revised
			• Value after reset of the IDB1 register revised
		43	• Value after reset of the PSC register revised
			Electrical Characteristics
		49	• **Table 5.3 Electrical Characteristics** ICC standard value revised
		51	• **Table 5.6 Flash Memory Electrical Characteristics** Topr value modified
		52	• **Table 5.7 Voltage Detection Circuit Electrical Characteristics** VCC1 value modified
		60	• **Figure 5.4 VCC1=VCC2=5V Timing Diagram (2)** Diagram modified
		63	• **Table 5.24 Electrical Characteristics** ICC standard value revised