Renesas Electronics America Inc - M30855FJGP#U5 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	M32C/80
Core Size	16/32-Bit
Speed	32MHz
Connectivity	CANbus, I²C, IEBus, SIO, UART/USART
Peripherals	DMA, WDT
Number of I/O	121
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 34x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LFQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m30855fjgp-u5

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1. Overview

The M32C/85 group (M32C/85, M32C/85T) microcomputer is a single-chip control unit that utilizes high-performance silicon gate CMOS technology with the M32C/80 series CPU core. The M32C/85 group (M32C/85, M32C/85T) is available in 144-pin and 100-pin plastic molded LQFP/QFP packages.

With a 16-Mbyte address space, this microcomputer combines advanced instruction manipulation capabilities to process complex instructions by less bytes and execute instructions at higher speed.

It includes a multiplier and DMAC adequate for office automation, communication devices and industrial equipments, and other high-speed processing applications.

1.1 Applications

Automobiles, audio, cameras, office equipment, communications equipment, portable equipment, etc.

1.5 Pin Assignments and Descriptions

Figures 1.3 to 1.5 show pin assignments (top view).

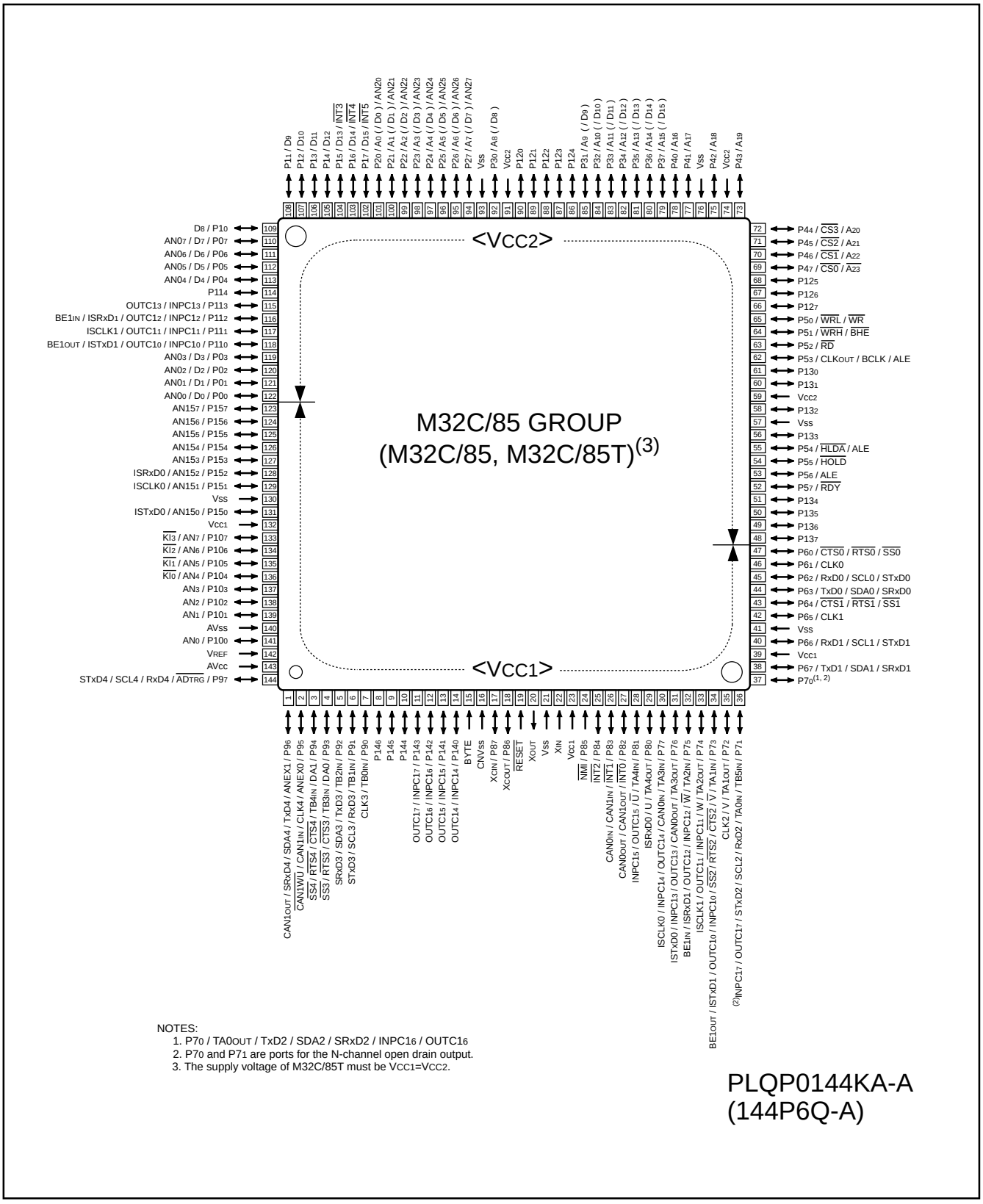

Figure 1.3 Pin Assignment for 144-Pin Package

Table 1.5 Pin Characteristics for 100-Pin Package (Continued)

Package Pin No.		Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin(1)
FP	GP								
51	49		$P4_3$						A_{19}
52	50		$P4_2$						A_{18}
53	51		$P4_1$						A_{17}
54	52		$P4_0$						A_{16}
55	53		$P3_7$						A_{15}(/D_{15})
56	54		$P3_6$						A_{14}(/D_{14})
57	55		$P3_5$						A_{13}(/D_{13})
58	56		$P3_4$						A_{12}(/D_{12})
59	57		$P3_3$						A_{11}(/D_{11})
60	58		$P3_2$						A_{10}(/D_{10})
61	59		$P3_1$						A_9(/D_9)
62	60	V_{CC2}							
63	61		$P3_0$						A_8(/D_8)
64	62	V_{SS}							
65	63		$P2_7$					$AN2_7$	A_7(/D_7)
66	64		$P2_6$					$AN2_6$	A_6(/D_6)
67	65		$P2_5$					$AN2_5$	A_5(/D_5)
68	66		$P2_4$					$AN2_4$	A_4(/D_4)
69	67		$P2_3$					$AN2_3$	A_3(/D_3)
70	68		$P2_2$					$AN2_2$	A_2(/D_2)
71	69		$P2_1$					$AN2_1$	A_1(/D_1)
72	70		$P2_0$					$AN2_0$	A_0(/D_0)
73	71		$P1_7$	$\overline{INT5}$					D_{15}
74	72		$P1_6$	$\overline{INT4}$					D_{14}
75	73		$P1_5$	$\overline{INT3}$					D_{13}
76	74		$P1_4$						D_{12}
77	75		$P1_3$						D_{11}
78	76		$P1_2$						D_{10}
79	77		$P1_1$						D_9
80	78		$P1_0$						D_8
81	79		$P0_7$					$AN0_7$	D_7
82	80		$P0_6$					$AN0_6$	D_6
83	81		$P0_5$					$AN0_5$	D_5
84	82		$P0_4$					$AN0_4$	D_4
85	83		$P0_3$					$AN0_3$	D_3
86	84		$P0_2$					$AN0_2$	D_2
87	85		$P0_1$					$AN0_1$	D_1
88	86		$P0_0$					$AN0_0$	D_0
89	87		$P10_7$	$\overline{KI_3}$				AN_7	
90	88		$P10_6$	$\overline{KI_2}$				AN_6	
91	89		$P10_5$	$\overline{KI_1}$				AN_5	
92	90		$P10_4$	$\overline{KI_0}$				AN_4	
93	91		$P10_3$					AN_3	
94	92		$P10_2$					AN_2	
95	93		$P10_1$					AN_1	
96	94	AV_{SS}							
97	95		$P10_0$					AN_0	
98	96	V_{REF}							
99	97	AV_{CC}							
100	98		$P9_7$			RxD4/SCL4/STxD4		$\overline{ADTRG}$	

NOTES:

1. Bus control pins in M32C/85T cannot be used.

Address	Register	Symbol	Value after RESET
012016	Base Timer Register 1	G1BT	XX16
012116			XX16
012216	Base Timer Control Register 10	G1BCR0	0016
012316	Base Timer Control Register 11	G1BCR1	X000 000X2
012416	Time Measurement Prescaler Register 16	G1TPR6	0016
012516	Time Measurement Prescaler Register 17	G1TPR7	0016
012616	Function Enable Register 1	G1FE	0016
012716	Function Select Register 1	G1FS	0016
012816	SI/O Receive Buffer Register 1	G1RB	XXXX XXXX2
012916			X000 XXXX2
012A16	Transmit Buffer/Receive Data Register 1	G1TB/G1DR	XX16
012B16			
012C16	Receive Input Register 1	G1RI	XX16
012D16	SI/O Communication Mode Register 1	G1MR	0016
012E16	Transmit Output Register 1	G1TO	XX16
012F16	SI/O Communication Control Register 1	G1CR	0000 X0112
013016	Data Compare Register 10	G1CMP0	XX16
013116	Data Compare Register 11	G1CMP1	XX16
013216	Data Compare Register 12	G1CMP2	XX16
013316	Data Compare Register 13	G1CMP3	XX16
013416	Data Mask Register 10	G1MSK0	XX16
013516	Data Mask Register 11	G1MSK1	XX16
013616			
013716			
013816	Receive CRC Code Register 1	G1RCRC	XX16
013916			XX16
013A16	Transmit CRC Code Register 1	G1TCRC	0016
013B16			0016
013C16	SI/O Extended Mode Register 1	G1EMR	0016
013D16	SI/O Extended Receive Control Register 1	G1ERC	0016
013E16	SI/O Special Communication Interrupt Detection Register 1	G1IRF	0016
013F16	SI/O Extended Transmit Control Register 1	G1ETC	0000 0XXX2
014016			
014116			
014216			
014316			
014416			
014516			
014616			
014716			
014816			
014916			
014A16			
014B16			
014C16			
014D16			
014E16			
014F16			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
01E0₁₆	CAN0 Message Slot Buffer 0 Standard ID0	C0SLOT0_0	XX₁₆
01E1₁₆	CAN0 Message Slot Buffer 0 Standard ID1	C0SLOT0_1	XX₁₆
01E2₁₆	CAN0 Message Slot Buffer 0 Extended ID0	C0SLOT0_2	XX₁₆
01E3₁₆	CAN0 Message Slot Buffer 0 Extended ID1	C0SLOT0_3	XX₁₆
01E4₁₆	CAN0 Message Slot Buffer 0 Extended ID2	C0SLOT0_4	XX₁₆
01E5₁₆	CAN0 Message Slot Buffer 0 Data Length Code	C0SLOT0_5	XX₁₆
01E6₁₆	CAN0 Message Slot Buffer 0 Data 0	C0SLOT0_6	XX₁₆
01E7₁₆	CAN0 Message Slot Buffer 0 Data 1	C0SLOT0_7	XX₁₆
01E8₁₆	CAN0 Message Slot Buffer 0 Data 2	C0SLOT0_8	XX₁₆
01E9₁₆	CAN0 Message Slot Buffer 0 Data 3	C0SLOT0_9	XX₁₆
01EA₁₆	CAN0 Message Slot Buffer 0 Data 4	C0SLOT0_10	XX₁₆
01EB₁₆	CAN0 Message Slot Buffer 0 Data 5	C0SLOT0_11	XX₁₆
01EC₁₆	CAN0 Message Slot Buffer 0 Data 6	C0SLOT0_12	XX₁₆
01ED₁₆	CAN0 Message Slot Buffer 0 Data 7	C0SLOT0_13	XX₁₆
01EE₁₆	CAN0 Message Slot Buffer 0 Time Stamp High-Order	C0SLOT0_14	XX₁₆
01EF₁₆	CAN0 Message Slot Buffer 0 Time Stamp Low-Order	C0SLOT0_15	XX₁₆
01F0₁₆	CAN0 Message Slot Buffer 1 Standard ID0	C0SLOT1_0	XX₁₆
01F1₁₆	CAN0 Message Slot Buffer 1 Standard ID1	C0SLOT1_1	XX₁₆
01F2₁₆	CAN0 Message Slot Buffer 1 Extended ID0	C0SLOT1_2	XX₁₆
01F3₁₆	CAN0 Message Slot Buffer 1 Extended ID1	C0SLOT1_3	XX₁₆
01F4₁₆	CAN0 Message Slot Buffer 1 Extended ID2	C0SLOT1_4	XX₁₆
01F5₁₆	CAN0 Message Slot Buffer 1 Data Length Code	C0SLOT1_5	XX₁₆
01F6₁₆	CAN0 Message Slot Buffer 1 Data 0	C0SLOT1_6	XX₁₆
01F7₁₆	CAN0 Message Slot Buffer 1 Data 1	C0SLOT1_7	XX₁₆
01F8₁₆	CAN0 Message Slot Buffer 1 Data 2	C0SLOT1_8	XX₁₆
01F9₁₆	CAN0 Message Slot Buffer 1 Data 3	C0SLOT1_9	XX₁₆
01FA₁₆	CAN0 Message Slot Buffer 1 Data 4	C0SLOT1_10	XX₁₆
01FB₁₆	CAN0 Message Slot Buffer 1 Data 5	C0SLOT1_11	XX₁₆
01FC₁₆	CAN0 Message Slot Buffer 1 Data 6	C0SLOT1_12	XX₁₆
01FD₁₆	CAN0 Message Slot Buffer 1 Data 7	C0SLOT1_13	XX₁₆
01FE₁₆	CAN0 Message Slot Buffer 1 Time Stamp High-Order	C0SLOT1_14	XX₁₆
01FF₁₆	CAN0 Message Slot Buffer 1 Time Stamp Low-Order	C0SLOT1_15	XX₁₆
0200₁₆ 0201₁₆	CAN0 Control Register 0	C0CTLR0	XX01 0X01₂(1) XXXX 0000₂(1)
0202₁₆ 0203₁₆	CAN0 Status Register	C0STR	0000 0000₂(1) X000 0X01₂(1)
0204₁₆ 0205₁₆	CAN0 Extended ID Register	C0IDR	00₁₆(1) 00₁₆(1)
0206₁₆ 0207₁₆	CAN0 Configuration Register	C0CONR	0000 XXXX₂(1) 0000 0000₂(1)
0208₁₆ 0209₁₆	CAN0 Time Stamp Register	C0TSR	00₁₆(1) 00₁₆(1)
020A₁₆	CAN0 Transmit Error Count Register	C0TEC	00₁₆(1)
020B₁₆	CAN0 Receive Error Count Register	C0REC	00₁₆(1)
020C₁₆ 020D₁₆	CAN0 Slot Interrupt Status Register	C0SISTR	00₁₆(1) 00₁₆(1)
020E₁₆			
020F₁₆			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTES:

1. Values are obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) after reset and applying the clock to the CAN module.

Address	Register	Symbol	Value after RESET
0210$_{16}$ 0211$_{16}$	CAN0 Slot Interrupt Mask Register	C0SIMKR	00$_{16}$(2) 00$_{16}$(2)
0212$_{16}$			
0213$_{16}$			
0214$_{16}$	CAN0 Error Interrupt Mask Register	C0EIMKR	XXXX X000$_2$(2)
0215$_{16}$	CAN0 Error Interrupt Status Register	C0EISTR	XXXX X000$_2$(2)
0216$_{16}$	CAN0 Error Cause Register	C0EFR	00$_{16}$(2)
0217$_{16}$	CAN0 Baud Rate Prescaler	C0BRP	0000 0001$_2$(2)
0218$_{16}$			
0219$_{16}$	CAN0 Mode Register	C0MDR	XXXX XX00$_2$(2)
021A$_{16}$			
021B$_{16}$			
021C$_{16}$			
021D$_{16}$			
021E$_{16}$			
021F$_{16}$			
0220$_{16}$ 0221$_{16}$	CAN0 Single Shot Control Register	C0SSCTLR	00$_{16}$(2) 00$_{16}$(2)
0222$_{16}$			
0223$_{16}$			
0224$_{16}$ 0225$_{16}$	CAN0 Single Shot Status Register	C0SSSTR	00$_{16}$(2) 00$_{16}$(2)
0226$_{16}$			
0227$_{16}$			
0228$_{16}$	CAN0 Global Mask Register Standard ID0	C0GMR0	XXX0 0000$_2$(2)
0229$_{16}$	CAN0 Global Mask Register Standard ID1	C0GMR1	XX00 0000$_2$(2)
022A$_{16}$	CAN0 Global Mask Register Extended ID0	C0GMR2	XXXX 0000$_2$(2)
022B$_{16}$	CAN0 Global Mask Register Extended ID1	C0GMR3	00$_{16}$(2)
022C$_{16}$	CAN0 Global Mask Register Extended ID2	C0GMR4	XX00 0000$_2$(2)
022D$_{16}$			
022E$_{16}$			
022F$_{16}$			
0230$_{16}$	CAN0 Message Slot 0 Control Register / CAN0 Local Mask Register A Standard ID0	C0MCTL0/ C0LMAR0	0000 0000$_2$(2) XXX0 0000$_2$(2)
0231$_{16}$	CAN0 Message Slot 1 Control Register / CAN0 Local Mask Register A Standard ID1	C0MCTL1/ C0LMAR1	0000 0000$_2$(2) XX00 0000$_2$(2)
0232$_{16}$	CAN0 Message Slot 2 Control Register / CAN0 Local Mask Register A Extended ID0	C0MCTL2/ C0LMAR2	0000 0000$_2$(2) XXXX 0000$_2$(2)
0233$_{16}$	CAN0 Message Slot 3 Control Register / CAN0 local Mask Register A Extended ID1	C0MCTL3/ C0LMAR3	00$_{16}$(2) 00$_{16}$(2)
0234$_{16}$	CAN0 Message Slot 4 Control Register / CAN0 Local Mask Register A Extended ID2	C0MCTL4/ C0LMAR4	0000 0000$_2$(2) XX00 0000$_2$(2)
0235$_{16}$	CAN0 Message Slot 5 Control Register	C0MCTL5	00$_{16}$(2)
0236$_{16}$	CAN0 Message Slot 6 Control Register	C0MCTL6	00$_{16}$(2)
0237$_{16}$	CAN0 Message Slot 7 Control Register	C0MCTL7	00$_{16}$(2)
0238$_{16}$	CAN0 Message Slot 8 Control Register / CAN0 Local Mask Register B Standard ID0	C0MCTL8/ C0LMBR0	0000 0000$_2$(2) XXX0 0000$_2$(2)
0239$_{16}$	CAN0 Message Slot 9 Control Register / CAN0 Local Mask Register B Standard ID1	C0MCTL9/ C0LMBR1	0000 0000$_2$(2) XX00 0000$_2$(2)

(Note 1)

X: Indeterminate

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NOTES:

1. The BANKSEL bit in the C0CTLR1 register switches functions for addresses 0220$_{16}$ to 023F$_{16}$.
2. Values are obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) after reset and applying the clock to the CAN module.

Address	Register	Symbol	Value after RESET
02E0₁₆	X/Y Control Register	XYC	XXXX XX00₂
02E1₁₆			
02E2₁₆			
02E3₁₆			
02E4₁₆	UART1 Special Mode Register 4	U1SMR4	00₁₆
02E5₁₆	UART1 Special Mode Register 3	U1SMR3	00₁₆
02E6₁₆	UART1 Special Mode Register 2	U1SMR2	00₁₆
02E7₁₆	UART1 Special Mode Register	U1SMR	00₁₆
02E8₁₆	UART1 Transmit/Receive Mode Register	U1MR	00₁₆
02E9₁₆	UART1 Bit Rate Register	U1BRG	XX₁₆
02EA₁₆	UART1 Transmit Buffer Register	U1TB	XX₁₆
02EB₁₆			XX₁₆
02EC₁₆	UART1 Transmit/Receive Control Register 0	U1C0	0000 1000₂
02ED₁₆	UART1 Transmit/Receive Control Register 1	U1C1	0000 0010₂
02EE₁₆	UART1 Receive Buffer Register	U1RB	XX₁₆
02EF₁₆			XX₁₆
02F0₁₆			
02F1₁₆			
02F2₁₆			
02F3₁₆			
02F4₁₆	UART4 Special Mode Register 4	U4SMR4	00₁₆
02F5₁₆	UART4 Special Mode Register 3	U4SMR3	00₁₆
02F6₁₆	UART4 Special Mode Register 2	U4SMR2	00₁₆
02F7₁₆	UART4 Special Mode Register	U4SMR	00₁₆
02F8₁₆	UART4 Transmit/Receive Mode Register	U4MR	00₁₆
02F9₁₆	UART4 Bit Rate Register	U4BRG	XX₁₆
02FA₁₆	UART4 Transmit Buffer Register	U4TB	XX₁₆
02FB₁₆			XX₁₆
02FC₁₆	UART4 Transmit/Receive Control Register 0	U4C0	0000 1000₂
02FD₁₆	UART4 Transmit/Receive Control Register 1	U4C1	0000 0010₂
02FE₁₆	UART4 Receive Buffer Register	U4RB	XX₁₆
02FF₁₆			XX₁₆
0300₁₆	Timer B3, B4, B5 Count Start Flag	TBSR	000X XXXX₂
0301₁₆			
0302₁₆	Timer A1-1 Register	TA11	XX₁₆
0303₁₆			XX₁₆
0304₁₆	Timer A2-1 Register	TA21	XX₁₆
0305₁₆			XX₁₆
0306₁₆	Timer A4-1 Register	TA41	XX₁₆
0307₁₆			XX₁₆
0308₁₆	Three-Phase PWM Control Register 0	INVC0	00₁₆
0309₁₆	Three-Phase PWM Control Register 1	INVC1	00₁₆
030A₁₆	Three-Phase Output Buffer Register 0	IDB0	XX11 1111₂
030B₁₆	Three-Phase Output Buffer Register 1	IDB1	XX11 1111₂
030C₁₆	Dead Time Timer	DTT	XX₁₆
030D₁₆	Timer B2 Interrupt Generation Frequency Set Counter	ICTB2	XX₁₆
030E₁₆			
030F₁₆			

X: Indeterminate

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Address	Register	Symbol	Value after RESET
0310$_{16}$	Timer B3 Register	TB3	XX$_{16}$
0311$_{16}$			XX$_{16}$
0312$_{16}$	Timer B4 Register	TB4	XX$_{16}$
0313$_{16}$			XX$_{16}$
0314$_{16}$	Timer B5 Register	TB5	XX$_{16}$
0315$_{16}$			XX$_{16}$
0316$_{16}$			
0317$_{16}$			
0318$_{16}$			
0319$_{16}$			
031A$_{16}$			
031B$_{16}$	Timer B3 Mode Register	TB3MR	00XX 0000$_2$
031C$_{16}$	Timer B4 Mode Register	TB4MR	00XX 0000$_2$
031D$_{16}$	Timer B5 Mode Register	TB5MR	00XX 0000$_2$
031E$_{16}$			
031F$_{16}$	External Interrupt Request Source Select Register	IFSR	00$_{16}$
0320$_{16}$			
0321$_{16}$			
0322$_{16}$			
0323$_{16}$			
0324$_{16}$	UART3 Special Mode Register 4	U3SMR4	00$_{16}$
0325$_{16}$	UART3 Special Mode Register 3	U3SMR3	00$_{16}$
0326$_{16}$	UART3 Special Mode Register 2	U3SMR2	00$_{16}$
0327$_{16}$	UART3 Special Mode Register	U3SMR	00$_{16}$
0328$_{16}$	UART3 Transmit/Receive Mode Register	U3MR	00$_{16}$
0329$_{16}$	UART3 Bit Rate Register	U3BRG	XX$_{16}$
032A$_{16}$	UART3 Transmit Buffer Register	U3TB	XX$_{16}$
032B$_{16}$			XX$_{16}$
032C$_{16}$	UART3 Transmit/Receive Control Register 0	U3C0	0000 1000$_2$
032D$_{16}$	UART3 Transmit/Receive Control Register 1	U3C1	0000 0010$_2$
032E$_{16}$	UART3 Receive Buffer Register	U3RB	XX$_{16}$
032F$_{16}$			XX$_{16}$
0330$_{16}$			
0331$_{16}$			
0332$_{16}$			
0333$_{16}$			
0334$_{16}$	UART2 Special Mode Register 4	U2SMR4	00$_{16}$
0335$_{16}$	UART2 Special Mode Register 3	U2SMR3	00$_{16}$
0336$_{16}$	UART2 Special Mode Register 2	U2SMR2	00$_{16}$
0337$_{16}$	UART2 Special Mode Register	U2SMR	00$_{16}$
0338$_{16}$	UART2 Transmit/Receive Mode Register	U2MR	00$_{16}$
0339$_{16}$	UART2 Bit Rate Register	U2BRG	XX$_{16}$
033A$_{16}$	UART2 Transmit Buffer Register	U2TB	XX$_{16}$
033B$_{16}$			XX$_{16}$
033C$_{16}$	UART2 Transmit/Receive Control Register 0	U2C0	0000 1000$_2$
033D$_{16}$	UART2 Transmit/Receive Control Register 1	U2C1	0000 0010$_2$
033E$_{16}$	UART2 Receive Buffer Register	U2RB	XX$_{16}$
033F$_{16}$			XX$_{16}$

X: Indeterminate

Blank spaces are reserved. No access is allowed.

<144-pin package>

Address	Register	Symbol	Value after RESET
03D0$_{16}$	Port P14 Register	P14	XX$_{16}$
03D1$_{16}$	Port P15 Register	P15	XX$_{16}$
03D2$_{16}$	Port P14 Direction Register	PD14	X000 0000$_2$
03D3$_{16}$	Port P15 Direction Register	PD15	00$_{16}$
03D4$_{16}$			
03D5$_{16}$			
03D6$_{16}$			
03D7$_{16}$			
03D8$_{16}$			
03D9$_{16}$			
03DA$_{16}$	Pull-Up Control Register 2	PUR2	00$_{16}$
03DB$_{16}$	Pull-Up Control Register 3	PUR3	00$_{16}$
03DC$_{16}$	Pull-Up Control Register 4	PUR4	XXXX 0000$_2$
03DD$_{16}$			
03DE$_{16}$			
03DF$_{16}$			
03E0$_{16}$	Port P0 Register	P0	XX$_{16}$
03E1$_{16}$	Port P1 Register	P1	XX$_{16}$
03E2$_{16}$	Port P0 Direction Register	PD0	00$_{16}$
03E3$_{16}$	Port P1 Direction Register	PD1	00$_{16}$
03E4$_{16}$	Port P2 Register	P2	XX$_{16}$
03E5$_{16}$	Port P3 Register	P3	XX$_{16}$
03E6$_{16}$	Port P2 Direction Register	PD2	00$_{16}$
03E7$_{16}$	Port P3 Direction Register	PD3	00$_{16}$
03E8$_{16}$	Port P4 Register	P4	XX$_{16}$
03E9$_{16}$	Port P5 Register	P5	XX$_{16}$
03EA$_{16}$	Port P4 Direction Register	PD4	00$_{16}$
03EB$_{16}$	Port P5 Direction Register	PD5	00$_{16}$
03EC$_{16}$			
03ED$_{16}$			
03EE$_{16}$			
03EF$_{16}$			
03F0$_{16}$	Pull-Up Control Register 0	PUR0	00$_{16}$
03F1$_{16}$	Pull-Up Control Register 1	PUR1	XXXX 0000$_2$
03F2$_{16}$			
03F3$_{16}$			
03F4$_{16}$			
03F5$_{16}$			
03F6$_{16}$			
03F7$_{16}$			
03F8$_{16}$			
03F9$_{16}$			
03FA$_{16}$			
03FB$_{16}$			
03FC$_{16}$			
03FD$_{16}$			
03FE$_{16}$			
03FF$_{16}$	Port Control Register	PCR	XXXX XXX0$_2$

X: Indeterminate

Blank spaces are reserved. No access is allowed.

<100-pin package>

Address	Register	Symbol	Value after RESET
03A0$_{16}$			
03A1$_{16}$			
03A2$_{16}$			
03A3$_{16}$			
03A4$_{16}$			
03A5$_{16}$			
03A6$_{16}$			
03A7$_{16}$	Function Select Register D1	PSD1	X0XX XX00$_2$
03A8$_{16}$			
03A9$_{16}$			
03AA$_{16}$			
03AB$_{16}$			
03AC$_{16}$	Function Select Register C2	PSC2	XXXX X00X$_2$
03AD$_{16}$	Function Select Register C3	PSC3	X0XX XXXX$_2$
03AE$_{16}$			
03AF$_{16}$	Function Select Register C	PSC	00X0 0000$_2$
03B0$_{16}$	Function Select Register A0	PS0	00$_{16}$
03B1$_{16}$	Function Select Register A1	PS1	00$_{16}$
03B2$_{16}$	Function Select Register B0	PSL0	00$_{16}$
03B3$_{16}$	Function Select Register B1	PSL1	00$_{16}$
03B4$_{16}$	Function Select Register A2	PS2	00X0 0000$_2$
03B5$_{16}$	Function Select Register A3	PS3	00$_{16}$
03B6$_{16}$	Function Select Register B2	PSL2	00X0 0000$_2$
03B7$_{16}$	Function Select Register B3	PSL3	00$_{16}$
03B8$_{16}$			
03B9$_{16}$			
03BA$_{16}$			
03BB$_{16}$			
03BC$_{16}$			
03BD$_{16}$			
03BE$_{16}$			
03BF$_{16}$			
03C0$_{16}$	Port P6 Register	P6	XX$_{16}$
03C1$_{16}$	Port P7 Register	P7	XX$_{16}$
03C2$_{16}$	Port P6 Direction Register	PD6	00$_{16}$
03C3$_{16}$	Port P7 Direction Register	PD7	00$_{16}$
03C4$_{16}$	Port P8 Register	P8	XX$_{16}$
03C5$_{16}$	Port P9 Register	P9	XX$_{16}$
03C6$_{16}$	Port P8 Direction Register	PD8	00X0 0000$_2$
03C7$_{16}$	Port P9 Direction Register	PD9	00$_{16}$
03C8$_{16}$	Port P10 Register	P10	XX$_{16}$
03C9$_{16}$			
03CA$_{16}$	Port P10 Direction Register	PD10	00$_{16}$
03CB$_{16}$	Set default value to "FF$_{16}$"		
03CC$_{16}$			
03CD$_{16}$			
03CE$_{16}$	Set default value to "FF$_{16}$"		
03CF$_{16}$	Set default value to "FF$_{16}$"		

X: Indeterminate

Blank spaces are reserved. No access is allowed.

5. Electrical Characteristics

5.1 Electrical Characteristics (M32C/85)

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter		Condition	Value	Unit
V_{CC1}, V_{CC2}	Supply Voltage		V_{CC1}=AV$_{CC}$	-0.3 to 6.0	V
V_{CC2}	Supply Voltage		-	-0.3 to V_{CC1}	V
AV$_{CC}$	Analog Supply Voltage		V_{CC1}=AV$_{CC}$	-0.3 to 6.0	V
V_I	Input Voltage	$\overline{RESET}$, CNV$_{SS}$, BYTE, P6$_0$-P6$_7$, P7$_2$-P7$_7$, P8$_0$-P8$_7$, P9$_0$-P9$_7$, P10$_0$-P10$_7$, P14$_0$-P14$_6$, P15$_0$-P15$_7$(1), V_{REF}, X_{IN}		-0.3 to V_{CC1}+0.3	V
		P0$_0$-P0$_7$, P1$_0$-P1$_7$, P2$_0$-P2$_7$, P3$_0$-P3$_7$, P4$_0$-P4$_7$, P5$_0$-P5$_7$, P11$_0$-P11$_4$, P12$_0$-P12$_7$, P13$_0$-P13$_7$(1)		-0.3 to V_{CC2}+0.3	
		P7$_0$, P7$_1$		-0.3 to 6.0	
V_O	Output Voltage	P6$_0$-P6$_7$, P7$_2$-P7$_7$, P8$_0$-P8$_4$, P8$_6$, P8$_7$, P9$_0$-P9$_7$, P10$_0$-P10$_7$, P14$_0$-P14$_6$, P15$_0$-P15$_7$(1), X_{OUT}		-0.3 to V_{CC1}+0.3	V
		P0$_0$-P0$_7$, P1$_0$-P1$_7$, P2$_0$-P2$_7$, P3$_0$-P3$_7$, P4$_0$-P4$_7$, P5$_0$-P5$_7$, P11$_0$-P11$_4$, P12$_0$-P12$_7$, P13$_0$-P13$_7$(1)		-0.3 to V_{CC2}+0.3	
		P7$_0$, P7$_1$		-0.3 to 6.0	
Pd	Power Dissipation		Topr=25° C	500	mW
Topr	Operating Ambient Temperature	during CPU operation		-20 to 85/ -40 to 85(2)	° C
		during flash memory program and erase operation		0 to 60	
Tstg	Storage Temperature			-65 to 150	° C

NOTES:
1. P11 to P15 are provided in the 144-pin package only.
2. Contact Renesas Technology Sales Co., Ltd, if temperature range of -40 to 85° C is required.

$V_{CC1}=V_{CC2}=5V$

Table 5.4 A/D Conversion Characteristics ($V_{CC1}=V_{CC2}=AV_{CC}=V_{REF}$=4.2 to 5.5V, V_{SS}= AV_{SS} = 0V at Topr=–20 to 85°C, f(BCLK) = 32MHz unless otherwise specified)

Symbol	Parameter	Measurement Condition		Standard			Unit
				Min.	Typ.	Max.	
-	Resolution	$V_{REF}=V_{CC1}$				10	Bits
INL	Integral Nonlinearity Error	$V_{REF}=V_{CC1}=V_{CC2}$=5V	AN_0 to AN_7, $AN0_0$ to $AN0_7$, $AN2_0$ to $AN2_7$, $AN15_0$ to $AN15_7$, ANEX0, ANEX1			±3	LSB
							LSB
			External op-amp connection mode			±7	LSB
							LSB
DNL	Differential Nonlinearity Error					±1	LSB
-	Offset Error					±3	LSB
-	Gain Error					±3	LSB
R_{LADDER}	Resistor Ladder	$V_{REF}=V_{CC1}$		8		40	kΩ
t_{CONV}	10-bit Conversion Time(1, 2)			2.06			µs
t_{CONV}	8-bit Conversion Time(1, 2)			1.75			µs
t_{SAMP}	Sampling Time(1)			0.188			µs
V_{REF}	Reference Voltage			2		V_{CC1}	V
V_{IA}	Analog Input Voltage			0		V_{REF}	V

NOTES:
1. Divide f(X_{IN}), if exceeding 16 MHz, to keep ϕAD frequency at 16 MHz or less.
2. With using the sample and hold function.

Table 5.5 D/A Conversion Characteristics ($V_{CC1}=V_{CC2}=V_{REF}$=4.2 to 5.5V, $V_{SS}=AV_{SS}$=0V at Topr=–20 to 85°C, f(BCLK) = 32MHz unless otherwise specified)

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min.	Typ.	Max.	
-	Resolution				8	Bits
-	Absolute Accuracy				1.0	%
t_{SU}	Setup Time				3	µs
R_O	Output Resistance		4	10	20	kΩ
I_{VREF}	Reference Power Supply Input Current	(Note 1)			1.5	mA

NOTES:
1. Measurement when using one D/A converter. The DAi register (i=0, 1) of the D/A converter, not being used, is set to "00_{16}". The resistor ladder in the A/D converter is excluded.
I_{VREF} flows even if the VCUT bit in the AD0CON1 register is set to "0" (no V_{REF} connection).

$V_{CC1}=V_{CC2}=5V$

Timing Requirements

($V_{CC1}=V_{CC2}=4.2$ to 5.5V, $V_{SS}=0V$ at Topr=–20 to 85°C unless otherwise specified)

Table 5.9 External Clock Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc	External Clock Input Cycle Time	31.25		ns
$t_{W(H)}$	External Clock Input High ("H") Width	13.75		ns
$t_{W(L)}$	External Clock Input Low ("L") Width	13.75		ns
tr	External Clock Rise Time		5	ns
tf	External Clock Fall Time		5	ns

Table 5.10 Memory Expansion Mode and Microprocessor Mode

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{ac1(RD-DB)}$	Data Input Access Time (RD standard)		(Note 1)	ns
$t_{ac1(AD-DB)}$	Data Input Access Time (AD standard, CS standard)		(Note 1)	ns
$t_{ac2(RD-DB)}$	Data Input Access Time (RD standard, when accessing a space with the multiplexed bus)		(Note 1)	ns
$t_{ac2(AD-DB)}$	Data Input Access Time (AD standard, when accessing a space with the multiplexed bus)		(Note 1)	ns
$t_{su(DB-BCLK)}$	Data Input Setup Time	26		ns
$t_{su(RDY-BCLK)}$	$\overline{RDY}$ Input Setup Time	26		ns
$t_{su(HOLD-BCLK)}$	$\overline{HOLD}$ Input Setup Time	30		ns
$t_{h(RD-DB)}$	Data Input Hold Time	0		ns
$t_{h(BCLK-RDY)}$	$\overline{RDY}$ Input Hold Time	0		ns
$t_{h(BCLK-HOLD)}$	$\overline{HOLD}$ Input Hold Time	0		ns
$t_{d(BCLK-HLDA)}$	$\overline{HLDA}$ Output Delay Time		25	ns

NOTES:
1. Values can be obtained from the following equations, according to BCLK frequecncy and external bus cycles. Insert a wait state or lower the operation frequency, $f_{(BCLK)}$, if the calculated value is negative.

$$t_{ac1(RD-DB)} = \frac{10^9 \times m}{f_{(BCLK)} \times 2} - 35$$ [ns] (if external bus cycle is aϕ + bϕ, m=(bx2)+1)

$$t_{ac1(AD-DB)} = \frac{10^9 \times n}{f_{(BCLK)}} - 35$$ [ns] (if external bus cycle is aϕ + bϕ, n=a+b)

$$t_{ac2(RD-DB)} = \frac{10^9 \times m}{f_{(BCLK)} \times 2} - 35$$ [ns] (if external bus cycle is aϕ + bϕ, m=(bx2)-1)

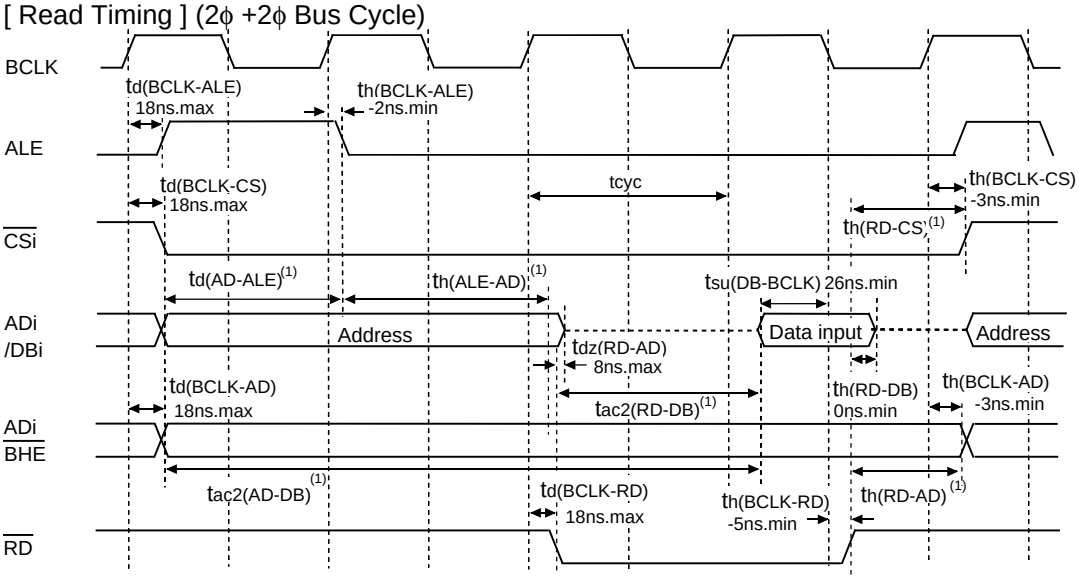
$$t_{ac2(AD-DB)} = \frac{10^9 \times p}{f_{(BCLK)} \times 2} - 35$$ [ns] (if external bus cycle is aϕ + bϕ, p={(a+b-1)x2}+1)

$V_{CC1}=V_{CC2}=5V$

Memory Expansion Mode and Microprocessor Mode

(when accessing an external memory space with the multiplexed bus)

[Read Timing] (2φ +2φ Bus Cycle)



NOTES:

1. Varies with operation frequency:

$t_{d(AD-ALE)}$=(tcyc/2 x n-20)ns.min (if external bus cycle is aφ + bφ, n=a)

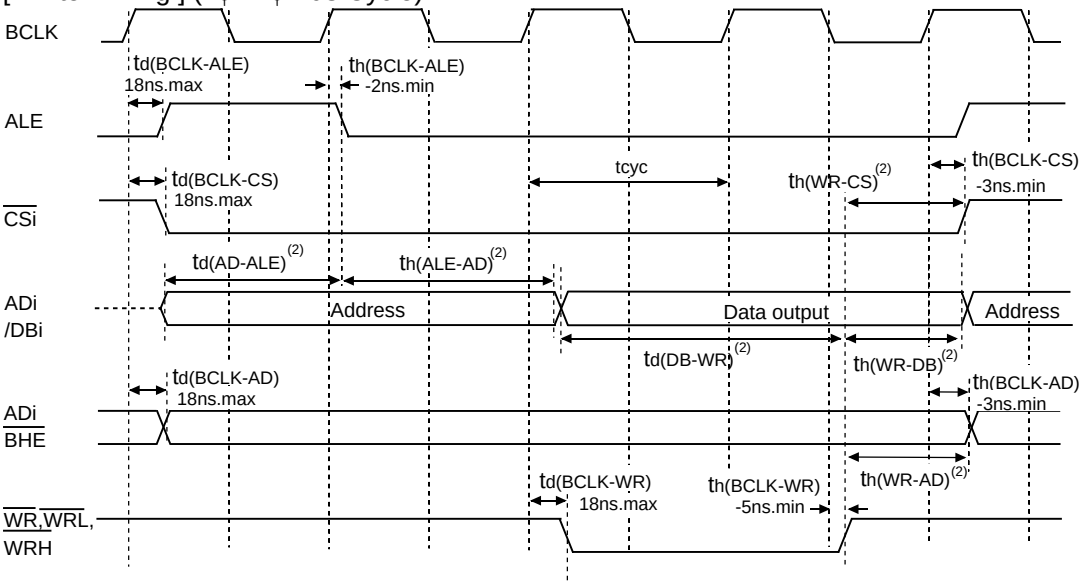
$t_{h(ALE-AD)}$=(tcyc/2 x n-10)ns.min (if external bus cycle is aφ + bφ, n=a)

$t_{h(RD-AD)}$=(tcyc/2-10)ns.min, $t_{h(RD-CS)}$=(tcyc/2-10)ns.min

$t_{ac2(RD-DB)}$=(tcyc/2 x m-35)ns.max (if external bus cycle is aφ + bφ, m=(b x 2)-1)

$t_{ac2(AD-DB)}$=(tcyc/2 x p-35)ns.max (if external bus cycle is aφ + bφ, p={(a+b-1) x 2}+1)

[Write Timing] (2φ +2φ Bus Cycle)



NOTES:

2. Varies with operation frequency:

$t_{d(AD-ALE)}$=(tcyc/2 x n - 20)ns.min

(if external bus cycle is aφ + bφ, n=a)

$t_{h(ALE-AD)}$=(tcyc/2 x n -10)ns.min

(if external bus cycle is aφ + bφ, n=a)

$t_{h(WR-AD)}$=(tcyc/2-10)ns.min,

$t_{h(WR-CS)}$=(tcyc/2-10)ns.min, $t_{h(WR-DB)}$=(tcyc/2-10)ns.min

$t_{d(DB-WR)}$=(tcyc/2 x m-25)ns.min

(if external bus cycle is aφ + bφ, m=(b x 2)-1)

Measurement Conditions:

- $V_{CC1}=V_{CC2}$=4.2 to 5.5V
- Input high and low voltage: V_{IH}=2.5V, V_{IL}=0.8V
- Output high and low voltage: V_{OH}=2.0V, V_{OL}=0.8V

$$tcyc=\frac{10^9}{f_{(BCLK)}}$$

Figure 5.4 $V_{CC1}=V_{CC2}$=5V Timing Diagram (2)

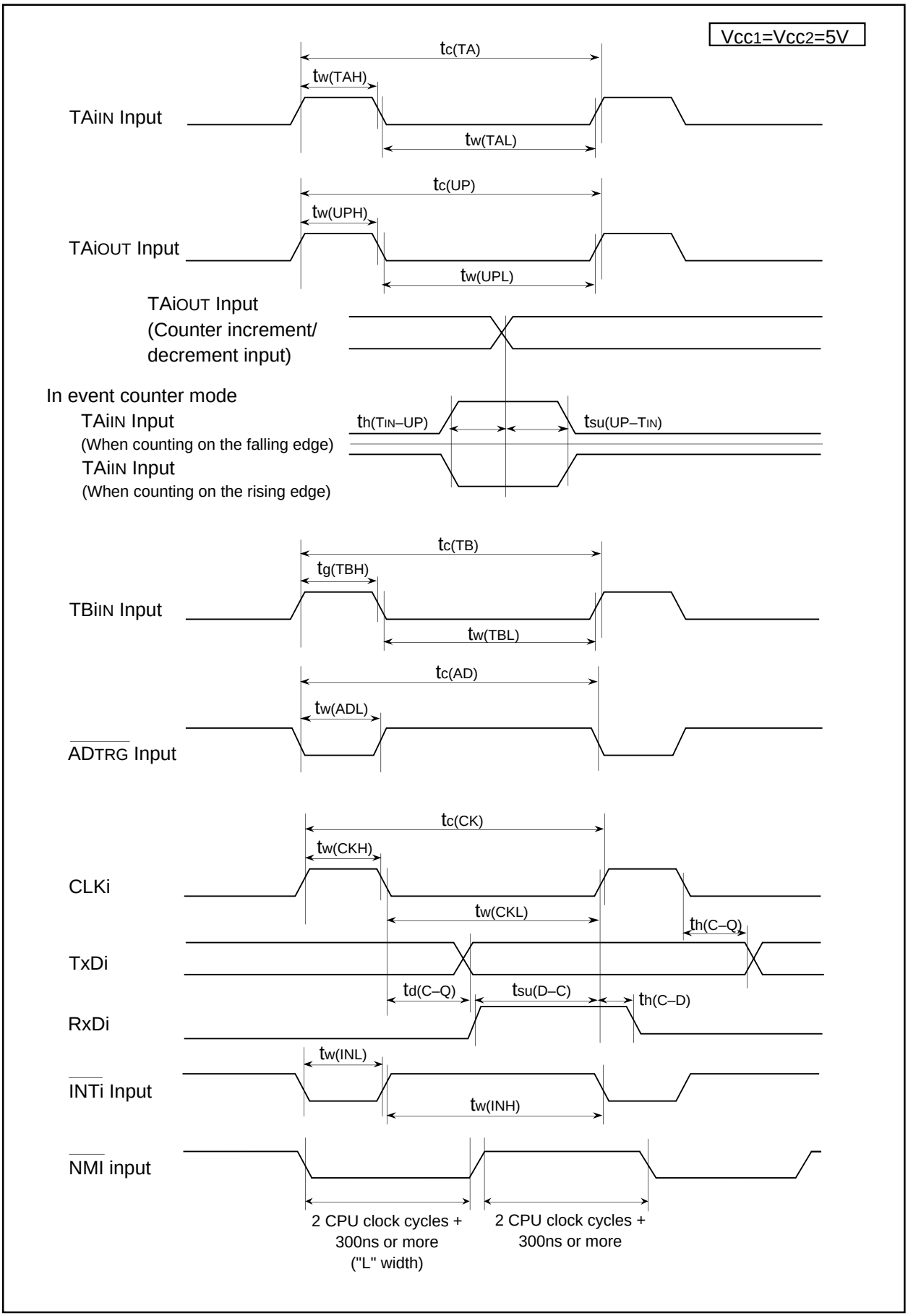


Figure 5.5 Vcc1=Vcc2=5V Timing Diagram (3)

$V_{CC1}=V_{CC2}=3.3V$

Table 5.25 A/D Conversion Characteristics ($V_{CC1}=V_{CC2}=AV_{CC}=V_{REF}$= 3.0 to 3.6V, $V_{SS}=AV_{SS}$=0V at Topr = –20 to 85°C, f(BCLK) = 24MHz unless otherwise specified)

Symbol	Parameter		Measurement Condition	Standard			Unit
				Min.	Typ.	Max.	
-	Resolution		$V_{REF}=V_{CC1}$			10	Bits
INL	Integral Nonlinearity Error	No S&H (8-bit)	$V_{CC1}=V_{CC2}=V_{REF}$=3.3V			±2	LSB
DNL	Differential Nonlinearity Error	No S&H (8-bit)				±1	LSB
-	Offset Error	No S&H (8-bit)				±2	LSB
-	Gain Error	No S&H (8-bit)				±2	LSB
R_{LADDER}	Resistor Ladder		$V_{REF}=V_{CC1}$	8		40	kΩ
t_{CONV}	8-bit Conversion Time(1, 2)			6.1			µs
V_{REF}	Reference Voltage			3		V_{CC1}	V
V_{IA}	Analog Input Voltage			0		V_{REF}	V

S&H: Sample and Hold

NOTES:
1. Divide f(X_{IN}), if exceeding 10 MHz, to keep ϕAD frequency at 10 MHz or less.
2. S&H not available.

Table 5.26 D/A Conversion Characteristics ($V_{CC1}=V_{CC2}=V_{REF}$=3.0 to 3.6V, $V_{SS}=AV_{SS}$=0V at Topr = –20 to 85°C, f(BCLK) = 24MHz unless otherwise specified)

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min.	Typ.	Max.	
-	Resolution				8	Bits
-	Absolute Accuracy				1.0	%
t_{SU}	Setup Time				3	µs
R_O	Output Resistance		4	10	20	kΩ
I_{VREF}	Reference Power Supply Input Current	(Note 1)			1.0	mA

NOTES:
1. Measurement results when using one D/A converter. The DAi register (i=0, 1) of the D/A converter, not being used, is set to "00_{16}". The resistor ladder in the A/D converter is excluded.
I_{VREF} flows even if the VCUT bit in the AD0CON1 register is set to "0" (no V_{REF} connection).

$V_{CC1}=V_{CC2}=3.3V$

Switching Characteristics

($V_{CC1}=V_{CC2}$=3.0 to 3.6V, VSS = 0V at Topr = –20 to 85°C unless otherwise specified)

Table 5.40 Memory Expansion Mode and Microprocessor Mode (when accessing external memory space)

Symbol	Parameter	Measurement Condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address Output Delay Time	See Figure 5.2		18	ns
$t_{h(BCLK-AD)}$	Address Output Hold Time (BCLK standard)		0		ns
$t_{h(RD-AD)}$	Address Output Hold Time (RD standard)(3)		0		ns
$t_{h(WR-AD)}$	Address Output Hold Time (WR standard)(3)		(Note 1)		ns
$t_{d(BCLK-CS)}$	Chip-Select Signal Output Delay Time			18	ns
$t_{h(BCLK-CS)}$	Chip-Select Signal Output Hold Time (BCLK standard)		0		ns
$t_{h(RD-CS)}$	Chip-Select Signal Output Hold Time (RD standard)(3)		0		ns
$t_{h(WR-CS)}$	Chip-Select Signal Output Hold Time (WR standard)(3)		(Note 1)		ns
$t_{d(BCLK-RD)}$	RD Signal Output Delay Time			18	ns
$t_{h(BCLK-RD)}$	RD Signal Output Hold Time		-3		ns
$t_{d(BCLK-WR)}$	WR Signal Output Delay Time			18	ns
$t_{h(BCLK-WR)}$	WR Signal Output Hold Time		0		ns
$t_{d(DB-WR)}$	Data Output Delay Time (WR standard)		(Note 2)		ns
$t_{h(WR-DB)}$	Data Output Hold Time (WR standard)(3)		(Note 1)		ns
$t_{w(WR)}$	WR Output Width		(Note 2)		ns

NOTES:

1. Values can be obtained from the following equations, according to BCLK frequency.

$$t_{h(WR-DB)} = \frac{10^9}{f_{(BCLK)} \times 2} - 20 \quad [ns]$$

$$t_{h(WR-AD)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$t_{h(WR-CS)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

2. Values can be obtained from the following equations, according to BCLK frequency and external bus cycles.

$$t_{w(WR)} = \frac{10^9 \times n}{f_{(BCLK)} \times 2} - 15 \quad [ns] \quad \text{(if external bus cycle is } a\phi + b\phi\text{, } n=(b \times 2)-1)$$

$$t_{d(DB-WR)} = \frac{10^9 \times m}{f_{(BCLK)}} - 20 \quad [ns] \quad \text{(if external bus cycle is } a\phi + b\phi\text{, } m=b)$$

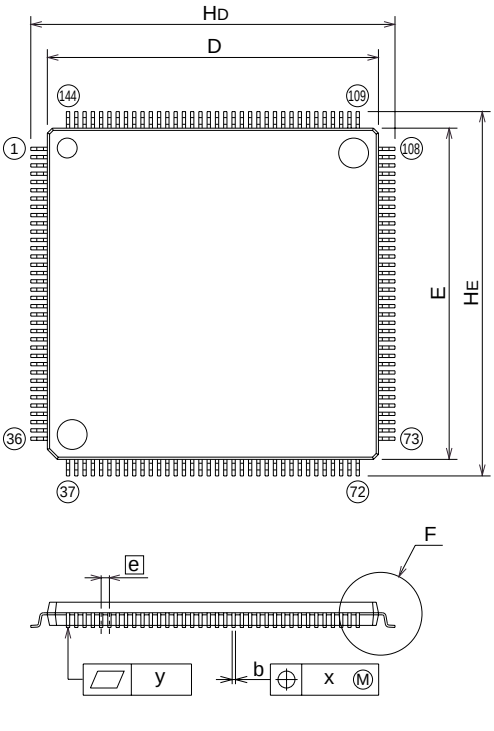
3. *tc* ns is added when recovery cycle is inserted.

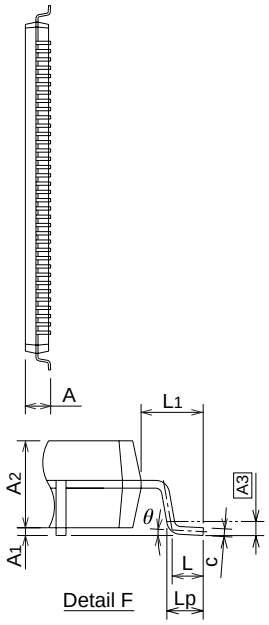
Package Dimensions

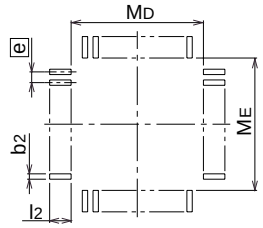
PLQP0144KA-A (144P6Q-A)

Plastic 144pin 20×20mm body LQFP

JEITA Package Code	RENESAS Code	Previous Code	Mass[Typ.]
P-LQFP144-20x20-0.50	PLQP0144KA-A	144P6Q-A	1.2g







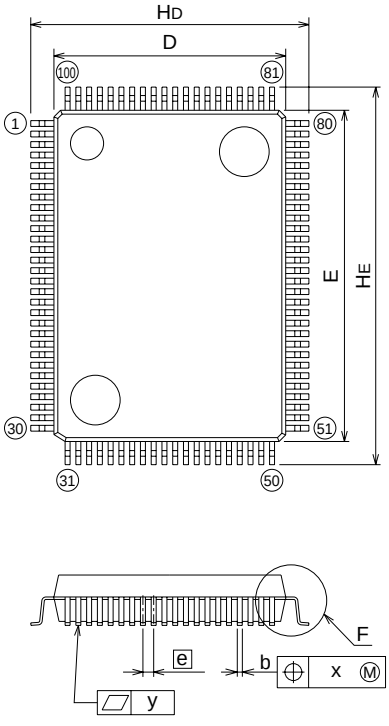
Recommended Mount Pad

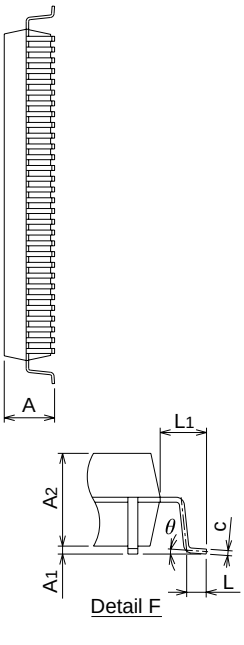
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	1.7
A1	0.05	0.125	0.2
A2	–	1.4	–
b	0.17	0.22	0.27
c	0.105	0.125	0.175
D	19.9	20.0	20.1
E	19.9	20.0	20.1
e	–	0.5	–
HD	21.8	22.0	22.2
HE	21.8	22.0	22.2
L	0.35	0.5	0.65
L1	–	1.0	–
Lp	0.45	0.6	0.75
A3	–	0.25	–
x	–	–	0.08
y	–	–	0.1
θ	0°	–	8°
b2	–	0.225	–
l2	0.95	–	–
MD	–	20.4	–
ME	–	20.4	–

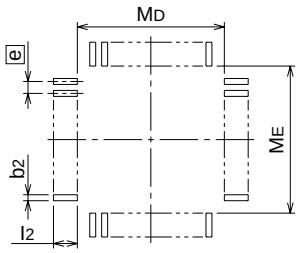
PRQP0100JB-A (100P6S-A)

Plastic 100pin 14×20mm body QFP

JEITA Package Code	RENESAS Code	Previous Code	Mass[Typ.]
P-QFP100-14x20-0.65	PRQP0100JB-A	100P6S-A	1.6g







Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	3.05
A1	0	0.1	0.2
A2	–	2.8	–
b	0.25	0.3	0.4
c	0.13	0.15	0.2
D	13.8	14.0	14.2
E	19.8	20.0	20.2
e	–	0.65	–
HD	16.5	16.8	17.1
HE	22.5	22.8	23.1
L	0.4	0.6	0.8
L1	–	1.4	–
x	–	–	0.13
y	–	–	0.1
θ	0°	–	10°
b2	–	0.35	–
l2	1.3	–	–
MD	–	14.6	–
ME	–	20.6	–

Rev.	Date	Description	
		Page	Summary
		65	• **Table 5.28 Memory Expansion Mode and Microprocessor Mode** tac1(AD-DB) expression modified
		77	• **Table 5.44 Electrical Characteristics** ICC standard value revised
		80	• **Table 5.47 Flash Memory Electrical Characteristics** Topr value modified
1.21	Jul.01, 2005	All pages	Package code changed: 144P6Q-A to PLQP0144KA-A, 100P6Q-A to PLQP0100KB-A, 100P6S-A to PRQP0100JB-A
		All pages	**"**Low Voltage Detection Reset**"** changed to **"**Brown-out Detection Reset**"**
			Special Function Register (SFR)
		27	• The G0RB register Value after reset modified
		39	• The TCSPR register Value after reset modified
			Electrical Characteristics
		47	• **Table 5.2 Electrical Characteristics** Parameter f(BCLK) and its values added
		51	• **Table 5.6 Flash Memory Version Electrical Characteristics** Mesurement condition changed
		53	• **Table 5.10 Memory Expansion Mode and Microprocessor Mode** *tac1(RD-DB)* expression on Note 1 modified; *tac2(RD-DB)* expression on Note 1 added
		59	• **Figure 5.3 Vcc1=Vcc2=5V Timing Diagram (1)** *tW(ER)* expression on Note 3 modified; *tcyc* expression added
		60	• **Figure 5.4 Vcc1=Vcc2=5V Timing Diagram (2)** *tac2(AD-DB)* expression on Note 1 modified; *th(ALE-AD)* expressions on Notes 1 and 2 modified; *tcyc* expression added
		65	• **Table 5.28 Memory Expansion Mode and Microprocessor Mode** *tac1(RD-DB)* expression on Note 1 modified; *tac2(RD-DB)* expression on Note 1 added
		70	• **Figure 5.7 Vcc1=Vcc2=3.3V Timing Diagram (1)** *tW(ER)* expression on Note 3 modified; *tcyc* expression added
		71	• **Figure 5.8 Vcc1=Vcc2=3.3V Timing Diagram (2)** *tac2(RD-DB)* expression on Note 1 modified; *th(ALE-AD)* expressions on Notes 1 and 2 modified; *th(WR-CS)* expression on Note 2 modified; *tcyc* expression added
		76	• **Table 5.43 Electrical Characteristics** Parameter f(BCLK) and its values added
		80	• **Table 5.47 Flash Memory Version Electrical Characteristics** Mesurement condition changed