Renesas Electronics America Inc - M30855FWGP#U3 Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	M32C/80
Core Size	16/32-Bit
Speed	32MHz
Connectivity	CANbus, I²C, IEBus, SIO, UART/USART
Peripherals	DMA, WDT
Number of I/O	121
Program Memory Size	320KB (320K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 34x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LFQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m30855fwgp-u3

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1. Overview

The M32C/85 group (M32C/85, M32C/85T) microcomputer is a single-chip control unit that utilizes high-performance silicon gate CMOS technology with the M32C/80 series CPU core. The M32C/85 group (M32C/85, M32C/85T) is available in 144-pin and 100-pin plastic molded LQFP/QFP packages.

With a 16-Mbyte address space, this microcomputer combines advanced instruction manipulation capabilities to process complex instructions by less bytes and execute instructions at higher speed.

It includes a multiplier and DMAC adequate for office automation, communication devices and industrial equipments, and other high-speed processing applications.

1.1 Applications

Automobiles, audio, cameras, office equipment, communications equipment, portable equipment, etc.

1.4 Product Information

Table 1.3 lists the product information. Figure 1.2 shows the product numbering system.

Table 1.3 M32C/85 Group (1) (M32C/85) **As of July, 2005**

Type Number	Package Type	ROM Capacity	RAM Capacity	Remarks
M30855FJGP	PLQP0144KA-A (144P6Q-A)	512K+4K	24K	Flash Memory
M30853FJGP	PLQP0100KB-A (100P6Q-A)			
M30853FJFP	PRQP0100JB-A (100P6S-A)			
M30855FHGP	PLQP0144KA-A (144P6Q-A)	384K+4K		
M30853FHGP	PLQP0100KB-A (100P6Q-A)			
M30853FHFP	PRQP0100JB-A (100P6S-A)			
M30855FWGP	PLQP0144KA-A (144P6Q-A)	320K+4K		
M30853FWGP	PLQP0100KB-A (100P6Q-A)			
M30853FWFP	PRQP0100JB-A (100P6S-A)			
M30855MW-XXXGP	PLQP0144KA-A (144P6Q-A)	320K		Mask ROM
M30853MW-XXXGP	PLQP0100KB-A (100P6Q-A)			
M30853MW-XXXFP	PRQP0100JB-A (100P6S-A)			

Table 1.3 M32C/85 Group (2) (T Version, M32C/85T) **As of July, 2005**

Type Number	Package Type	ROM Capacity	RAM Capacity	Remarks
M30855FJTGP	PLQP0144KA-A (144P6Q-A)	512K+4K	24K	Flash Memory T Version (High-reliability 85°C Version)
M30853FJTGP	PLQP0100KB-A (100P6Q-A)			
M30855FHTGP	PLQP0144KA-A (144P6Q-A)	384K+4K		
M30853FHTGP	PLQP0100KB-A (100P6Q-A)			
M30855FWTGP	PLQP0144KA-A (144P6Q-A)	320K+4K		
M30853FWTGP	PLQP0100KB-A (100P6Q-A)			

1.5 Pin Assignments and Descriptions

Figures 1.3 to 1.5 show pin assignments (top view).

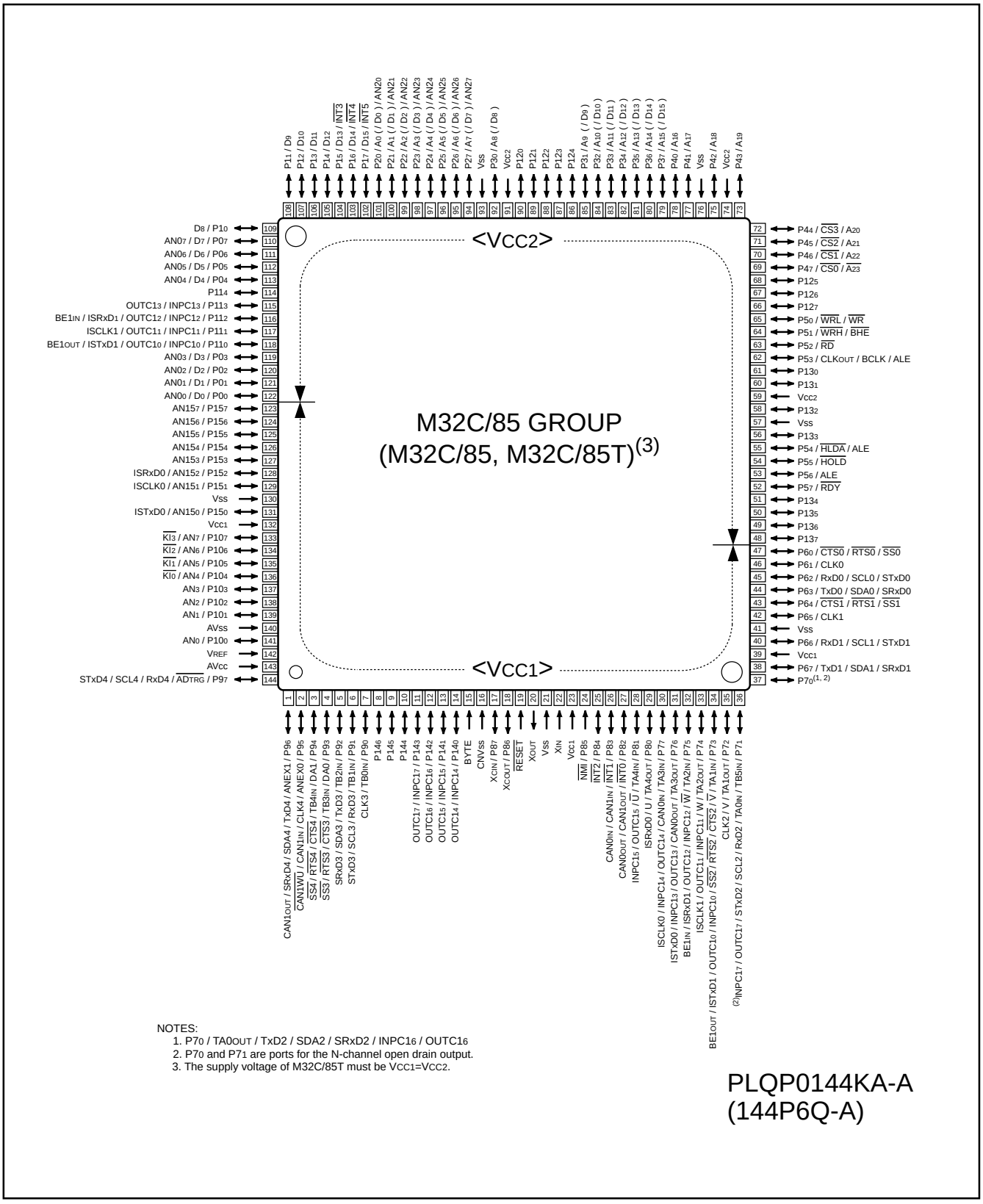
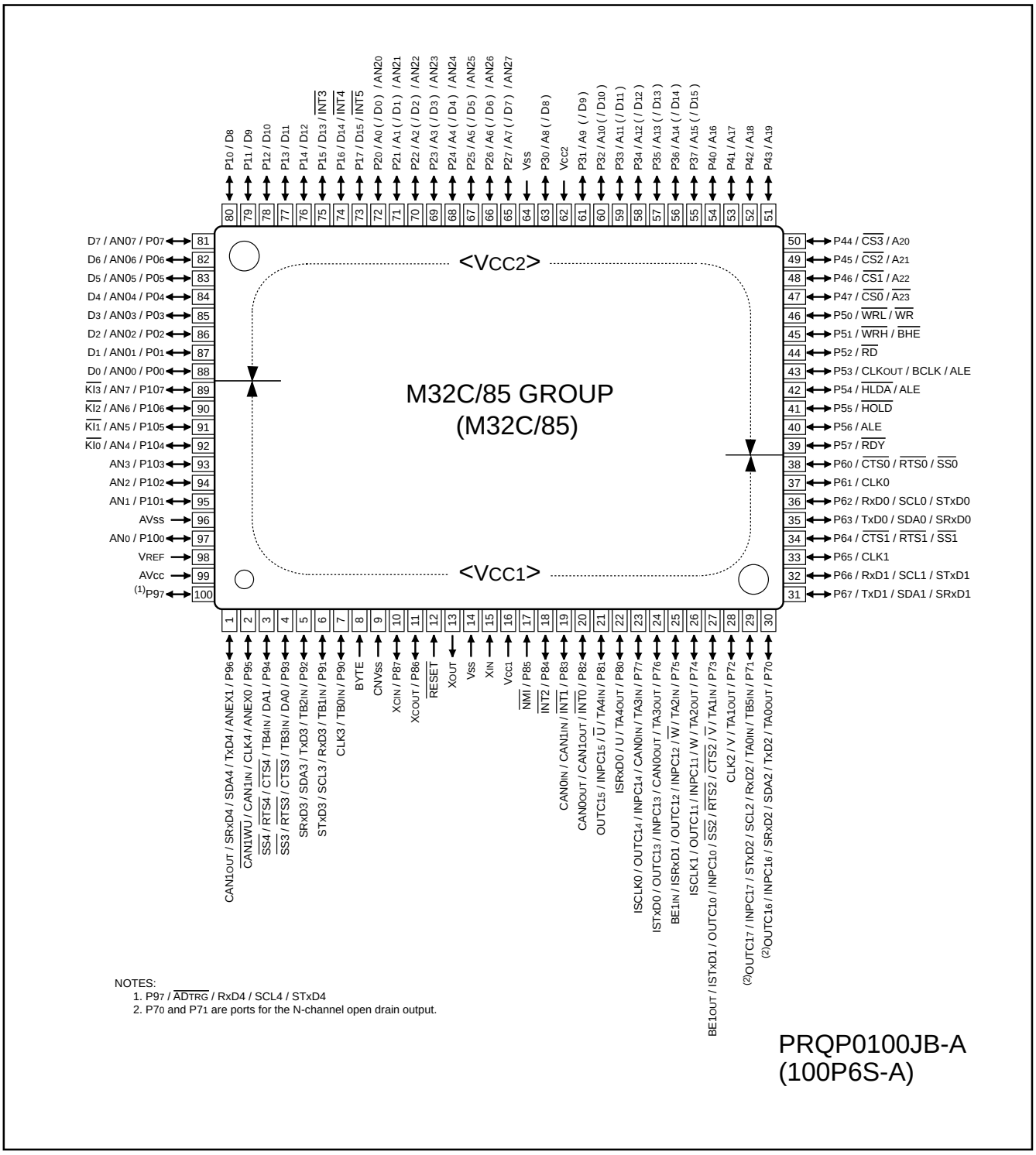


Figure 1.3 Pin Assignment for 144-Pin Package



NOTES:
1. P97 / ADTRG / RxD4 / SCL4 / STxD4
2. P70 and P71 are ports for the N-channel open drain output.

Figure 1.5 Pin Assignment for 100-Pin Package

Table 1.6 Pin Description (100-Pin and 144-Pin Packages) (Continued)

Classsfication	Symbol	I/O Type	Supply Voltage	Function
Main Clock Input	XIN	I	VCC1	I/O pins for the main clock oscillation circuit. Connect a ceramic resonator or crystal oscillator between XIN and XOUT. To apply external clock, apply it to XIN and leave XOUT open
Main Clock Output	XOUT	O	VCC1	
Sub Clock Input	XCIN	I	VCC1	I/O pins for the sub clock oscillation circuit. Connect a crystal oscillator between XCIN and XCOUT. To apply external clock, apply it to XCIN and leave XCOUT open
Sub Clock Output	XCOUT	O	VCC1	
BCLK Output(1)	BCLK	O	VCC2	Outputs BCLK signal
Clock Output	CLKOUT	O	VCC2	Outputs the clock having the same frequency as fC, f8 or f32
$\overline{\text{INT}}$ Interrupt Input	$\overline{\text{INT0}}$ to $\overline{\text{INT2}}$	I	VCC1	Input pins for the $\overline{\text{INT}}$ interrupt
	$\overline{\text{INT3}}$ to $\overline{\text{INT5}}$		VCC2	
$\overline{\text{NMI}}$ Interrupt Input	$\overline{\text{NMI}}$	I	VCC1	Input pin for the $\overline{\text{NMI}}$ interrupt
Key Input Interrupt	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	I	VCC1	Input pins for the key input interrupt
Timer A	TA0OUT to TA4OUT	I/O	VCC1	I/O pins for the timer A0 to A4 (TA0OUT is a pin for the N-channel open drain output.)
	TA0IN to TA4IN	I	VCC1	Input pins for the timer A0 to A4
Timer B	TB0IN to TB5IN	I	VCC1	Input pins for the timer B0 to B5
Three-phase Motor Control Timer Output	U, $\overline{\text{U}}$, V, $\overline{\text{V}}$, W, $\overline{\text{W}}$	O	VCC1	Output pins for the three-phase motor control timer
Serial I/O	$\overline{\text{CTS0}}$ to $\overline{\text{CTS4}}$	I	VCC1	Input pins for data transmission control
	$\overline{\text{RTS0}}$ to $\overline{\text{RTS4}}$	O	VCC1	Output pins for data reception control
	CLK0 to CLK4	I/O	VCC1	Inputs and outputs the transfer clock
	RxD0 to RxD4	I	VCC1	Inputs serial data
	TxD0 to TxD4	O	VCC1	Outputs serial data (TxD2 is a pin for the N-channel open drain output.)
I^2C Mode	SDA0 to SDA4	I/O	VCC1	Inputs and outputs serial data (SDA2 is a pin for the N-channel open drain output.)
	SCL0 to SCL4			Inputs and outputs the transfer clock (SCL2 is a pin for the N-channel open drain output.)
Serial I/O Special Function	STxD0 to STxD4	O	VCC1	Outputs serial data when slave mode is selected (STxD2 is a pin for the N-channel open drain output.)
	SRxD0 to SRxD4	I		Inputs serial data when slave mode is selected
	$\overline{\text{SS0}}$ to $\overline{\text{SS4}}$	I	VCC1	Input pins to control serial I/O special function

I : Input O : Output I/O : Input and output

NOTES:

1. Bus control pins in M32C/85T cannot be used.

Table 1.6 Pin Description (100-Pin and 144-Pin Packages) (Continued)

Classsfication	Symbol	I/O Type	Supply Voltage	Function
Reference Voltage Input	V_{REF}	I	-	Applies reference voltage to the A/D converter and D/A converter
A/D Converter	AN_0 to AN_7 $AN0_0$ to $AN0_7$ $AN2_0$ to $AN2_7$	I	V_{CC1}	Analog input pins for the A/D converter
	$\overline{ADTRG}$	I	V_{CC1}	Input pin for an external A/D trigger
	ANEX0	I/O	V_{CC1}	Extended analog input pin for the A/D converter and output pin in external op-amp connection mode
	ANEX1	I	V_{CC1}	Extended analog input pin for the A/D converter
D/A Converter	DA0, DA1	O	V_{CC1}	Output pin for the D/A converter
Intelligent I/O	$INPC1_0$ to $INPC1_3$	I	V_{CC1}/V_{CC2}(1)	Input pins for the time measurement function
	$INPC1_4$ to $INPC1_7$		V_{CC1}	
	$OUTC1_0$ to $OUTC1_3$	O	V_{CC1}/V_{CC2}(1)	Output pins for the waveform generating function
	$OUTC1_4$ to $OUTC1_7$		V_{CC1}	($OUTC1_6$ and $OUTC1_7$ assigned to $P7_0$ and $P7_1$ are pins for the N-channel open drain output.)
	ISCLK0	I/O	V_{CC1}	Inputs and outputs the clock for the intelligent I/O communication function
	ISCLK1		V_{CC1}/V_{CC2}(1)	
	ISRXD0	I	V_{CC1}	Inputs data for the intelligent I/O communication function
	ISRXD1		V_{CC1}/V_{CC2}(1)	
	ISTXD0	O	V_{CC1}	Outputs data for the intelligent I/O communication function
	ISTXD1		V_{CC1}/V_{CC2}(1)	
	$BE1_{IN}$	I	V_{CC1}/V_{CC2}(1)	Inputs data for the intelligent I/O communication function
	$BE1_{OUT}$	O	V_{CC1}/V_{CC2}(1)	Outputs data for the intelligent I/O communication function
CAN	$CAN0_{IN}$	I	V_{CC1}	Input pin for the CAN communication function
	$CAN1_{IN}$			
	$CAN0_{OUT}$	O		Output pin for the CAN communication function
	$CAN1_{OUT}$			
	$\overline{CAN1WU}$	I		Input pin for the CAN1 wake-up interrupt
I/O Ports	$P0_0$ to $P0_7$ $P1_0$ to $P1_7$ $P2_0$ to $P2_7$ $P3_0$ to $P3_7$ $P4_0$ to $P4_7$ $P5_0$ to $P5_7$	I/O	V_{CC2}	I/O ports for CMOS. Each port can be programmed for input or output under the control of the direction register. An input port can be set, by program, for a pull-up resistor available or for no pull-up resister available in 4-bit units
	$P6_0$ to $P6_7$ $P7_0$ to $P7_7$ $P9_0$ to $P9_7$ $P10_0$ to $P10_7$	I/O	V_{CC1}	I/O ports having equivalent functions to P0 ($P7_0$ and $P7_1$ are ports for the N-channel open drain output.)
	$P8_0$ to $P8_4$ $P8_6$, $P8_7$	I/O	V_{CC1}	I/O ports having equivalent functions to P0
Input Port	$P8_5$	I	V_{CC1}	Shares a pin with $\overline{NMI}$. $\overline{NMI}$ input state can be got by reading $P8_5$

I : Input O : Output I/O : Input and output

NOTES:

1. V_{CC2} is not available in the 100-pin package. V_{CC1} only available.

Address	Register	Symbol	Value after RESET
006016			
006116			
006216			
006316			
006416			
006516			
006616			
006716			
006816	DMA0 Interrupt Control Register	DM0IC	XXXX X0002
006916	Timer B5 Interrupt Control Register	TB5IC	XXXX X0002
006A16	DMA2 Interrupt Control Register	DM2IC	XXXX X0002
006B16	UART2 Receive /ACK Interrupt Control Register	S2RIC	XXXX X0002
006C16	Timer A0 Interrupt Control Register	TA0IC	XXXX X0002
006D16	UART3 Receive /ACK Interrupt Control Register	S3RIC	XXXX X0002
006E16	Timer A2 Interrupt Control Register	TA2IC	XXXX X0002
006F16	UART4 Receive /ACK Interrupt Control Register	S4RIC	XXXX X0002
007016	Timer A4 Interrupt Control Register	TA4IC	XXXX X0002
007116	UART0/UART3 Bus Conflict Detect Interrupt Control Register	BCN0IC/BCN3IC	XXXX X0002
007216	UART0 Receive/ACK Interrupt Control Register	S0RIC	XXXX X0002
007316	A/D0 Conversion Interrupt Control Register	AD0IC	XXXX X0002
007416	UART1 Receive/ACK Interrupt Control Register	S1RIC	XXXX X0002
007516	Intelligent I/O Interrupt Control Register 0/ CAN Interrupt 3 Control Register	IIO0IC/ CAN3IC	XXXX X0002
007616	Timer B1 Interrupt Control Register	TB1IC	XXXX X0002
007716	Intelligent I/O Interrupt Control Register 2	IIO2IC	XXXX X0002
007816	Timer B3 Interrupt Control Register	TB3IC	XXXX X0002
007916	Intelligent I/O Interrupt Control Register 4	IIO4IC	XXXX X0002
007A16	INT5 Interrupt Control Register	INT5IC	XX00 X0002
007B16			
007C16	INT3 Interrupt Control Register	INT3IC	XX00 X0002
007D16	Intelligent I/O Interrupt Control Register 8	IIO8IC	XXXX X0002
007E16	INT1 Interrupt Control Register	INT1IC	XX00 X0002
007F16	Intelligent I/O Interrupt Control Register 10/ CAN Interrupt 1 Control Register	IIO10IC/ CAN1IC	XXXX X0002
008016			
008116	CAN Interrupt 2 Control Register	CAN2IC	XXXX X0002
008216			
008316			
008416			
008516			
008616			
008716			
008816	DMA1 Interrupt Control Register	DM1IC	XXXX X0002
008916	UART2 Transmit /NACK Interrupt Control Register	S2TIC	XXXX X0002
008A16	DMA3 Interrupt Control Register	DM3IC	XXXX X0002
008B16	UART3 Transmit /NACK Interrupt Control Register	S3TIC	XXXX X0002
008C16	Timer A1 Interrupt Control Register	TA1IC	XXXX X0002
008D16	UART4 Transmit /NACK Interrupt Control Register	S4TIC	XXXX X0002
008E16	Timer A3 Interrupt Control Register	TA3IC	XXXX X0002
008F16	UART2 Bus Conflict Detect Interrupt Control Register	BCN2IC	XXXX X0002

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
0210$_{16}$ 0211$_{16}$	CAN0 Slot Interrupt Mask Register	C0SIMKR	00$_{16}$(2) 00$_{16}$(2)
0212$_{16}$			
0213$_{16}$			
0214$_{16}$	CAN0 Error Interrupt Mask Register	C0EIMKR	XXXX X000$_2$(2)
0215$_{16}$	CAN0 Error Interrupt Status Register	C0EISTR	XXXX X000$_2$(2)
0216$_{16}$	CAN0 Error Cause Register	C0EFR	00$_{16}$(2)
0217$_{16}$	CAN0 Baud Rate Prescaler	C0BRP	0000 0001$_2$(2)
0218$_{16}$			
0219$_{16}$	CAN0 Mode Register	C0MDR	XXXX XX00$_2$(2)
021A$_{16}$			
021B$_{16}$			
021C$_{16}$			
021D$_{16}$			
021E$_{16}$			
021F$_{16}$			
0220$_{16}$ 0221$_{16}$	CAN0 Single Shot Control Register	C0SSCTLR	00$_{16}$(2) 00$_{16}$(2)
0222$_{16}$			
0223$_{16}$			
0224$_{16}$ 0225$_{16}$	CAN0 Single Shot Status Register	C0SSSTR	00$_{16}$(2) 00$_{16}$(2)
0226$_{16}$			
0227$_{16}$			
0228$_{16}$	CAN0 Global Mask Register Standard ID0	C0GMR0	XXX0 0000$_2$(2)
0229$_{16}$	CAN0 Global Mask Register Standard ID1	C0GMR1	XX00 0000$_2$(2)
022A$_{16}$	CAN0 Global Mask Register Extended ID0	C0GMR2	XXXX 0000$_2$(2)
022B$_{16}$	CAN0 Global Mask Register Extended ID1	C0GMR3	00$_{16}$(2)
022C$_{16}$	CAN0 Global Mask Register Extended ID2	C0GMR4	XX00 0000$_2$(2)
022D$_{16}$			
022E$_{16}$			
022F$_{16}$			
0230$_{16}$	CAN0 Message Slot 0 Control Register / CAN0 Local Mask Register A Standard ID0	C0MCTL0/ C0LMAR0	0000 0000$_2$(2) XXX0 0000$_2$(2)
0231$_{16}$	CAN0 Message Slot 1 Control Register / CAN0 Local Mask Register A Standard ID1	C0MCTL1/ C0LMAR1	0000 0000$_2$(2) XX00 0000$_2$(2)
0232$_{16}$	CAN0 Message Slot 2 Control Register / CAN0 Local Mask Register A Extended ID0	C0MCTL2/ C0LMAR2	0000 0000$_2$(2) XXXX 0000$_2$(2)
0233$_{16}$	CAN0 Message Slot 3 Control Register / CAN0 local Mask Register A Extended ID1	C0MCTL3/ C0LMAR3	00$_{16}$(2) 00$_{16}$(2)
0234$_{16}$	CAN0 Message Slot 4 Control Register / CAN0 Local Mask Register A Extended ID2	C0MCTL4/ C0LMAR4	0000 0000$_2$(2) XX00 0000$_2$(2)
0235$_{16}$	CAN0 Message Slot 5 Control Register	C0MCTL5	00$_{16}$(2)
0236$_{16}$	CAN0 Message Slot 6 Control Register	C0MCTL6	00$_{16}$(2)
0237$_{16}$	CAN0 Message Slot 7 Control Register	C0MCTL7	00$_{16}$(2)
0238$_{16}$	CAN0 Message Slot 8 Control Register / CAN0 Local Mask Register B Standard ID0	C0MCTL8/ C0LMBR0	0000 0000$_2$(2) XXX0 0000$_2$(2)
0239$_{16}$	CAN0 Message Slot 9 Control Register / CAN0 Local Mask Register B Standard ID1	C0MCTL9/ C0LMBR1	0000 0000$_2$(2) XX00 0000$_2$(2)

(Note 1)

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTES:

1. The BANKSEL bit in the C0CTLR1 register switches functions for addresses 0220$_{16}$ to 023F$_{16}$.
2. Values are obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) after reset and applying the clock to the CAN module.

Address	Register	Symbol	Value after RESET
029016 029116	CAN1 Slot Interrupt Mask Register	C1SIMKR	0016 0016
029216			
029316			
029416	CAN1 Error Interrupt Mask Register	C1EIMKR	XXXX X0002(2)
029516	CAN1 Error Interrupt Status Register	C1EISTR	XXXX X0002(2)
029616	CAN1 Error Factor Register	C1EFR	0016(2)
029716	CAN1 Baud Rate Prescaler	C1BRP	0000 00012(2)
029816			
029916	CAN1 Mode Register	C1MDR	XXXX XX002(2)
029A16			
029B16			
029C16			
029D16			
029E16			
029F16			
02A016 02A116	CAN1 Single Shot Control Register	C1SSCTLR	0016(2) 0016(2)
02A216			
02A316			
02A416 02A516	CAN1 Single Shot Status Register	C1SSSTR	0016(2) 0016(2)
02A616			
02A716			
02A816	CAN1 Global Mask Register Standard ID0	C1GMR0	XXX0 00002(2)
02A916	CAN1 Global Mask Register Standard ID1	C1GMR1	XX00 00002(2)
02AA16	CAN1 Global Mask Register Extended ID0	C1GMR2	XXXX 00002(2)
02AB16	CAN1 Global Mask Register Extended ID1	C1GMR3	0016(2)
02AC16	CAN1 Global Mask Register Extended ID2	C1GMR4	XX00 00002(2)
02AD16			
02AE16			
02AF16			
02B016	CAN1 Message Slot 0 Control Register / CAN1 Local Mask Register A Standard ID0	C1MCTL0/ C1LMAR0	0000 00002(2) XXX0 00002(2)
02B116	CAN1 Message Slot 1 Control Register / CAN1 Local Mask Register A Standard ID1	C1MCTL1/ C1LMAR1	0000 00002(2) XX00 00002(2)
02B216	CAN1 Message Slot 2 Control Register / CAN1 Local Mask Register A Extended ID0	C1MCTL2/ C1LMAR2	0000 00002(2) XXXX 00002(2)
02B316	CAN1 Message Slot 3 Control Register / CAN1 Local Mask Register A Extended ID1	C1MCTL3/ C1LMAR3	0016(2) 0016(2)
02B416	CAN1 Message Slot 4 Control Register / CAN1 Local Mask Register A Extended ID2	C1MCTL4/ C1LMAR4	0000 00002(2) XX00 00002(2)
02B516	CAN1 Message Slot 5 Control Register	C1MCTL5	0016(2)
02B616	CAN1 Message Slot 6 Control Register	C1MCTL6	0016(2)
02B716	CAN1 Message Slot 7 Control Register	C1MCTL7	0016(2)
02B816	CAN1 Message Slot 8 Control Register / CAN1 Local Mask Register B Standard ID0	C1MCTL8/ C1LMBR0	0000 00002(2) XXX0 00002(2)
02B916	CAN1 Message Slot 9 Control Register / CAN1 Local Mask Register B Standard ID1	C1MCTL9/ C1LMBR1	0000 00002(2) XX00 00002(2)

(Note 1)

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTES:

1. The BANKSEL bit in the C1CTLR1 register switches functions for addresses 02A016 to 02BF16.
2. Values are obtained by setting the SLEEP bit in the C1SLPR register to "1" (sleep mode exited) after reset and applying the clock to the CAN module.

Address	Register	Symbol	Value after RESET
0310$_{16}$	Timer B3 Register	TB3	XX$_{16}$
0311$_{16}$			XX$_{16}$
0312$_{16}$	Timer B4 Register	TB4	XX$_{16}$
0313$_{16}$			XX$_{16}$
0314$_{16}$	Timer B5 Register	TB5	XX$_{16}$
0315$_{16}$			XX$_{16}$
0316$_{16}$			
0317$_{16}$			
0318$_{16}$			
0319$_{16}$			
031A$_{16}$			
031B$_{16}$	Timer B3 Mode Register	TB3MR	00XX 0000$_2$
031C$_{16}$	Timer B4 Mode Register	TB4MR	00XX 0000$_2$
031D$_{16}$	Timer B5 Mode Register	TB5MR	00XX 0000$_2$
031E$_{16}$			
031F$_{16}$	External Interrupt Request Source Select Register	IFSR	00$_{16}$
0320$_{16}$			
0321$_{16}$			
0322$_{16}$			
0323$_{16}$			
0324$_{16}$	UART3 Special Mode Register 4	U3SMR4	00$_{16}$
0325$_{16}$	UART3 Special Mode Register 3	U3SMR3	00$_{16}$
0326$_{16}$	UART3 Special Mode Register 2	U3SMR2	00$_{16}$
0327$_{16}$	UART3 Special Mode Register	U3SMR	00$_{16}$
0328$_{16}$	UART3 Transmit/Receive Mode Register	U3MR	00$_{16}$
0329$_{16}$	UART3 Bit Rate Register	U3BRG	XX$_{16}$
032A$_{16}$	UART3 Transmit Buffer Register	U3TB	XX$_{16}$
032B$_{16}$			XX$_{16}$
032C$_{16}$	UART3 Transmit/Receive Control Register 0	U3C0	0000 1000$_2$
032D$_{16}$	UART3 Transmit/Receive Control Register 1	U3C1	0000 0010$_2$
032E$_{16}$	UART3 Receive Buffer Register	U3RB	XX$_{16}$
032F$_{16}$			XX$_{16}$
0330$_{16}$			
0331$_{16}$			
0332$_{16}$			
0333$_{16}$			
0334$_{16}$	UART2 Special Mode Register 4	U2SMR4	00$_{16}$
0335$_{16}$	UART2 Special Mode Register 3	U2SMR3	00$_{16}$
0336$_{16}$	UART2 Special Mode Register 2	U2SMR2	00$_{16}$
0337$_{16}$	UART2 Special Mode Register	U2SMR	00$_{16}$
0338$_{16}$	UART2 Transmit/Receive Mode Register	U2MR	00$_{16}$
0339$_{16}$	UART2 Bit Rate Register	U2BRG	XX$_{16}$
033A$_{16}$	UART2 Transmit Buffer Register	U2TB	XX$_{16}$
033B$_{16}$			XX$_{16}$
033C$_{16}$	UART2 Transmit/Receive Control Register 0	U2C0	0000 1000$_2$
033D$_{16}$	UART2 Transmit/Receive Control Register 1	U2C1	0000 0010$_2$
033E$_{16}$	UART2 Receive Buffer Register	U2RB	XX$_{16}$
033F$_{16}$			XX$_{16}$

X: Indeterminate

Blank spaces are reserved. No access is allowed.

<100-pin package>

Address	Register	Symbol	Value after RESET
03D0$_{16}$			
03D1$_{16}$			
03D2$_{16}$	Set default value to "FF$_{16}$"		
03D3$_{16}$	Set default value to "FF$_{16}$"		
03D4$_{16}$			
03D5$_{16}$			
03D6$_{16}$			
03D7$_{16}$			
03D8$_{16}$			
03D9$_{16}$			
03DA$_{16}$	Pull-Up Control Register 2	PUR2	00$_{16}$
03DB$_{16}$	Pull-Up Control Register 3	PUR3	00$_{16}$
03DC$_{16}$	Set default value to "00$_{16}$"		
03DD$_{16}$			
03DE$_{16}$			
03DF$_{16}$			
03E0$_{16}$	Port P0 Register	P0	XX$_{16}$
03E1$_{16}$	Port P1 Register	P1	XX$_{16}$
03E2$_{16}$	Port P0 Direction Register	PD0	00$_{16}$
03E3$_{16}$	Port P1 Direction Register	PD1	00$_{16}$
03E4$_{16}$	Port P2 Register	P2	XX$_{16}$
03E5$_{16}$	Port P3 Register	P3	XX$_{16}$
03E6$_{16}$	Port P2 Direction Register	PD2	00$_{16}$
03E7$_{16}$	Port P3 Direction Register	PD3	00$_{16}$
03E8$_{16}$	Port P4 Register	P4	XX$_{16}$
03E9$_{16}$	Port P5 Register	P5	XX$_{16}$
03EA$_{16}$	Port P4 Direction Register	PD4	00$_{16}$
03EB$_{16}$	Port P5 Direction Register	PD5	00$_{16}$
03EC$_{16}$			
03ED$_{16}$			
03EE$_{16}$			
03EF$_{16}$			
03F0$_{16}$	Pull-up Control Register 0	PUR0	00$_{16}$
03F1$_{16}$	Pull-up Control Register 1	PUR1	XXXX 0000$_{2}$
03F2$_{16}$			
03F3$_{16}$			
03F4$_{16}$			
03F5$_{16}$			
03F6$_{16}$			
03F7$_{16}$			
03F8$_{16}$			
03F9$_{16}$			
03FA$_{16}$			
03FB$_{16}$			
03FC$_{16}$			
03FD$_{16}$			
03FE$_{16}$			
03FF$_{16}$	Port Control Register	PCR	XXXX XXX0$_{2}$

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Table 5.2 Recommended Operating Conditions (Continued)
(V_{CC1}=V_{CC2}=3.0V to 5.5V at Topr=–20 to 85°C unless otherwise specified)

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
$f(BCLK)$	CPU Clock Frequency	V_{CC1}=4.2 to 5.5V	0		32	MHz
		V_{CC1}=3.0 to 5.5V	0		24	MHz
$f(X_{IN})$	Main Clock Input Frequency	V_{CC1}=4.2 to 5.5V	0		32	MHz
		V_{CC1}=3.0 to 5.5V	0		24	MHz
$f(X_{CIN})$	Sub Clock Frequency			32.768	50	kHz
$f(Ring)$	On-chip Oscillator Frequency (V_{CC1}=V_{CC2}=5.0V, Topr=25° C)		0.5	1	2	MHz
$f(PLL)$	PLL Clock Frequency	V_{CC1}=4.2 to 5.5V	10		32	MHz
		V_{CC1}=3.0 to 5.5V	10		24	MHz
$t_{SU(PLL)}$	Wait Time to Stabilize PLL Frequency Synthesizer	V_{CC1}=5.0V			5	ms
		V_{CC1}=3.3V			10	ms

$V_{CC1}=V_{CC2}=5V$

Timing Requirements

($V_{CC1}=V_{CC2}=4.2$ to 5.5V, $V_{SS}=0V$ at Topr=–20 to 85°C unless otherwise specified)

Table 5.9 External Clock Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc	External Clock Input Cycle Time	31.25		ns
$t_{W(H)}$	External Clock Input High ("H") Width	13.75		ns
$t_{W(L)}$	External Clock Input Low ("L") Width	13.75		ns
tr	External Clock Rise Time		5	ns
tf	External Clock Fall Time		5	ns

Table 5.10 Memory Expansion Mode and Microprocessor Mode

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{ac1(RD-DB)}$	Data Input Access Time (RD standard)		(Note 1)	ns
$t_{ac1(AD-DB)}$	Data Input Access Time (AD standard, CS standard)		(Note 1)	ns
$t_{ac2(RD-DB)}$	Data Input Access Time (RD standard, when accessing a space with the multiplexed bus)		(Note 1)	ns
$t_{ac2(AD-DB)}$	Data Input Access Time (AD standard, when accessing a space with the multiplexed bus)		(Note 1)	ns
$t_{su(DB-BCLK)}$	Data Input Setup Time	26		ns
$t_{su(RDY-BCLK)}$	$\overline{RDY}$ Input Setup Time	26		ns
$t_{su(HOLD-BCLK)}$	$\overline{HOLD}$ Input Setup Time	30		ns
$t_{h(RD-DB)}$	Data Input Hold Time	0		ns
$t_{h(BCLK-RDY)}$	$\overline{RDY}$ Input Hold Time	0		ns
$t_{h(BCLK-HOLD)}$	$\overline{HOLD}$ Input Hold Time	0		ns
$t_{d(BCLK-HLDA)}$	$\overline{HLDA}$ Output Delay Time		25	ns

NOTES:
1. Values can be obtained from the following equations, according to BCLK frequecncy and external bus cycles. Insert a wait state or lower the operation frequency, $f_{(BCLK)}$, if the calculated value is negative.

$$t_{ac1(RD-DB)} = \frac{10^9 \times m}{f_{(BCLK)} \times 2} - 35$$ [ns] (if external bus cycle is aϕ + bϕ, m=(bx2)+1)

$$t_{ac1(AD-DB)} = \frac{10^9 \times n}{f_{(BCLK)}} - 35$$ [ns] (if external bus cycle is aϕ + bϕ, n=a+b)

$$t_{ac2(RD-DB)} = \frac{10^9 \times m}{f_{(BCLK)} \times 2} - 35$$ [ns] (if external bus cycle is aϕ + bϕ, m=(bx2)-1)

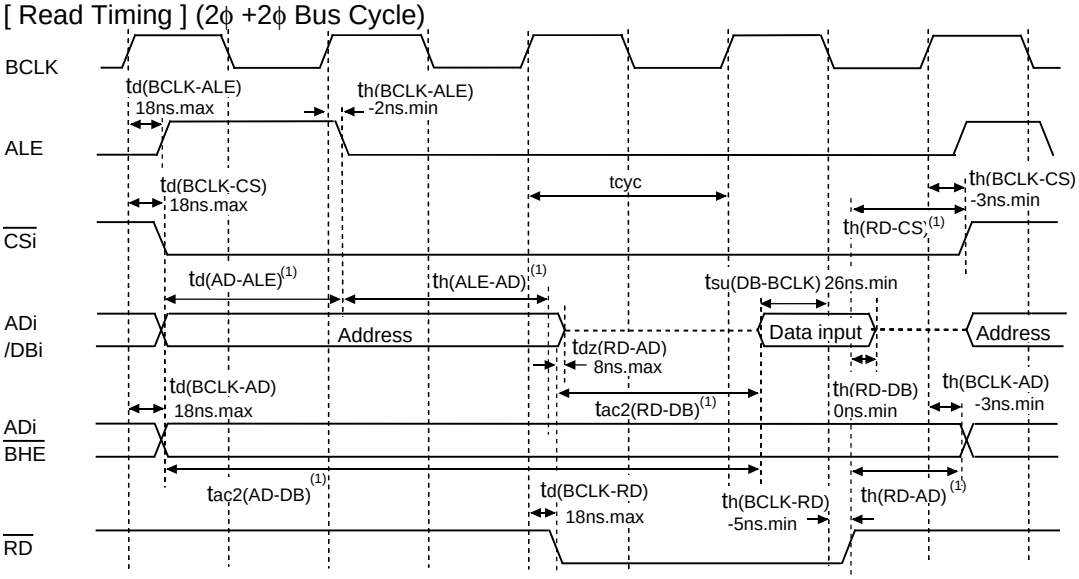
$$t_{ac2(AD-DB)} = \frac{10^9 \times p}{f_{(BCLK)} \times 2} - 35$$ [ns] (if external bus cycle is aϕ + bϕ, p={(a+b-1)x2}+1)

$V_{CC1}=V_{CC2}=5V$

Memory Expansion Mode and Microprocessor Mode

(when accessing an external memory space with the multiplexed bus)

[Read Timing] (2φ +2φ Bus Cycle)



NOTES:

1. Varies with operation frequency:

$t_{d(AD-ALE)}$=(tcyc/2 x n-20)ns.min (if external bus cycle is aφ + bφ, n=a)

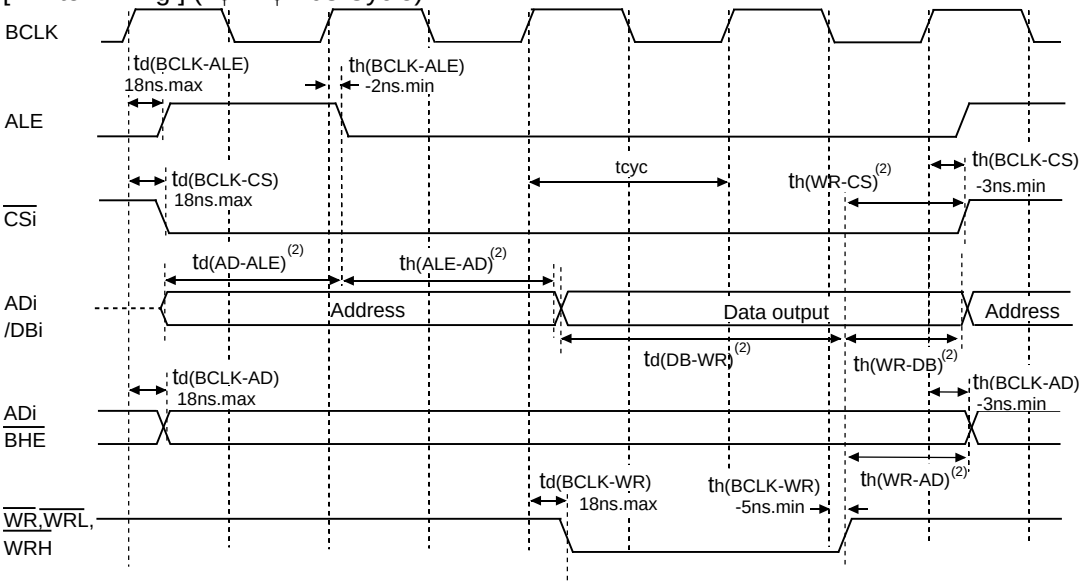
$t_{h(ALE-AD)}$=(tcyc/2 x n-10)ns.min (if external bus cycle is aφ + bφ, n=a)

$t_{h(RD-AD)}$=(tcyc/2-10)ns.min, $t_{h(RD-CS)}$=(tcyc/2-10)ns.min

$t_{ac2(RD-DB)}$=(tcyc/2 x m-35)ns.max (if external bus cycle is aφ + bφ, m=(b x 2)-1)

$t_{ac2(AD-DB)}$=(tcyc/2 x p-35)ns.max (if external bus cycle is aφ + bφ, p={(a+b-1) x 2}+1)

[Write Timing] (2φ +2φ Bus Cycle)



NOTES:

2. Varies with operation frequency:

$t_{d(AD-ALE)}$=(tcyc/2 x n - 20)ns.min

(if external bus cycle is aφ + bφ, n=a)

$t_{h(ALE-AD)}$=(tcyc/2 x n -10)ns.min

(if external bus cycle is aφ + bφ, n=a)

$t_{h(WR-AD)}$=(tcyc/2-10)ns.min,

$t_{h(WR-CS)}$=(tcyc/2-10)ns.min, $t_{h(WR-DB)}$=(tcyc/2-10)ns.min

$t_{d(DB-WR)}$=(tcyc/2 x m-25)ns.min

(if external bus cycle is aφ + bφ, m=(b x 2)-1)

Measurement Conditions:

- $V_{CC1}=V_{CC2}$=4.2 to 5.5V
- Input high and low voltage: V_{IH}=2.5V, V_{IL}=0.8V
- Output high and low voltage: V_{OH}=2.0V, V_{OL}=0.8V

$$tcyc=\frac{10^9}{f_{(BCLK)}}$$

Figure 5.4 $V_{CC1}=V_{CC2}$=5V Timing Diagram (2)

$V_{CC1}=V_{CC2}=3.3V$

Table 5.24 Electrical Characteristics ($V_{CC1}=V_{CC2}=3.0$ to $3.6V$, $V_{SS}=0V$ at Topr = –20 to 85°C, f(BCLK)=24MHz unless otherwise specified)

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output High ("H") Voltage	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$	I_{OH}=-1mA		V_{CC2}-0.6		V_{CC2}	V
		$P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1)			V_{CC1}-0.6		V_{CC1}	V
		X_{OUT}	I_{OH}=-0.1mA		2.7		V_{CC1}	V
		X_{COUT} High Power	No load applied			2.5		V
		X_{COUT} Low Power	No load applied			1.6		V
V_{OL}	Output Low ("L") Voltage	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1)	I_{OL}=1mA				0.5	V
		X_{OUT}	I_{OL}=0.1mA				0.5	V
		X_{COUT} High Power	No load applied			0		V
		X_{COUT} Low Power	No load applied			0		V
V_{T+}-V_{T-}	Hysteresis	$\overline{HOLD}$, $\overline{RDY}$, $TA0_{IN}$-$TA4_{IN}$, $TB0_{IN}$-$TB5_{IN}$, $\overline{INT0}$-$\overline{INT5}$, $\overline{ADTRG}$, $\overline{CTS0}$-$\overline{CTS4}$, CLK0-CLK4, $TA0_{OUT}$-$TA4_{OUT}$, $\overline{NMI}$, $\overline{KI0}$-$\overline{KI3}$, RxD0-RxD4, SCL0-SCL4, SDA0-SDA4			0.2		1.0	V
		$\overline{RESET}$			0.2		1.8	V
I_{IH}	Input High ("H") Current	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1), X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE	V_I=3V				4.0	µA
I_{IL}	Input Low ("L") Current	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1), X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE	V_I=0V				-4.0	µA
R_{PULLUP}	Pull-up Resistance	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(1)	V_I=0V	Flash Memory	66	120	500	kΩ
				Masked ROM	40	70	500	kΩ
R_{fXIN}	Feedback Resistance	X_{IN}				3.0		MΩ
R_{fXCIN}	Feedback Resistance	X_{CIN}				20.0		MΩ
V_{RAM}	RAM Standby Voltage	in stop mode			2.0			V
I_{CC}	Power Supply Current	Measurement condition: In single-chip mode, output pins are left open and other pins are connected to V_{SS}.	f(BCLK)=24 MHz, Square wave, No division			22	35	mA
			f(BCLK)=32 kHz, In wait mode, Topr=25° C			10		µA
			While clock stops, Topr=25° C			0.8	5	µA
			While clock stops, Topr=85° C				50	µA

NOTES:

1. P11 to P15 are provided in the 144-pin package only.

$V_{CC1}=V_{CC2}=3.3V$

Table 5.25 A/D Conversion Characteristics ($V_{CC1}=V_{CC2}=AV_{CC}=V_{REF}$= 3.0 to 3.6V, $V_{SS}=AV_{SS}$=0V at Topr = –20 to 85°C, f(BCLK) = 24MHz unless otherwise specified)

Symbol	Parameter		Measurement Condition	Standard			Unit
				Min.	Typ.	Max.	
-	Resolution		$V_{REF}=V_{CC1}$			10	Bits
INL	Integral Nonlinearity Error	No S&H (8-bit)	$V_{CC1}=V_{CC2}=V_{REF}$=3.3V			±2	LSB
DNL	Differential Nonlinearity Error	No S&H (8-bit)				±1	LSB
-	Offset Error	No S&H (8-bit)				±2	LSB
-	Gain Error	No S&H (8-bit)				±2	LSB
R_{LADDER}	Resistor Ladder		$V_{REF}=V_{CC1}$	8		40	kΩ
t_{CONV}	8-bit Conversion Time(1, 2)			6.1			µs
V_{REF}	Reference Voltage			3		V_{CC1}	V
V_{IA}	Analog Input Voltage			0		V_{REF}	V

S&H: Sample and Hold

NOTES:
1. Divide f(X_{IN}), if exceeding 10 MHz, to keep ϕAD frequency at 10 MHz or less.
2. S&H not available.

Table 5.26 D/A Conversion Characteristics ($V_{CC1}=V_{CC2}=V_{REF}$=3.0 to 3.6V, $V_{SS}=AV_{SS}$=0V at Topr = –20 to 85°C, f(BCLK) = 24MHz unless otherwise specified)

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min.	Typ.	Max.	
-	Resolution				8	Bits
-	Absolute Accuracy				1.0	%
t_{SU}	Setup Time				3	µs
R_O	Output Resistance		4	10	20	kΩ
I_{VREF}	Reference Power Supply Input Current	(Note 1)			1.0	mA

NOTES:
1. Measurement results when using one D/A converter. The DAi register (i=0, 1) of the D/A converter, not being used, is set to "00_{16}". The resistor ladder in the A/D converter is excluded.
I_{VREF} flows even if the VCUT bit in the AD0CON1 register is set to "0" (no V_{REF} connection).

$V_{CC1}=V_{CC2}=5V$

Table 5.47 Flash Memory Version Electrical Characteristics

(V_{CC1}=4.5 to 5.5V, 3.0 to 3.6V at Topr= 0 to 60°C unless otherwise specified)

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
-	Program and Erase Endurance(2)		100			cycles
-	Word Program Time (V_{CC1}=5.0V, Topr=25° C)			25	200	µs
-	Lock Bit Program Time			25	200	µs
-	Block Erase Time (V_{CC1}=5.0V, Topr=25° C)	4-Kbyte Block		0.3	4	s
		8-Kbyte Block		0.3	4	s
		32-Kbyte Block		0.5	4	s
		64-Kbyte Block		0.8	4	s
-	All-Unlocked-Block Erase Time(1)				4 x *n*	s
t_{PS}	Wait Time to Stabilize Flash Memory Circuit				15	µs
-	Data Hold Time (Topr=-40 to 85 ° C)		10			years

NOTES:
1. *n* denotes the number of block to be erased.
2. Number of program-erase cycles per block.
   If Program and Erase Endurance is *n* cycle (*n*=100), each block can be erased and programmed *n* cycles. For example, if a 4-Kbyte block A is erased after programming a word data 2,048 times, each to a different address, this counts as one program and erase endurance. Data can not be programmed to the same address more than once without erasing the block. (rewrite prohibited).

Table 5.48 Power Supply Timing

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min.	Typ.	Max.	
td(P-R)	Wait Time to Stabilize Internal Supply Voltage when Power-on	V_{CC1}=3.0 to 5.5V			2	ms

$t_{d(P-R)}$
Wait Time to Stabilize Internal Supply Voltage when Power-on

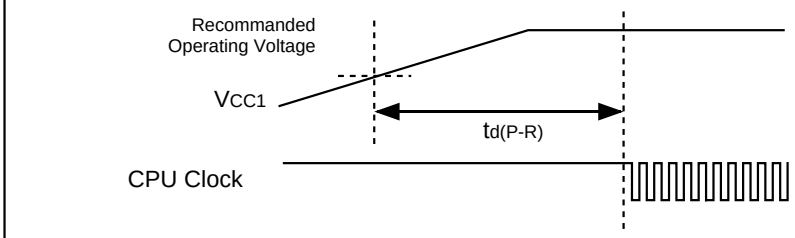


Figure 5.11 Power Supply Timing Diagram

REVISION HISTORY	M32C/85 Group (M32C/85, M32C/85T) Datasheet

Rev.	Date	Description	
		Page	Summary
			Electrical Characteristics
		50	• **Table 5.3 Electrical Characteristics** Maximum values for Power Supply Current modified
		52	• **Table 5.6 Flash Memory Version Electrical Characteristics** Note 1. 100-cycle Products (D3, D5, U3, U5) deleted; Note 4 modified
			• **Table 5.7 Flash Memory Version Program and Erase Voltage and Read Operation Voltage Characteristics (at Topr=0 to 60°C)** deleted
		63	• **Table 5.22 Electrical Characteristics** Maximum values for Power Supply Consumption modified and standard values when "Topr=85°C while clock is stopped" deleted
1.00	Jun.01, 2004	-	**M32C/85T (High-reliability version)** added
		All Pages	Words standardized: On-chip oscillator, A/D converter and D/A converter
			Overview
		1	• **1.1 Applications** Automobiles added
		2, 3	• **Table 1.1** and **Table 1.2 M32C/85 Group (M32C/85, M32C/85T) Performance** M32C/85T added; note 3 added
		4	• **Figure 1.1 M32C/85 Group (M32C/85, M32C/85T) Block Diagram** Note 3 added
		5	• **1.4 Product Information** Description modified
			• **Figure 1.2 ROM/RAM Capacity** figure modified
		5, 6	• **Table 1.3 M32C/85 Group** M32C/85T added
		6	• **Figure 1.3 Product Numbering System** M32C/85T added
		7	• **Figure 1.4 Pin Assignment for 144-Pin Package** Note 3 added
		12	• **Figure 1.6 Pin Assignment for 100-Pin Pacakage** Note 5 added
		8 to 10	• **Table 1.5 Pin Characteristics for 144-Pin Package** Note 1 added
		13, 14	• **Table 1.6 Pin Characteristics for 100-Pin Package** Note 1 added
		15 to 18	• **Table 1.7 Pin Description** Notes added
			Memory
		22	• **Figure 3.1 Memory Map** Tables of internal ROM/internal RAM modified; note 2 modified; notes 4 and 5 added
			SFR
		23	• Note 2 added
		24	• PWCR0 and PWCR1 registers deleted
			• "Values after RESET" of the masked ROM version added to the FMR0 register
			• Note 1 added
			Electrical Characteristics
		46	• **Table 5.2 Recommended Operating Conditions** $f_{(ripple)}$, $V_{p-p(ripple)}$, V_{CC}, SV_{CC} and note 1 deleted
		47	• **Table 5.3 Electrical Characteristics** R_{PULLUP} value for the masked ROM version added

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