Renesas Electronics America Inc - M30855FWGP#U5 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	M32C/80
Core Size	16/32-Bit
Speed	32MHz
Connectivity	CANbus, I²C, IEBus, SIO, UART/USART
Peripherals	DMA, WDT
Number of I/O	121
Program Memory Size	320KB (320K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 34x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LFQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m30855fwgp-u5

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1.2 Performance Overview

Tables 1.1 and 1.2 list performance overview of the M32C/85 group (M32C/85, M32C/85T).

Table 1.1 M32C/85 Group (M32C/85, M32C/85T) Performance (144-Pin Package)

Characteristic		Performance	
		M32C/85	M32C/85T
CPU	Basic Instructions	108 instructions	
	Minimum Instruction Execution Time	31.3 ns (f(BCLK)=32 MHz, V_{CC1}=4.2 V to 5.5 V) 41.7 ns (f(BCLK)=24 MHz, V_{CC1}=3.0 V to 5.5 V)	31.3 ns (f(BCLK)=32 MHz, V_{CC1}=4.2 V to 5.5 V)
	Operating Mode	Single-chip mode, Memory expansion mode and Microprocessor mode	Single-chip mode
	Address Space	16 Mbytes	
	Memory Capacity	See Table 1.3	
Peripheral Function	I/O Port	123 I/O pins and 1 input pin	
	Multifunction Timer	Timer A: 16 bits x 5 channels, Timer B: 16 bits x 6 channels Three-phase motor control circuit	
	Intelligent I/O	Time measurement function or Waveform generating function: 16 bits x 8 channels Communication function (Clock synchronous serial I/O, Clock asynchronous serial I/O, HDLC data processing)	
	Serial I/O	5 Channels Clock synchronous serial I/O, Clock asynchronous serial I/O, IEBus(1), I^2C bus(2)	
	CAN Module	2 channels Supporting CAN 2.0B specification	
	A/D Converter	10-bit A/D converter: 1 circuit, 34 channels	
	D/A Converter	8 bits x 2 channels	
	DMAC	4 channels	
	DMAC II	Can be activated by all peripheral function interrupt sources Immediate transfer, Calculation transfer and Chain transfer functions	
	CRC Calculation Circuit	CRC-CCITT	
	X/Y Converter	16 bits x 16 bits	
	Watchdog Timer	15 bits x 1 channel (with prescaler)	
	Interrupt	39 internal and 8 external sources, 5 software sources Interrupt priority level: 7	
	Clock Generation Circuit	4 circuits Main clock oscillation circuit(*), Sub clock oscillation circuit(*), On-chip oscillator, PLL frequency synthesizer (*)Equipped with a built-in feedback resistor. Ceramic resonator or crystal oscillator must be connected externally	
	Oscillation Stop Detect Function	Main clock oscillation stop detect function	
	Voltage Detection Circuit	Available (optional)	Not available(4)
Electrical Characteristics	Supply Voltage	V_{CC1}=4.2 V to 5.5 V, V_{CC2}=3.0 V to V_{CC1} (f(BCLK)=32 MHz) V_{CC1}=3.0 V to 5.5 V, V_{CC2}=3.0 V to V_{CC1} (f(BCLK)=24 MHz)	V_{CC1}=V_{CC2}=4.2 V to 5.5 V, (f(BCLK)=32 MHz)(3)
	Power Consumption	28 mA (V_{CC1}=V_{CC2}=5 V, f(BCLK)=32 MHz) 22 mA (V_{CC1}=V_{CC2}=3.3 V, f(BCLK)=24 MHz) 10µA (V_{CC1}=V_{CC2}=5 V, f(BCLK)=32 kHz, in wait mode)	28 mA (V_{CC1}=V_{CC2}=5 V, f(BCLK)=32 MHz) 10µA (V_{CC1}=V_{CC2}=5 V, f(BCLK)=32 kHz, in wait mode)
Flash Memory	Program/Erase Supply Voltage	3.3 V ± 0.3 V or 5.0 V ± 0.5 V	5.0 V ± 0.5 V
	Program and Erase Endurance	100 times (all space)	
Operating Ambient Temperature		–20 to 85°C –40 to 85°C (optional)	–40 to 85°C (T version)
Package		144-pin plastic molded LQFP	

NOTES:
1. IEBus is a trademark of NEC Electronics Corporation.
2. I^2C bus is a trademark of Koninklijke Philips Electronics N. V.
3. The supply voltage of M32C/85T (High-reliability version) must be V_{CC1}=V_{CC2}.
4. The cold start-up/warm start-up determine function is available only at the user's option.

All options are on a request basis.

Table 1.2 M32C/85 Group (M32C/85, M32C/85T) Performance (100-Pin Package)

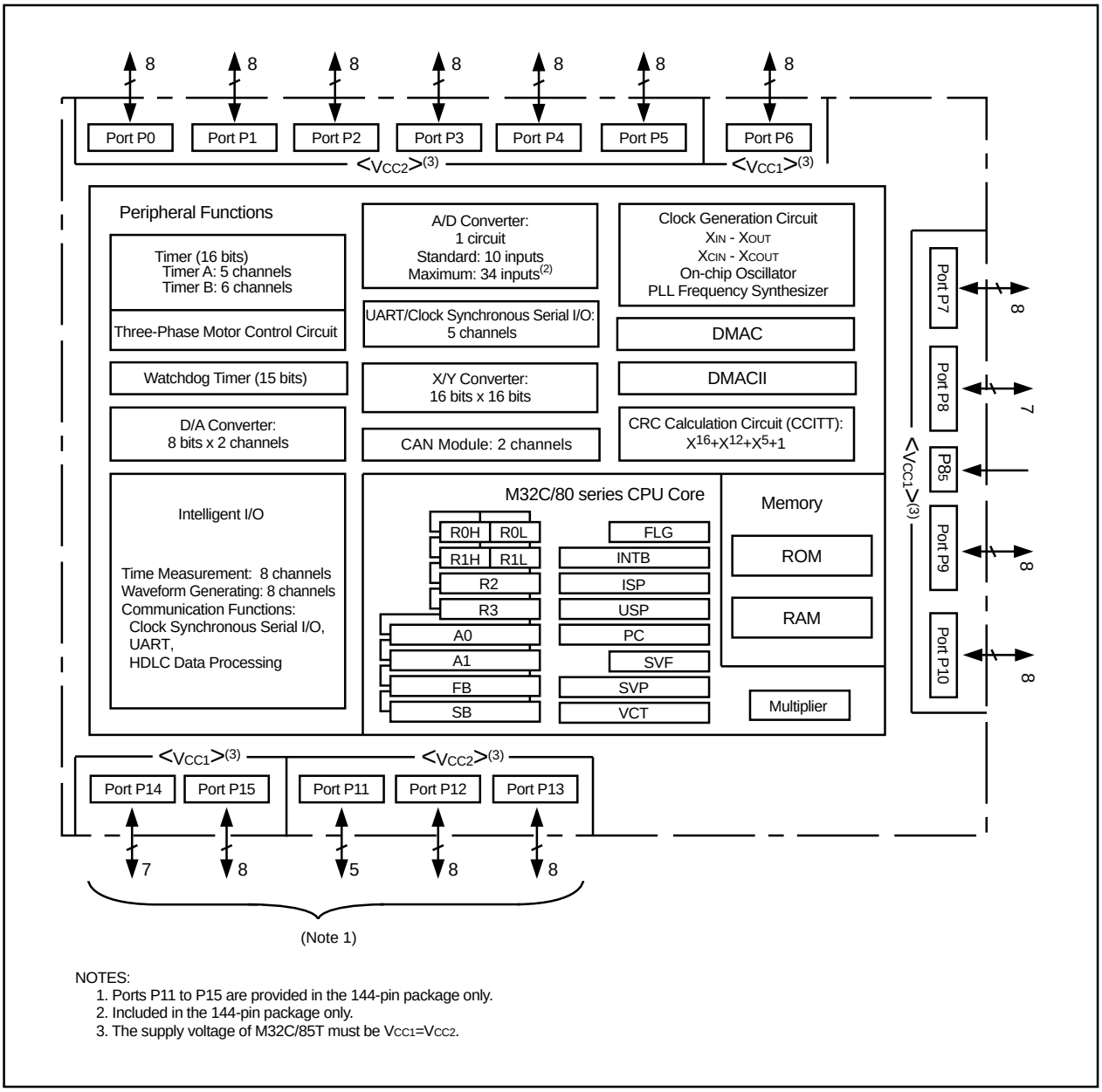
Characteristic		Performance	
		M32C/85	M32C/85T
CPU	Basic Instructions	108 instructions	
	Minimum Instruction Execution Time	31.3 ns (f(BCLK)=32 MHz, V_{CC1}=4.2 V to 5.5 V) 41.7 ns (f(BCLK)=24 MHz, V_{CC1}=3.0 V to 5.5 V)	31.3 ns (f(BCLK)=32 MHz, V_{CC1}=4.2 V to 5.5 V)
	Operating Mode	Single-chip mode, Memory expansion mode and Microprocessor mode	Single-chip mode
	Address Space	16 Mbytes	
	Memory Capacity	See Table 1.3	
Peripheral Function	I/O Port	87 I/O pins and 1 input pin	
	Multifunction Timer	Timer A: 16 bits x 5 channels, Timer B: 16 bits x 6 channels Three-phase motor control circuit	
	Intelligent I/O	Time measurement function or Waveform generating function: 16 bits x 8 channels Communication function (Clock synchronous serial I/O, Clock asynchronous serial I/O, HDLC data processing)	
	Serial I/O	5 Channels Clock synchronous serial I/O, Clock asynchronous serial I/O, IEBus(1), I^2C bus(2)	
	CAN Module	2 channels Supporting CAN 2.0B specification	
	A/D Converter	10-bit A/D converter: 1 circuit, 26 channels	
	D/A Converter	8 bits x 2 channels	
	DMAC	4 channels	
	DMAC II	Can be activated by all peripheral function interrupt sources Immediate transfer, Calculation transfer and Chain transfer functions	
	CRC Calculation Circuit	CRC-CCITT	
	X/Y Converter	16 bits x 16 bits	
	Watchdog Timer	15 bits x 1 channel (with prescaler)	
	Interrupt	39 internal and 8 external sources, 5 software sources Interrupt priority level: 7	
	Clock Generation Circuit	4 circuits Main clock oscillation circuit(*), Sub clock oscillation circuit(*), On-chip oscillator, PLL frequency synthesizer (*)Equipped with a built-in feedback resistor. Ceramic resonator or crystal oscillator must be connected externally	
	Oscillation Stop Detect Function	Main clock oscillation stop detect function	
	Voltage Detection Circuit	Available (optional)	Not available(4)
Electrical Characteristics	Supply Voltage	V_{CC1}=4.2 V to 5.5 V, V_{CC2}=3.0 V to V_{CC1} (f(BCLK)=32 MHz) V_{CC1}=3.0 V to 5.5 V, V_{CC2}=3.0 V to V_{CC1} (f(BCLK)=24 MHz)	V_{CC1}=V_{CC2}=4.2 V to 5.5 V, (f(BCLK)=32 MHz)(3)
	Power Consumption	28 mA (V_{CC1}=V_{CC2}=5 V, f(BCLK)=32 MHz) 22 mA (V_{CC1}=V_{CC2}=3.3 V, f(BCLK)=24 MHz) 10µA (V_{CC1}=V_{CC2}=5 V, f(BCLK)=32 kHz, in wait mode)	28 mA (V_{CC1}=V_{CC2}=5 V, f(BCLK)=32 MHz) 10µA (V_{CC1}=V_{CC2}=5 V, f(BCLK)=32 kHz, in wait mode)
Flash Memory	Program/Erase Supply Voltage	3.3 V ± 0.3 V or 5.0 V ± 0.5 V	5.0 V ± 0.5 V
	Program and Erase Endurance	100 times (all space)	
Operating Ambient Temperature		–20 to 85°C –40 to 85°C (optional)	–40 to 85°C (T version)
Package		100-pin plastic molded LQFP/QFP	

NOTES:
1. IEBus is a trademark of NEC Electronics Corporation.
2. I^2C bus is a trademark of Koninklijke Philips Electronics N. V.
3. The supply voltage of M32C/85T (High-reliability version) must be V_{CC1}=V_{CC2}.
4. The cold start-up/warm start-up determine function is available only at the user's option.

All options are on a request basis.

1.3 Block Diagram

Figure 1.1 shows a block diagram of the M32C/85 group (M32C/85, M32C/85T) microcomputer.



NOTES:
1. Ports P11 to P15 are provided in the 144-pin package only.
2. Included in the 144-pin package only.
3. The supply voltage of M32C/85T must be V_{CC1}=V_{CC2}.

Figure 1.1 M32C/85 Group (M32C/85, M32C/85T) Block Diagram

1.5 Pin Assignments and Descriptions

Figures 1.3 to 1.5 show pin assignments (top view).

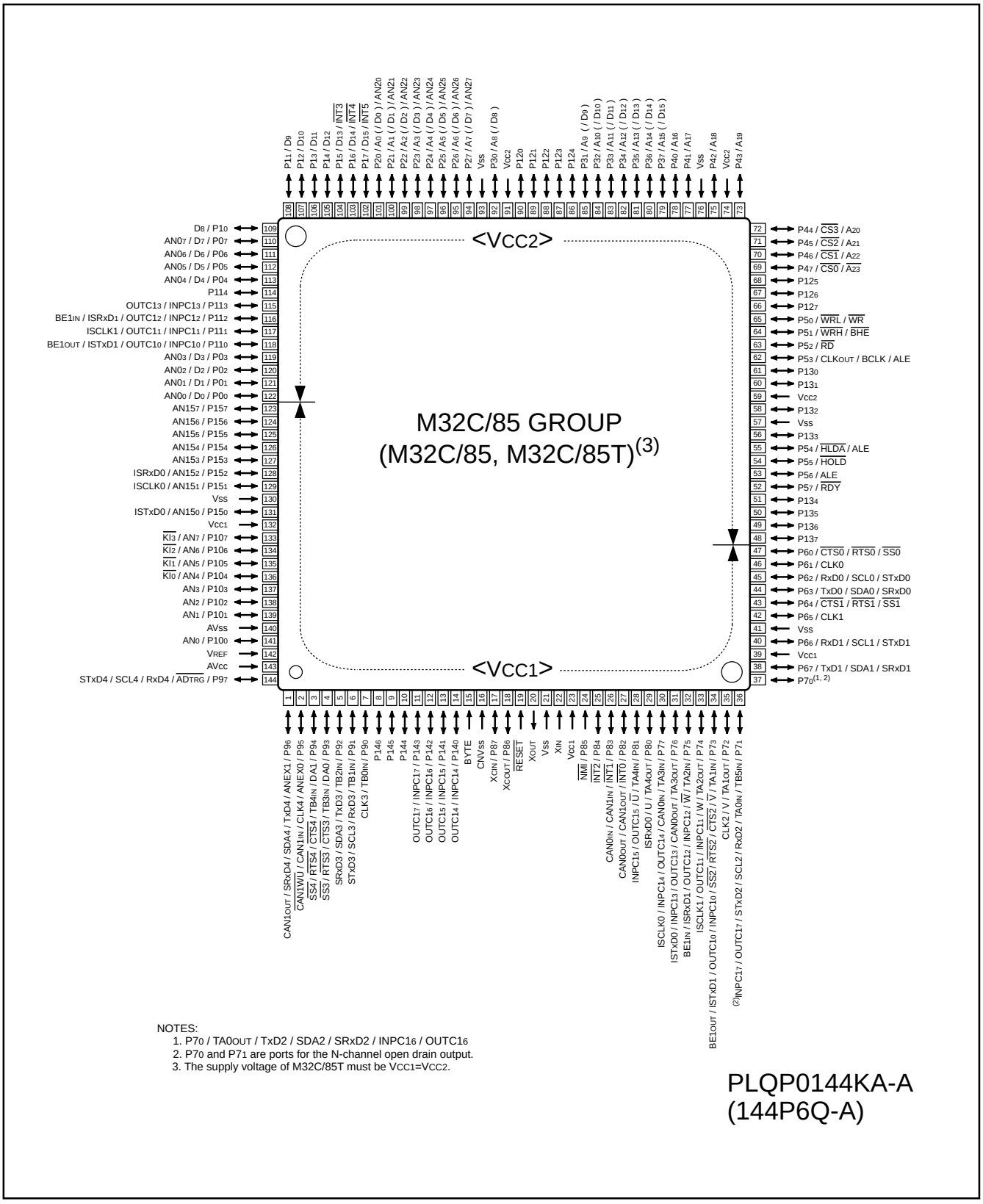


Figure 1.3 Pin Assignment for 144-Pin Package

Table 1.4 Pin Characteristics for 144-Pin Package (Continued)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin(1)
97		$P2_4$					$AN2_4$	A_4(/D_4)
98		$P2_3$					$AN2_3$	A_3(/D_3)
99		$P2_2$					$AN2_2$	A_2(/D_2)
100		$P2_1$					$AN2_1$	A_1(/D_1)
101		$P2_0$					$AN2_0$	A_0(/D_0)
102		$P1_7$	$\overline{INT5}$					D_{15}
103		$P1_6$	$\overline{INT4}$					D_{14}
104		$P1_5$	$\overline{INT3}$					D_{13}
105		$P1_4$						D_{12}
106		$P1_3$						D_{11}
107		$P1_2$						D_{10}
108		$P1_1$						D_9
109		$P1_0$						D_8
110		$P0_7$					$AN0_7$	D_7
111		$P0_6$					$AN0_6$	D_6
112		$P0_5$					$AN0_5$	D_5
113		$P0_4$					$AN0_4$	D_4
114		$P11_4$						
115		$P11_3$				$INPC1_3$/$OUTC1_3$		
116		$P11_2$				$INPC1_2$/$OUTC1_2$/ISRxD1/$BE1_{IN}$		
117		$P11_1$				$INPC1_1$/$OUTC1_1$/ISCLK1		
118		$P11_0$				$INPC1_0$/$OUTC1_0$/ISTxD1/$BE1_{OUT}$		
119		$P0_3$					$AN0_3$	D_3
120		$P0_2$					$AN0_2$	D_2
121		$P0_1$					$AN0_1$	D_1
122		$P0_0$					$AN0_0$	D_0
123		$P15_7$					$AN15_7$	
124		$P15_6$					$AN15_6$	
125		$P15_5$					$AN15_5$	
126		$P15_4$					$AN15_4$	
127		$P15_3$					$AN15_3$	
128		$P15_2$				ISRxD0	$AN15_2$	
129		$P15_1$				ISCLK0	$AN15_1$	
130	V_{SS}							
131		$P15_0$				ISTxD0	$AN15_0$	
132	V_{CC1}							
133		$P10_7$	$\overline{KI_3}$				AN_7	
134		$P10_6$	$\overline{KI_2}$				AN_6	
135		$P10_5$	$\overline{KI_1}$				AN_5	
136		$P10_4$	$\overline{KI_0}$				AN_4	
137		$P10_3$					AN_3	
138		$P10_2$					AN_2	
139		$P10_1$					AN_1	
140	AV_{SS}							
141		$P10_0$					AN_0	
142	V_{REF}							
143	AV_{CC}							
144		$P9_7$			RxD4/SCL4/STxD4		$\overline{ADTRG}$	

NOTES:

1. Bus control pins in M32C/85T cannot be used,

2.1 General Registers

2.1.1 Data Registers (R0, R1, R2 and R3)

R0, R1, R2 and R3 are 16-bit registers for transfer, arithmetic and logic operations. R0 and R1 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R0 can be combined with R2 to be used as a 32-bit data register (R2R0). The same applies to R1 and R3.

2.1.2 Address Registers (A0 and A1)

A0 and A1 are 24-bit registers for A0-/A1-indirect addressing, A0-/A1-relative addressing, transfer, arithmetic and logic operations.

2.1.3 Static Base Register (SB)

SB is a 24-bit register for SB-relative addressing.

2.1.4 Frame Base Register (FB)

FB is a 24-bit register for FB-relative addressing.

2.1.5 Program Counter (PC)

PC, 24 bits wide, indicates the address of an instruction to be executed.

2.1.6 Interrupt Table Register (INTB)

INTB is a 24-bit register indicating the starting address of an relocatable interrupt vector table.

2.1.7 User Stack Pointer (USP), Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP and ISP, are 24 bits wide each. The U flag is used to switch between USP and ISP. Refer to **2.1.8 Flag Register (FLG)** for details on the U flag. Set USP and ISP to even addresses to execute an interrupt sequence efficiently.

2.1.8 Flag Register (FLG)

FLG is a 16-bit register indicating a CPU state.

2.1.8.1 Carry Flag (C)

The C flag indicates whether carry or borrow has occurred after executing an instruction.

2.1.8.2 Debug Flag (D)

The D flag is for debug only. Set to "0".

2.1.8.3 Zero Flag (Z)

The Z flag is set to "1" when the value of zero is obtained from an arithmetic operation; otherwise "0".

2.1.8.4 Sign Flag (S)

The S flag is set to "1" when a negative value is obtained from an arithmetic operation; otherwise "0".

Address	Register	Symbol	Value after RESET
006016			
006116			
006216			
006316			
006416			
006516			
006616			
006716			
006816	DMA0 Interrupt Control Register	DM0IC	XXXX X0002
006916	Timer B5 Interrupt Control Register	TB5IC	XXXX X0002
006A16	DMA2 Interrupt Control Register	DM2IC	XXXX X0002
006B16	UART2 Receive /ACK Interrupt Control Register	S2RIC	XXXX X0002
006C16	Timer A0 Interrupt Control Register	TA0IC	XXXX X0002
006D16	UART3 Receive /ACK Interrupt Control Register	S3RIC	XXXX X0002
006E16	Timer A2 Interrupt Control Register	TA2IC	XXXX X0002
006F16	UART4 Receive /ACK Interrupt Control Register	S4RIC	XXXX X0002
007016	Timer A4 Interrupt Control Register	TA4IC	XXXX X0002
007116	UART0/UART3 Bus Conflict Detect Interrupt Control Register	BCN0IC/BCN3IC	XXXX X0002
007216	UART0 Receive/ACK Interrupt Control Register	S0RIC	XXXX X0002
007316	A/D0 Conversion Interrupt Control Register	AD0IC	XXXX X0002
007416	UART1 Receive/ACK Interrupt Control Register	S1RIC	XXXX X0002
007516	Intelligent I/O Interrupt Control Register 0/ CAN Interrupt 3 Control Register	IIO0IC/ CAN3IC	XXXX X0002
007616	Timer B1 Interrupt Control Register	TB1IC	XXXX X0002
007716	Intelligent I/O Interrupt Control Register 2	IIO2IC	XXXX X0002
007816	Timer B3 Interrupt Control Register	TB3IC	XXXX X0002
007916	Intelligent I/O Interrupt Control Register 4	IIO4IC	XXXX X0002
007A16	INT5 Interrupt Control Register	INT5IC	XX00 X0002
007B16			
007C16	INT3 Interrupt Control Register	INT3IC	XX00 X0002
007D16	Intelligent I/O Interrupt Control Register 8	IIO8IC	XXXX X0002
007E16	INT1 Interrupt Control Register	INT1IC	XX00 X0002
007F16	Intelligent I/O Interrupt Control Register 10/ CAN Interrupt 1 Control Register	IIO10IC/ CAN1IC	XXXX X0002
008016			
008116	CAN Interrupt 2 Control Register	CAN2IC	XXXX X0002
008216			
008316			
008416			
008516			
008616			
008716			
008816	DMA1 Interrupt Control Register	DM1IC	XXXX X0002
008916	UART2 Transmit /NACK Interrupt Control Register	S2TIC	XXXX X0002
008A16	DMA3 Interrupt Control Register	DM3IC	XXXX X0002
008B16	UART3 Transmit /NACK Interrupt Control Register	S3TIC	XXXX X0002
008C16	Timer A1 Interrupt Control Register	TA1IC	XXXX X0002
008D16	UART4 Transmit /NACK Interrupt Control Register	S4TIC	XXXX X0002
008E16	Timer A3 Interrupt Control Register	TA3IC	XXXX X0002
008F16	UART2 Bus Conflict Detect Interrupt Control Register	BCN2IC	XXXX X0002

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
00F016	Data Compare Register 00	G0CMP0	XX16
00F116	Data Compare Register 01	G0CMP1	XX16
00F216	Data Compare Register 02	G0CMP2	XX16
00F316	Data Compare Register 03	G0CMP3	XX16
00F416	Data Mask Register 00	G0MSK0	XX16
00F516	Data Mask Register 01	G0MSK1	XX16
00F616	Communication Clock Select Register	CCS	XXXX 00002
00F716			
00F816	Receive CRC Code Register 0	G0RCRC	XX16
00F916			XX16
00FA16	Transmit CRC Code Register 0	G0TCRC	0016
00FB16			0016
00FC16	SI/O Extended Mode Register 0	G0EMR	0016
00FD16	SI/O Extended Receive Control Register 0	G0ERC	0016
00FE16	SI/O Special Communication Interrupt Detect Register 0	G0IRF	0016
00FF16	SI/O Extended Transmit Control Register 0	G0ETC	0000 0XXX2
010016	Time Measurement/Waveform Generating Register 10	G1TM0/G1PO0	XX16
010116			XX16
010216	Time Measurement/Waveform Generating Register 11	G1TM1/G1PO1	XX16
010316			XX16
010416	Time Measurement/Waveform Generating Register 12	G1TM2/G1PO2	XX16
010516			XX16
010616	Time Measurement/Waveform Generating Register 13	G1TM3/G1PO3	XX16
010716			XX16
010816	Time Measurement/Waveform Generating Register 14	G1TM4/G1PO4	XX16
010916			XX16
010A16	Time Measurement/Waveform Generating Register 15	G1TM5/G1PO5	XX16
010B16			XX16
010C16	Time Measurement/Waveform Generating Register 16	G1TM6/G1PO6	XX16
010D16			XX16
010E16	Time Measurement/Waveform Generating Register 17	G1TM7/G1PO7	XX16
010F16			XX16
011016	Waveform Generating Control Register 10	G1POCR0	0000 X0002
011116	Waveform Generating Control Register 11	G1POCR1	0X00 X0002
011216	Waveform Generating Control Register 12	G1POCR2	0X00 X0002
011316	Waveform Generating Control Register 13	G1POCR3	0X00 X0002
011416	Waveform Generating Control Register 14	G1POCR4	0X00 X0002
011516	Waveform Generating Control Register 15	G1POCR5	0X00 X0002
011616	Waveform Generating Control Register 16	G1POCR6	0X00 X0002
011716	Waveform Generating Control Register 17	G1POCR7	0X00 X0002
011816	Time Measurement Control Register 10	G1TMCR0	0016
011916	Time Measurement Control Register 11	G1TMCR1	0016
011A16	Time Measurement Control Register 12	G1TMCR2	0016
011B16	Time Measurement Control Register 13	G1TMCR3	0016
011C16	Time Measurement Control Register 14	G1TMCR4	0016
011D16	Time Measurement Control Register 15	G1TMCR5	0016
011E16	Time Measurement Control Register 16	G1TMCR6	0016
011F16	Time Measurement Control Register 17	G1TMCR7	0016

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
01E0₁₆	CAN0 Message Slot Buffer 0 Standard ID0	C0SLOT0_0	XX₁₆
01E1₁₆	CAN0 Message Slot Buffer 0 Standard ID1	C0SLOT0_1	XX₁₆
01E2₁₆	CAN0 Message Slot Buffer 0 Extended ID0	C0SLOT0_2	XX₁₆
01E3₁₆	CAN0 Message Slot Buffer 0 Extended ID1	C0SLOT0_3	XX₁₆
01E4₁₆	CAN0 Message Slot Buffer 0 Extended ID2	C0SLOT0_4	XX₁₆
01E5₁₆	CAN0 Message Slot Buffer 0 Data Length Code	C0SLOT0_5	XX₁₆
01E6₁₆	CAN0 Message Slot Buffer 0 Data 0	C0SLOT0_6	XX₁₆
01E7₁₆	CAN0 Message Slot Buffer 0 Data 1	C0SLOT0_7	XX₁₆
01E8₁₆	CAN0 Message Slot Buffer 0 Data 2	C0SLOT0_8	XX₁₆
01E9₁₆	CAN0 Message Slot Buffer 0 Data 3	C0SLOT0_9	XX₁₆
01EA₁₆	CAN0 Message Slot Buffer 0 Data 4	C0SLOT0_10	XX₁₆
01EB₁₆	CAN0 Message Slot Buffer 0 Data 5	C0SLOT0_11	XX₁₆
01EC₁₆	CAN0 Message Slot Buffer 0 Data 6	C0SLOT0_12	XX₁₆
01ED₁₆	CAN0 Message Slot Buffer 0 Data 7	C0SLOT0_13	XX₁₆
01EE₁₆	CAN0 Message Slot Buffer 0 Time Stamp High-Order	C0SLOT0_14	XX₁₆
01EF₁₆	CAN0 Message Slot Buffer 0 Time Stamp Low-Order	C0SLOT0_15	XX₁₆
01F0₁₆	CAN0 Message Slot Buffer 1 Standard ID0	C0SLOT1_0	XX₁₆
01F1₁₆	CAN0 Message Slot Buffer 1 Standard ID1	C0SLOT1_1	XX₁₆
01F2₁₆	CAN0 Message Slot Buffer 1 Extended ID0	C0SLOT1_2	XX₁₆
01F3₁₆	CAN0 Message Slot Buffer 1 Extended ID1	C0SLOT1_3	XX₁₆
01F4₁₆	CAN0 Message Slot Buffer 1 Extended ID2	C0SLOT1_4	XX₁₆
01F5₁₆	CAN0 Message Slot Buffer 1 Data Length Code	C0SLOT1_5	XX₁₆
01F6₁₆	CAN0 Message Slot Buffer 1 Data 0	C0SLOT1_6	XX₁₆
01F7₁₆	CAN0 Message Slot Buffer 1 Data 1	C0SLOT1_7	XX₁₆
01F8₁₆	CAN0 Message Slot Buffer 1 Data 2	C0SLOT1_8	XX₁₆
01F9₁₆	CAN0 Message Slot Buffer 1 Data 3	C0SLOT1_9	XX₁₆
01FA₁₆	CAN0 Message Slot Buffer 1 Data 4	C0SLOT1_10	XX₁₆
01FB₁₆	CAN0 Message Slot Buffer 1 Data 5	C0SLOT1_11	XX₁₆
01FC₁₆	CAN0 Message Slot Buffer 1 Data 6	C0SLOT1_12	XX₁₆
01FD₁₆	CAN0 Message Slot Buffer 1 Data 7	C0SLOT1_13	XX₁₆
01FE₁₆	CAN0 Message Slot Buffer 1 Time Stamp High-Order	C0SLOT1_14	XX₁₆
01FF₁₆	CAN0 Message Slot Buffer 1 Time Stamp Low-Order	C0SLOT1_15	XX₁₆
0200₁₆ 0201₁₆	CAN0 Control Register 0	C0CTLR0	XX01 0X01₂(1) XXXX 0000₂(1)
0202₁₆ 0203₁₆	CAN0 Status Register	C0STR	0000 0000₂(1) X000 0X01₂(1)
0204₁₆ 0205₁₆	CAN0 Extended ID Register	C0IDR	00₁₆(1) 00₁₆(1)
0206₁₆ 0207₁₆	CAN0 Configuration Register	C0CONR	0000 XXXX₂(1) 0000 0000₂(1)
0208₁₆ 0209₁₆	CAN0 Time Stamp Register	C0TSR	00₁₆(1) 00₁₆(1)
020A₁₆	CAN0 Transmit Error Count Register	C0TEC	00₁₆(1)
020B₁₆	CAN0 Receive Error Count Register	C0REC	00₁₆(1)
020C₁₆ 020D₁₆	CAN0 Slot Interrupt Status Register	C0SISTR	00₁₆(1) 00₁₆(1)
020E₁₆			
020F₁₆			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTES:

1. Values are obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) after reset and applying the clock to the CAN module.

Address	Register	Symbol	Value after RESET
0210$_{16}$ 0211$_{16}$	CAN0 Slot Interrupt Mask Register	C0SIMKR	00$_{16}$(2) 00$_{16}$(2)
0212$_{16}$			
0213$_{16}$			
0214$_{16}$	CAN0 Error Interrupt Mask Register	C0EIMKR	XXXX X000$_2$(2)
0215$_{16}$	CAN0 Error Interrupt Status Register	C0EISTR	XXXX X000$_2$(2)
0216$_{16}$	CAN0 Error Cause Register	C0EFR	00$_{16}$(2)
0217$_{16}$	CAN0 Baud Rate Prescaler	C0BRP	0000 0001$_2$(2)
0218$_{16}$			
0219$_{16}$	CAN0 Mode Register	C0MDR	XXXX XX00$_2$(2)
021A$_{16}$			
021B$_{16}$			
021C$_{16}$			
021D$_{16}$			
021E$_{16}$			
021F$_{16}$			
0220$_{16}$ 0221$_{16}$	CAN0 Single Shot Control Register	C0SSCTLR	00$_{16}$(2) 00$_{16}$(2)
0222$_{16}$			
0223$_{16}$			
0224$_{16}$ 0225$_{16}$	CAN0 Single Shot Status Register	C0SSSTR	00$_{16}$(2) 00$_{16}$(2)
0226$_{16}$			
0227$_{16}$			
0228$_{16}$	CAN0 Global Mask Register Standard ID0	C0GMR0	XXX0 0000$_2$(2)
0229$_{16}$	CAN0 Global Mask Register Standard ID1	C0GMR1	XX00 0000$_2$(2)
022A$_{16}$	CAN0 Global Mask Register Extended ID0	C0GMR2	XXXX 0000$_2$(2)
022B$_{16}$	CAN0 Global Mask Register Extended ID1	C0GMR3	00$_{16}$(2)
022C$_{16}$	CAN0 Global Mask Register Extended ID2	C0GMR4	XX00 0000$_2$(2)
022D$_{16}$			
022E$_{16}$			
022F$_{16}$			
0230$_{16}$	CAN0 Message Slot 0 Control Register / CAN0 Local Mask Register A Standard ID0	C0MCTL0/ C0LMAR0	0000 0000$_2$(2) XXX0 0000$_2$(2)
0231$_{16}$	CAN0 Message Slot 1 Control Register / CAN0 Local Mask Register A Standard ID1	C0MCTL1/ C0LMAR1	0000 0000$_2$(2) XX00 0000$_2$(2)
0232$_{16}$	CAN0 Message Slot 2 Control Register / CAN0 Local Mask Register A Extended ID0	C0MCTL2/ C0LMAR2	0000 0000$_2$(2) XXXX 0000$_2$(2)
0233$_{16}$	CAN0 Message Slot 3 Control Register / CAN0 local Mask Register A Extended ID1	C0MCTL3/ C0LMAR3	00$_{16}$(2) 00$_{16}$(2)
0234$_{16}$	CAN0 Message Slot 4 Control Register / CAN0 Local Mask Register A Extended ID2	C0MCTL4/ C0LMAR4	0000 0000$_2$(2) XX00 0000$_2$(2)
0235$_{16}$	CAN0 Message Slot 5 Control Register	C0MCTL5	00$_{16}$(2)
0236$_{16}$	CAN0 Message Slot 6 Control Register	C0MCTL6	00$_{16}$(2)
0237$_{16}$	CAN0 Message Slot 7 Control Register	C0MCTL7	00$_{16}$(2)
0238$_{16}$	CAN0 Message Slot 8 Control Register / CAN0 Local Mask Register B Standard ID0	C0MCTL8/ C0LMBR0	0000 0000$_2$(2) XXX0 0000$_2$(2)
0239$_{16}$	CAN0 Message Slot 9 Control Register / CAN0 Local Mask Register B Standard ID1	C0MCTL9/ C0LMBR1	0000 0000$_2$(2) XX00 0000$_2$(2)

(Note 1)

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTES:

1. The BANKSEL bit in the C0CTLR1 register switches functions for addresses 0220$_{16}$ to 023F$_{16}$.
2. Values are obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) after reset and applying the clock to the CAN module.

Address	Register	Symbol	Value after RESET
02E0₁₆	X/Y Control Register	XYC	XXXX XX00₂
02E1₁₆			
02E2₁₆			
02E3₁₆			
02E4₁₆	UART1 Special Mode Register 4	U1SMR4	00₁₆
02E5₁₆	UART1 Special Mode Register 3	U1SMR3	00₁₆
02E6₁₆	UART1 Special Mode Register 2	U1SMR2	00₁₆
02E7₁₆	UART1 Special Mode Register	U1SMR	00₁₆
02E8₁₆	UART1 Transmit/Receive Mode Register	U1MR	00₁₆
02E9₁₆	UART1 Bit Rate Register	U1BRG	XX₁₆
02EA₁₆	UART1 Transmit Buffer Register	U1TB	XX₁₆
02EB₁₆			XX₁₆
02EC₁₆	UART1 Transmit/Receive Control Register 0	U1C0	0000 1000₂
02ED₁₆	UART1 Transmit/Receive Control Register 1	U1C1	0000 0010₂
02EE₁₆	UART1 Receive Buffer Register	U1RB	XX₁₆
02EF₁₆			XX₁₆
02F0₁₆			
02F1₁₆			
02F2₁₆			
02F3₁₆			
02F4₁₆	UART4 Special Mode Register 4	U4SMR4	00₁₆
02F5₁₆	UART4 Special Mode Register 3	U4SMR3	00₁₆
02F6₁₆	UART4 Special Mode Register 2	U4SMR2	00₁₆
02F7₁₆	UART4 Special Mode Register	U4SMR	00₁₆
02F8₁₆	UART4 Transmit/Receive Mode Register	U4MR	00₁₆
02F9₁₆	UART4 Bit Rate Register	U4BRG	XX₁₆
02FA₁₆	UART4 Transmit Buffer Register	U4TB	XX₁₆
02FB₁₆			XX₁₆
02FC₁₆	UART4 Transmit/Receive Control Register 0	U4C0	0000 1000₂
02FD₁₆	UART4 Transmit/Receive Control Register 1	U4C1	0000 0010₂
02FE₁₆	UART4 Receive Buffer Register	U4RB	XX₁₆
02FF₁₆			XX₁₆
0300₁₆	Timer B3, B4, B5 Count Start Flag	TBSR	000X XXXX₂
0301₁₆			
0302₁₆	Timer A1-1 Register	TA11	XX₁₆
0303₁₆			XX₁₆
0304₁₆	Timer A2-1 Register	TA21	XX₁₆
0305₁₆			XX₁₆
0306₁₆	Timer A4-1 Register	TA41	XX₁₆
0307₁₆			XX₁₆
0308₁₆	Three-Phase PWM Control Register 0	INVC0	00₁₆
0309₁₆	Three-Phase PWM Control Register 1	INVC1	00₁₆
030A₁₆	Three-Phase Output Buffer Register 0	IDB0	XX11 1111₂
030B₁₆	Three-Phase Output Buffer Register 1	IDB1	XX11 1111₂
030C₁₆	Dead Time Timer	DTT	XX₁₆
030D₁₆	Timer B2 Interrupt Generation Frequency Set Counter	ICTB2	XX₁₆
030E₁₆			
030F₁₆			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
0310$_{16}$	Timer B3 Register	TB3	XX$_{16}$
0311$_{16}$			XX$_{16}$
0312$_{16}$	Timer B4 Register	TB4	XX$_{16}$
0313$_{16}$			XX$_{16}$
0314$_{16}$	Timer B5 Register	TB5	XX$_{16}$
0315$_{16}$			XX$_{16}$
0316$_{16}$			
0317$_{16}$			
0318$_{16}$			
0319$_{16}$			
031A$_{16}$			
031B$_{16}$	Timer B3 Mode Register	TB3MR	00XX 0000$_2$
031C$_{16}$	Timer B4 Mode Register	TB4MR	00XX 0000$_2$
031D$_{16}$	Timer B5 Mode Register	TB5MR	00XX 0000$_2$
031E$_{16}$			
031F$_{16}$	External Interrupt Request Source Select Register	IFSR	00$_{16}$
0320$_{16}$			
0321$_{16}$			
0322$_{16}$			
0323$_{16}$			
0324$_{16}$	UART3 Special Mode Register 4	U3SMR4	00$_{16}$
0325$_{16}$	UART3 Special Mode Register 3	U3SMR3	00$_{16}$
0326$_{16}$	UART3 Special Mode Register 2	U3SMR2	00$_{16}$
0327$_{16}$	UART3 Special Mode Register	U3SMR	00$_{16}$
0328$_{16}$	UART3 Transmit/Receive Mode Register	U3MR	00$_{16}$
0329$_{16}$	UART3 Bit Rate Register	U3BRG	XX$_{16}$
032A$_{16}$	UART3 Transmit Buffer Register	U3TB	XX$_{16}$
032B$_{16}$			XX$_{16}$
032C$_{16}$	UART3 Transmit/Receive Control Register 0	U3C0	0000 1000$_2$
032D$_{16}$	UART3 Transmit/Receive Control Register 1	U3C1	0000 0010$_2$
032E$_{16}$	UART3 Receive Buffer Register	U3RB	XX$_{16}$
032F$_{16}$			XX$_{16}$
0330$_{16}$			
0331$_{16}$			
0332$_{16}$			
0333$_{16}$			
0334$_{16}$	UART2 Special Mode Register 4	U2SMR4	00$_{16}$
0335$_{16}$	UART2 Special Mode Register 3	U2SMR3	00$_{16}$
0336$_{16}$	UART2 Special Mode Register 2	U2SMR2	00$_{16}$
0337$_{16}$	UART2 Special Mode Register	U2SMR	00$_{16}$
0338$_{16}$	UART2 Transmit/Receive Mode Register	U2MR	00$_{16}$
0339$_{16}$	UART2 Bit Rate Register	U2BRG	XX$_{16}$
033A$_{16}$	UART2 Transmit Buffer Register	U2TB	XX$_{16}$
033B$_{16}$			XX$_{16}$
033C$_{16}$	UART2 Transmit/Receive Control Register 0	U2C0	0000 1000$_2$
033D$_{16}$	UART2 Transmit/Receive Control Register 1	U2C1	0000 0010$_2$
033E$_{16}$	UART2 Receive Buffer Register	U2RB	XX$_{16}$
033F$_{16}$			XX$_{16}$

X: Indeterminate

Blank spaces are reserved. No access is allowed.

$V_{CC1}=V_{CC2}=5V$

Table 5.3 Electrical Characteristics (Continued)

($V_{CC1}=V_{CC2}=4.2$ to 5.5V, $V_{SS}=0V$ at Topr= –20 to 85°C, f(BCLK)=32MHz unless otherwise specified)

Symbol	Parameter	Measurement Condition		Standard			Unit
				Min.	Typ.	Max.	
I_{CC}	Power Supply Current	In single-chip mode, output pins are left open and other pins are connected to V_{SS}.	f(BCLK)=32 MHz, Square wave, No division		28	45	mA
			f(BCLK)=32 kHz, In low-power consumption mode, Program running on ROM — Flash Memory		430		µA
			f(BCLK)=32 kHz, In low-power consumption mode, Program running on ROM — Masked ROM		25		µA
			f(BCLK)=32 kHz, In low-power consumption mode, Program running on RAM(1)		25		µA
			f(BCLK)=32 kHz, In wait mode, Topr=25° C		10		µA
			While clock stops, Topr=25° C		0.8	5	µA
			While clock stops, Topr=85° C			50	µA

NOTES:

1. Value is obtained when setting the FMSTP bit in the FMR0 register to "1" (flash memory stopped).

$V_{CC1}=V_{CC2}=5V$

Table 5.4 A/D Conversion Characteristics ($V_{CC1}=V_{CC2}=AV_{CC}=V_{REF}$=4.2 to 5.5V, V_{SS}= AV_{SS} = 0V at Topr=–20 to 85°C, f(BCLK) = 32MHz unless otherwise specified)

Symbol	Parameter	Measurement Condition		Standard			Unit
				Min.	Typ.	Max.	
-	Resolution	$V_{REF}=V_{CC1}$				10	Bits
INL	Integral Nonlinearity Error	$V_{REF}=V_{CC1}=V_{CC2}$=5V	AN_0 to AN_7, $AN0_0$ to $AN0_7$, $AN2_0$ to $AN2_7$, $AN15_0$ to $AN15_7$, ANEX0, ANEX1			±3	LSB
							LSB
			External op-amp connection mode			±7	LSB
							LSB
DNL	Differential Nonlinearity Error					±1	LSB
-	Offset Error					±3	LSB
-	Gain Error					±3	LSB
R_{LADDER}	Resistor Ladder	$V_{REF}=V_{CC1}$		8		40	kΩ
t_{CONV}	10-bit Conversion Time(1, 2)			2.06			µs
t_{CONV}	8-bit Conversion Time(1, 2)			1.75			µs
t_{SAMP}	Sampling Time(1)			0.188			µs
V_{REF}	Reference Voltage			2		V_{CC1}	V
V_{IA}	Analog Input Voltage			0		V_{REF}	V

NOTES:
1. Divide f(X_{IN}), if exceeding 16 MHz, to keep ϕAD frequency at 16 MHz or less.
2. With using the sample and hold function.

Table 5.5 D/A Conversion Characteristics ($V_{CC1}=V_{CC2}=V_{REF}$=4.2 to 5.5V, $V_{SS}=AV_{SS}$=0V at Topr=–20 to 85°C, f(BCLK) = 32MHz unless otherwise specified)

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min.	Typ.	Max.	
-	Resolution				8	Bits
-	Absolute Accuracy				1.0	%
t_{SU}	Setup Time				3	µs
R_O	Output Resistance		4	10	20	kΩ
I_{VREF}	Reference Power Supply Input Current	(Note 1)			1.5	mA

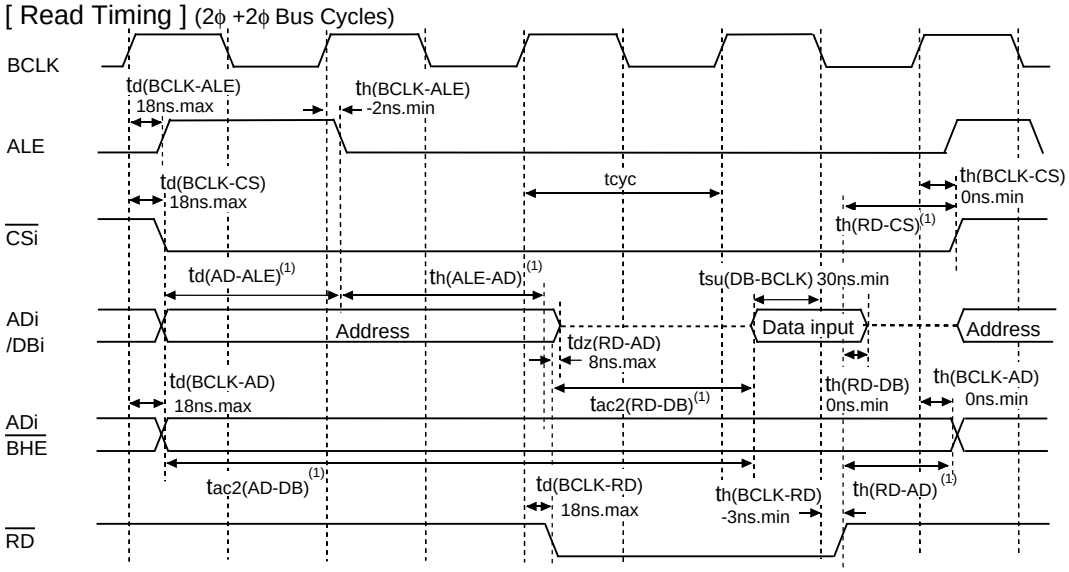
NOTES:
1. Measurement when using one D/A converter. The DAi register (i=0, 1) of the D/A converter, not being used, is set to "00_{16}". The resistor ladder in the A/D converter is excluded.
I_{VREF} flows even if the VCUT bit in the AD0CON1 register is set to "0" (no V_{REF} connection).

Memory Expansion Mode and Microprocessor Mode

Vcc1=Vcc2=3.3V

(when accessing external memory space and using the multiplexed bus)

[Read Timing] (2ϕ +2ϕ Bus Cycles)



NOTES:

1. Varies with operation frequency:

$t_{d(AD-ALE)}$=(tcyc/2 x n-20)ns.min (if external bus cycle is aϕ + bϕ, n=a)

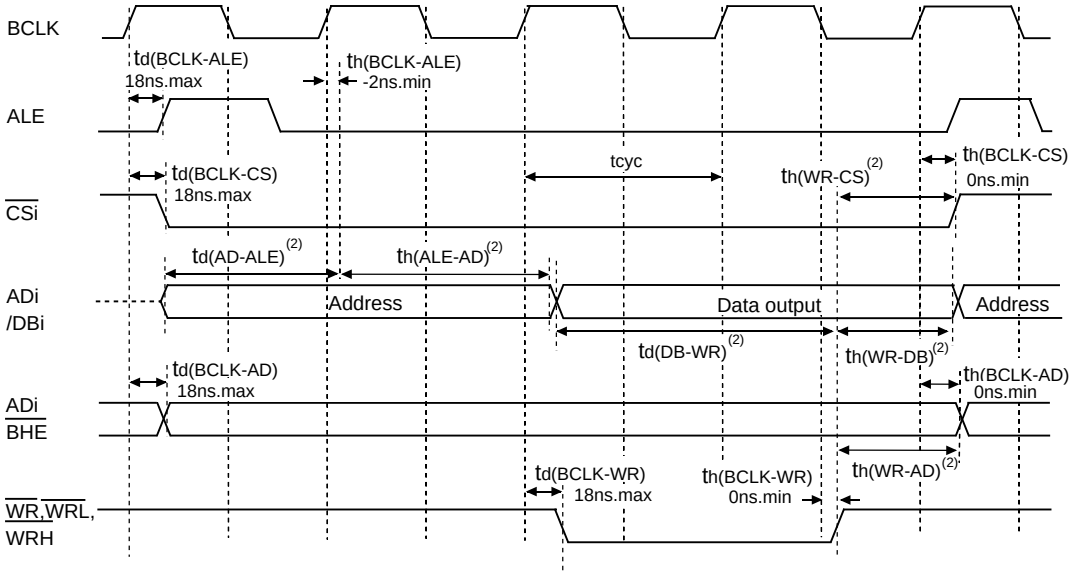
$t_{h(ALE-AD)}$=(tcyc/2 x n-10)ns.min (if external bus cycle is aϕ + bϕ, n=a)

$t_{h(RD-AD)}$=(tcyc/2-10)ns.min, $t_{h(RD-CS)}$=(tcyc/2-10)ns.min

$t_{ac2(RD-DB)}$=(tcyc/2 x m-35)ns.max (if external bus cycle is aϕ + bϕ, m=(b x 2)-1)

$t_{ac2(AD-DB)}$=(tcyc/2 x p-35)ns.max (if external bus cycle is aϕ + bϕ, p={(a+b-1) x 2}+1)

[Write Timing] (2ϕ +2ϕ Bus Cycles)



NOTES:

2. Varies with operation frequency:

$t_{d(AD-ALE)}$=(tcyc/2 x n - 20)ns.min

(if external bus cycle is aϕ + bϕ, n=a)

$t_{h(ALE-AD)}$=(tcyc/2 x n -10)ns.min

(if external bus cycle is aϕ + bϕ, n=a)

$t_{h(WR-AD)}$=(tcyc/2-10)ns.min,

$t_{h(WR-CS)}$=(tcyc/2-10)ns.min, $t_{h(WR-DB)}$=(tcyc/2-20)ns.min

$t_{d(DB-WR)}$=(tcyc/2 x m-25)ns.min

(if external bus cycle is aϕ + bϕ, m=(b x 2)-1)

Measurement Conditions:

- V_{CC1}=V_{CC2}=3.0 to 3.6V
- Input high and low voltage:
  V_{IH}=1.5V, V_{IL}=0.5V
- Output high and low voltage:
  V_{OH}=1.5V, V_{OL}=1.5V

$$tcyc = \frac{10^9}{f_{(BCLK)}}$$

Figure 5.8 V_{CC1}=V_{CC2}=3.3V Timing Diagram (2)

Table 5.43 Recommended Operating Conditions

(V_{CC1}=V_{CC2}=4.2 to 5.5V, V_{SS}=0V at Topr = -40 to 85°C (T version) unless otherwise specified)

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
V_{CC1}, V_{CC2}	Supply Voltage (V_{CC1}≥ V_{CC2})		4.2	5.0	5.5	V
AVcc	Analog Supply Voltage			V_{CC1}		V
Vss	Supply Voltage			0		V
AVss	Analog Supply Voltage			0		V
V_{IH}	Input High ("H") Voltage	$P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$(4)	0.8V_{CC2}		V_{CC2}	V
		$P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_7$(3), $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(4), X_{IN}, $\overline{RESET}$, CNVss, BYTE	0.8V_{CC1}		V_{CC1}	
		$P7_0$, $P7_1$	0.8V_{CC1}		6.0	
		$P0_0$-$P0_7$, $P1_0$-$P1_7$	0.8V_{CC2}		V_{CC2}	
V_{IL}	Input Low ("L") Voltage	$P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$(4)	0		0.2V_{CC2}	V
		$P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_7$(3), $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(4), X_{IN}, $\overline{RESET}$, CNVss, BYTE	0		0.2V_{CC1}	
		$P0_0$-$P0_7$, $P1_0$-$P1_7$	0		0.2V_{CC2}	
$I_{OH(peak)}$	Peak Output High ("H") Current(2)	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(4)			-10.0	mA
$I_{OH(avg)}$	Average Output High ("H") Current(1)	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(4)			-5.0	mA
$I_{OL(peak)}$	Peak Output Low ("L") Current(2)	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(4)			10.0	mA
$I_{OL(avg)}$	Average Output Low ("L") Current(1)	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, $P11_0$-$P11_4$, $P12_0$-$P12_7$, $P13_0$-$P13_7$, $P14_0$-$P14_6$, $P15_0$-$P15_7$(4)			5.0	mA

NOTES:

1. Typical values when average output current is 100ms.
2. Total $I_{OL(peak)}$ for P0, P1, P2, $P8_6$, $P8_7$, P9, P10, P11, P14 and P15 must be 80mA or less.
   Total $I_{OL(peak)}$ for P3, P4, P5, P6, P7, $P8_0$ to $P8_4$, P12 and P13 must be 80mA or less.
   Total $I_{OH(peak)}$ for P0, P1, P2, and P11 must be -40mA or less.
   Total $I_{OH(peak)}$ for $P8_6$, $P8_7$, P9, P10, P14 and P15 must be -40mA or less.
   Total $I_{OH(peak)}$ for P3, P4, P5, P12 and P13 must be -40mA or less.
   Total $I_{OH(peak)}$ for P6, P7, and $P8_0$ to $P8_4$ must be -40mA or less.
3. V_{IH} and V_{IL} reference for $P8_7$ applies when $P8_7$ is used as a programmable input port.
   It does not apply when $P8_7$ is used as X_{CIN}.
4. P11 to P15 are provided in the 144-pin package only.

$V_{CC1}=V_{CC2}=5V$

Timing Requirements

($V_{CC1}=V_{CC2}=4.2$ to 5.5V, $V_{SS}=0V$ at Topr= -40 to 85°C (T version) unless otherwise specified)

Table 5.49 External Clock Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc	External Clock Input Cycle Time	31.25		ns
$tw_{(H)}$	External Clock Input High ("H") Width	13.75		ns
$tw_{(L)}$	External Clock Input Low ("L") Width	13.75		ns
tr	External Clock Rise Time		5	ns
tf	External Clock Fall Time		5	ns

$V_{CC1}=V_{CC2}=5V$

Timing Requirements

($V_{CC1}=V_{CC2}=4.2$ to 5.5V, $V_{SS}=0V$ at Topr= -40 to 85°C (T version) unless otherwise specified)

Table 5.55 Timer B Input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBi_{IN} Input Cycle Time (counted on one edge)	100		ns
$t_{w(TBH)}$	TBi_{IN} Input High ("H") Width (counted on one edge)	40		ns
$t_{w(TBL)}$	TBi_{IN} Input Low ("L") Width (counted on one edge)	40		ns
$t_{c(TB)}$	TBi_{IN} Input Cycle Time (counted on both edges)	200		ns
$t_{w(TBH)}$	TBi_{IN} Input High ("H") Width (counted on both edges)	80		ns
$t_{w(TBL)}$	TBi_{IN} Input Low ("L") Width (counted on both edges)	80		ns

Table 5.56 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBi_{IN} Input Cycle Time	400		ns
$t_{w(TBH)}$	TBi_{IN} Input High ("H") Width	200		ns
$t_{w(TBL)}$	TBi_{IN} Input Low ("L") Width	200		ns

Table 5.57 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBi_{IN} Input Cycle Time	400		ns
$t_{w(TBH)}$	TBi_{IN} Input High ("H") Width	200		ns
$t_{w(TBL)}$	TBi_{IN} Input Low ("L") Width	200		ns

Table 5.58 A/D Trigger Input

Symbol	Parameter	Standard		Unit
		Min.	Max	
$t_{c(AD)}$	$\overline{ADTRG}$ Input Cycle Time (required for trigger)	1000		ns
$t_{w(ADL)}$	$\overline{ADTRG}$ Input Low ("L") Pulse Width	125		ns

Table 5.59 Serial I/O

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi Input Cycle Time	200		ns
$t_{w(CKH)}$	CLKi Input High ("H") Width	100		ns
$t_{w(CKL)}$	CLKi Input Low ("L") Width	100		ns
$t_{d(C-Q)}$	TxDi Output Delay Time		80	ns
$t_{h(C-Q)}$	TxDi Hold Time	0		ns
$t_{su(D-C)}$	RxDi Input Setup Time	30		ns
$t_{h(C-Q)}$	RxDi Input Hold Time	90		ns

Table 5.60 External Interrupt $\overline{INTi}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ Input High ("H") Width	250		ns
$t_{w(INL)}$	$\overline{INTi}$ Input Low ("L") Width	250		ns

Rev.	Date	Description	
		Page	Summary
		65	• **Table 5.28 Memory Expansion Mode and Microprocessor Mode** tac1(AD-DB) expression modified
		77	• **Table 5.44 Electrical Characteristics** ICC standard value revised
		80	• **Table 5.47 Flash Memory Electrical Characteristics** Topr value modified
1.21	Jul.01, 2005	All pages	Package code changed: 144P6Q-A to PLQP0144KA-A, 100P6Q-A to PLQP0100KB-A, 100P6S-A to PRQP0100JB-A
		All pages	**"**Low Voltage Detection Reset**"** changed to **"**Brown-out Detection Reset**"**
			Special Function Register (SFR)
		27	• The G0RB register Value after reset modified
		39	• The TCSPR register Value after reset modified
			Electrical Characteristics
		47	• **Table 5.2 Electrical Characteristics** Parameter f(BCLK) and its values added
		51	• **Table 5.6 Flash Memory Version Electrical Characteristics** Mesurement condition changed
		53	• **Table 5.10 Memory Expansion Mode and Microprocessor Mode** *tac1(RD-DB)* expression on Note 1 modified; *tac2(RD-DB)* expression on Note 1 added
		59	• **Figure 5.3 Vcc1=Vcc2=5V Timing Diagram (1)** *tW(ER)* expression on Note 3 modified; *tcyc* expression added
		60	• **Figure 5.4 Vcc1=Vcc2=5V Timing Diagram (2)** *tac2(AD-DB)* expression on Note 1 modified; *th(ALE-AD)* expressions on Notes 1 and 2 modified; *tcyc* expression added
		65	• **Table 5.28 Memory Expansion Mode and Microprocessor Mode** *tac1(RD-DB)* expression on Note 1 modified; *tac2(RD-DB)* expression on Note 1 added
		70	• **Figure 5.7 Vcc1=Vcc2=3.3V Timing Diagram (1)** *tW(ER)* expression on Note 3 modified; *tcyc* expression added
		71	• **Figure 5.8 Vcc1=Vcc2=3.3V Timing Diagram (2)** *tac2(RD-DB)* expression on Note 1 modified; *th(ALE-AD)* expressions on Notes 1 and 2 modified; *th(WR-CS)* expression on Note 2 modified; *tcyc* expression added
		76	• **Table 5.43 Electrical Characteristics** Parameter f(BCLK) and its values added
		80	• **Table 5.47 Flash Memory Version Electrical Characteristics** Mesurement condition changed