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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, LVD, POR, PWM, WDT
Number of I/O	48
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z32f12811ars

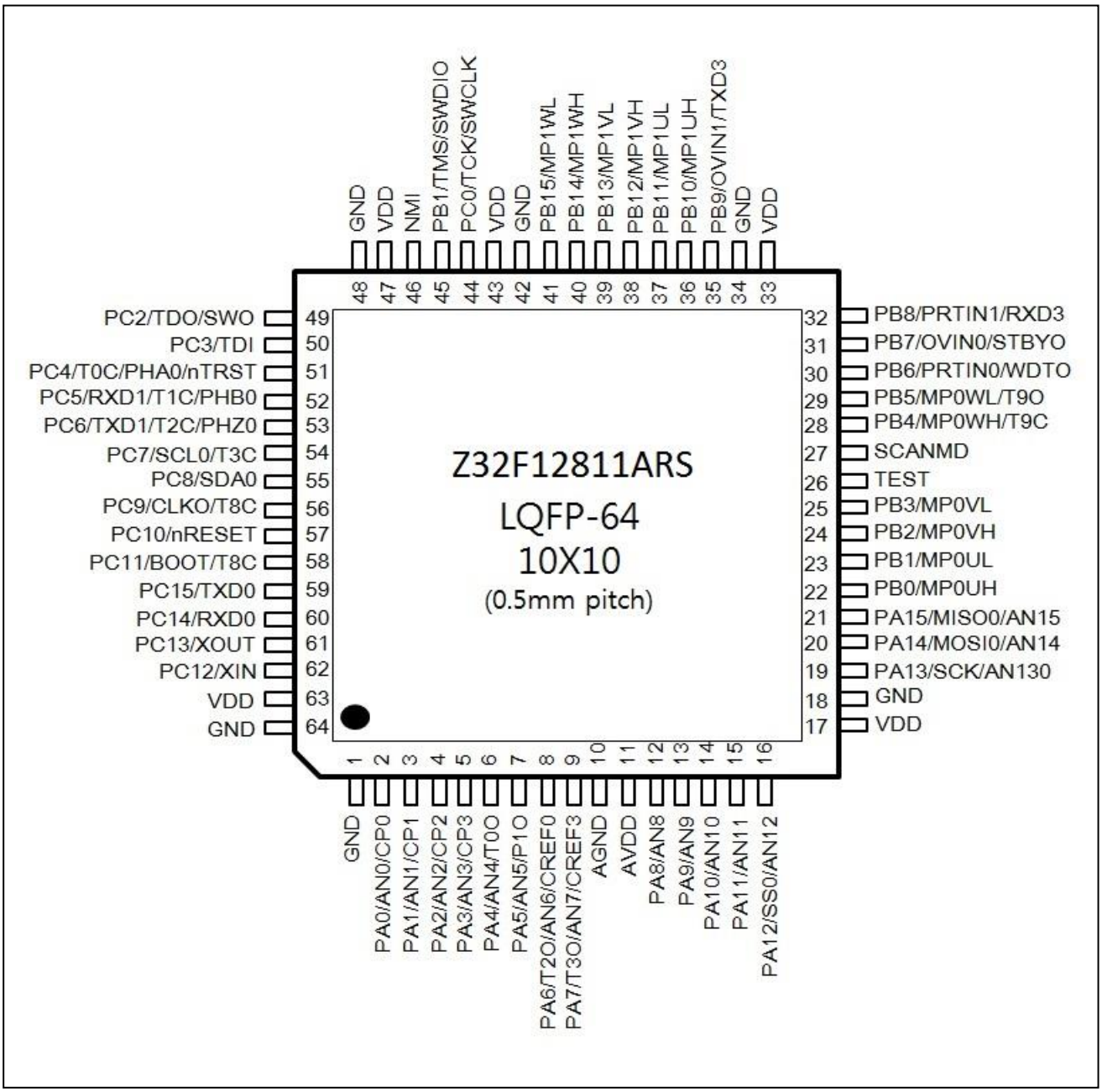

Figure 1.3. Pin Layout (LQFP-64)

39	-	PD8	IOUS	PORT D Bit 8 Input/Output	
		WDTO	Output	WDT Output	
30	-	PD9	IOUS	PORT D Bit 9 Input/Output	
		STBYO	Output	Power-down mode indication signal	
41	33	VDD	P	VDD	
42	34	GND	P	Ground	
43	35	PB9	IOUS	PORT B Bit 9 Input/Output	
		OVIN1	Input	PWM1 Over-voltage Input signal 1	
		TXD3	Output	UART3 TXD Output	
44	36	PB10	IOUS	PORT B Bit 10 Input/Output	
		PWM1H0	Output	PWM Channel 1 Phase 0 H-side Output	
45	37	PB11	IOUS	PORT B Bit 11 Input/Output	
		PWM1L0	Output	PWM Channel 1 Phase 0 L-side Output	
46	38	PB12	IOUS	PORT B Bit 12 Input/Output	
		PWM1H1	Output	PWM Channel 1 Phase 1 H-side Output	
47	39	PB13	IOUS	PORT B Bit 13 Input/Output	
		PWM1L1	Output	PWM Channel 1 Phase 1 L-side Output	
48	40	PB14	IOUS	PORT B Bit 14 Input/Output	
		PWM1H2	Output	PWM Channel 1 Phase 2 H-side Output	
49	41	PB15	IOUS	PORT B Bit 15 Input/Output	
		PWM1L2	Output	PWM Channel 1 Phase 2 L-side Output	
50	42	GND	P	Ground	
51	43	VDD	P	VDD	
52	44	PC0	IOUS	PORT C Bit 0 Input/Output	
		TCK/SWCK	Input	JTAG TCK, SWD Clock Input	
53	45	PC1	IOUS	PORT C Bit 1 Input/Output	
		TMS/SWDIO	I/O	JTAG TMS, SWD Data Input/Output	
54	-	PD10	IOUS	PORT D Bit 10 Input/Output	
		AD0SOC	Output	ADC0 Start-of-Conversion	
		T0C/PHA	Input	Timer 0 Clock/Capture/Phase-A Input	
55	-	PD11	IOUS	PORT D Bit 10 Input/Output	
		AD0EOC	Output	ADC0 End-of-Conversion	
		T1C/PHB	Input	Timer 1 Clock/Capture/Phase-B Input	
56	46	NMI	Input	Non-maskable Interrupt Input	
57	-	PD12	IOUS	PORT D Bit 12 Input/Output	
		AD1SOC	Output	ADC1 Start-of-Conversion	
		T2C/PHZ0	Input	Timer 2 Clock/Capture/Phase-Z Input	
58	-	PD13	IOUS	PORT D Bit 13 Input/Output	
		AD1EOC	Output	ADC1 End-of-Conversion	
		T3C	Input	Timer 3 Clock/Capture Input	
59	47	VDD	P	VDD	
60	48	GND	P	Ground	
61	49	PC2	IOUS	PORT C Bit 2 Input/Output	
		TDO/SWO	Output	JTAG TDO, SWO Output	
62	50	PC3	IOUS	PORT C Bit 3 Input/Output	
		TDI	Input	JTAG TDI Input	
63	51	PC4	IOUS	PORT C Bit 4Input/Output	
		nTRST	Input	JTAG nTRST Input	
		T0C/PHA	Input	Timer 0 Clock/Capture/Phase-A Input	
64	52	PC5	IOUS	PORT C Bit 5Input/Output	
		RXD1	Input	UART1 RXD Input	
		T1C/PHB	Input	Timer 1 Clock/Capture/Phase-B Input	
65	53	PC6	IOUS	PORT C Bit 6Input/Output	

		TXD1	Output	UART1 TXD Output	
		T2C/PHZ	Input	Timer 2 Clock/Capture/Phase-Z Input	
66	54	PC7	IOUS	PORT C Bit 7Input/Output	
		SCL0	Output	I^2C Channel 0 SCL In/Out	
		T3C	Input	Timer 3 Clock/Capture input	
67	55	PC8	IOUS	PORT C Bit 8 Input/Output	
		SDA0	Output	I^2C Channel 0 SDA In/Out	
68	56	PC9	IOUS	PORT C Bit 9 Input/Output	
		CLKO	Output	System Clock Output	
		T8O	Output	Timer 8 Output	
69	57	PC10	IOUS	PORT C Bit 10 Input/Output	
		nRESET	Input	External Reset Input	Pull-up
70	58	PC11	IOUS	PORT C Bit 11 Input/Output	
		BOOT	Input	Boot mode Selection Input	
		T8C	Input	Timer 8 Clock/Capture Input	
71	-	PD14	IOUS	PORT D Bit 14 Input/Output	
		AD2SOC	Output	ADC2 Start-of-Conversion Output signal	
72	-	TD15	IOUS	PORT D Bit 15 Input/Output	
		AD2EOC	Output	ADC2 Start-of-Conversion Output signal	
73	59	PC15	IOUS	PORT C Bit 14 Input/Output	
		TXD0	Output	UART0 TXD Output	
		MISO0	I/O	SPI0 Master-Input/Slave-Output	
74	60	PC14	IOUS	PORT C Bit 14 Input/Output	
		RXD0	Input	UART0 RXD Input	
		MOSI0	I/O	SPI0 Master-Output/Slave-Input	
		VMARGIN	OA	Not used. (test purpose)	
75	61	PC13	IOUS	PORT C Bit 13 Input/Output	
		XOUT	OA	External Crystal Oscillator Output	
76	62	PC12	IOUS	PORT C Bit 12 Input/Output	
		XIN	IA	External Crystal Oscillator Input	
77	-	PD0	IOUS	PORT D Bit 0 Input/Output	
		SS1	I/O	SPI1 Slave Select	
78	-	PD1	IOUS	PORT D Bit 1 Input/Output	
		SCK1	I/O	SPI1 Clock Input/Output	

*Notation: I=Input, O=Output, U=Pull-up, D=Pull-down,
S=Schmitt-Trigger Input Type, C=CMOS Input Type, A=Analog, P=Power
(*) Selected pin function after reset condition
Pin order may be changed with revision notice

3. Boot Mode

Boot Mode Pins

The Z32F1281 MCU has a Boot Mode option to program internal Flash memory. When the BOOT pin is pulled low, the system will start up in the BOOT area (0x1FFF_0000) instead of the default Flash area (0x0000_0000). This provides the ability to flash the part using either UART or SPI interfaces. The BOOT pin has an internal pull up resistor. Therefore, when the BOOT pin is not connected, it rides high (normal state).

Boot Mode uses the UART0 port and the SPI0 ports for the interface. The JTAG and SW interfaces can also be used, which provide the ability to recover from a bad Flash update that prevents the JTAG or SW debugger from attaching.

The pins for Boot Mode are listed in Table 3.1.

Table 3.1. Boot Mode Pin List

Block	Pin Name	Dir	Description
SYSTEM	**nRESET/PC10**	I	Reset Input signal
	BOOT/PC11	I	'0' to enter Boot mode
UART0	**RXD0/PC14**	I	UART Boot Receive Data
	TXD0/PC15	O	UART Boot Transmit Data
SPI0	**SS0/PA12**	I	SPI Boot Slave Select
	SCK0/PA13	I	SPI Boot Clock Input
	MOSI0/PA14	I	SPI Boot Data Input
	MISO0/PA15	O	SPI Boot Data Output

RSER Reset Source Enable Register

The reset source which will generate the reset event can be selected by the RSER register. Write **1** in the bit field of each reset source to transfer the reset source event to the reset generator. Write **0** in the bit field of each reset source to mask the reset source event, and therefore, not generate the reset event.

RSER=0x4000_0018

7	6	5	4	3	2	1	0
	PINRST	CPURST	SWRST	WDTRST	MCKFRST	XFRST	LVDRST
0	1	0	0	1	0	0	1
	RW	RW	RW	RW	RW	RW	RW

6	PINRST	External pin reset enable bit
		0 Reset from this event is masked
		1 Reset from this event is enabled
5	CPURST	CPU request reset enable bit
		0 Reset from this event is masked
		1 Reset from this event is enabled
4	SWRST	Software reset enable bit
		0 Reset from this event is masked
		1 Reset from this event is enabled
3	WDTRST	Watchdog Timer reset enable bit
		0 Reset from this event is masked
		1 Reset from this event is enabled
2	MCKFRST	MCLK Clock fail reset enable bit
		0 Reset from this event is masked
		1 Reset from this event is enabled
1	XFRST	External OSC Clock fail reset enable bit
		0 Reset from this event is masked
		1 Reset from this event is enabled
0	LVDRST	LVD reset enable bit
		0 Reset from this event is masked
		1 Reset from this event is enabled

PER2 Peripheral Enable Register 2

To use a peripheral unit, it should be activated by writing **1** to the corresponding bit in the PER1/2 register. Prior to activation, the peripheral stays in reset state.

To disable the peripheral unit, write **0** to the corresponding bit in the PER0/1 register, after which the peripheral enters the reset state.

PER2=0x4000_002C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								AFE	ADC2	ADC1	ADC0			MPWM1	MWPM0					UART3	UART2	UART1	UART0			I2C1	I2C0			SPI1	SPI0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1
								RW	RW	RW	RW			RW	RW					RW	RW	RW	RW			RW	RW			RW	RW

23	AFE	AFE function enable
22	ADC2	ADC2 function enable
21	ADC1	ADC1 function enable
20	ADC0	ADC0 function enable
17	MPWM1	MPWM1 function enable
16	MPWM0	MPWM0 function enable
11	UART3	UART3 function enable
10	UART2	UART2 function enable
9	UART1	UART1 function enable
8	UART0	UART0 function enable
5	I2C1	I²C1 function enable
4	I2C0	I²C0 function enable
1	SPI1	SPI1 function enable
0	SPI0	SPI0 function enable

		1 TSL filed can be updated by writing
18 16	TSL[2:0]	TSL trim value
15	LTEN	LTM/LT value write enable. Write only with LTM/LT value
		0 LT field is not updated by writing
		1 LT filed can be updated by writing
13 8	LTM/LT	Internal oscillator LT trim value Not recommended strongly to write into this field
7	UDCEN	UDCH/UDCL value write enable. Write only with UDC value
		0 UDC field is not updated by writing
		1 UDC filed can be updated by writing
4 0	UDCH/UDCL	Internal oscillator UDC trim value Not recommended strongly to write into this field

All trim bits are writable when Trim mode is enabled.

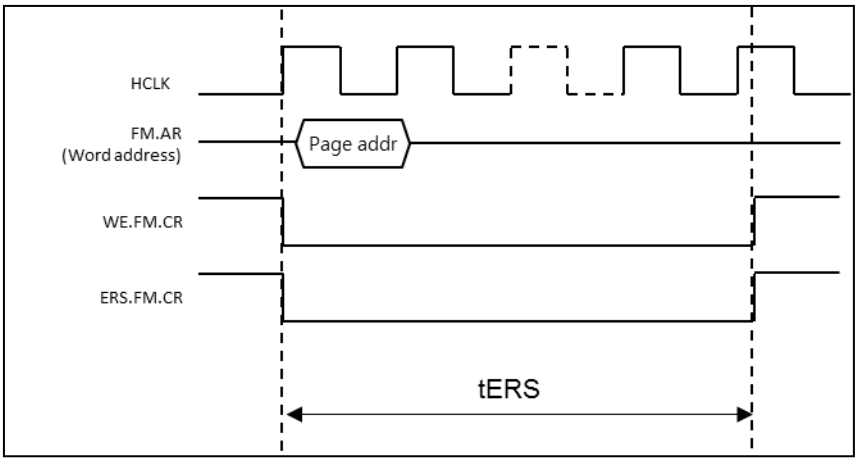

Figure 7.4. Page Erase Timing Diagram

Flash erase is done by the ERS.FM.CR command. A safe writing operation requires the correct program time. The tERS erase time is defined by the FM.TMR register. When the timer is activated (TIMER.FM.CR bit is set), the IDLE.FM.MR bit is cleared and the Flash controller will start counting the HCLK pulses until the pulse count matches the value in the FM.TMR. When the count is reached, the Flash controller will set the IDLE.FM.MR bit to show the time has elapsed.

Figure 7.5 shows the bulk erase operation.

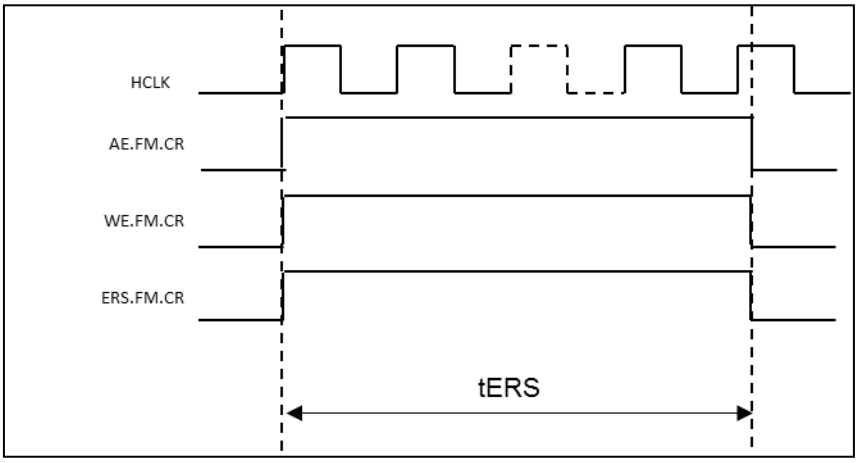

Figure 7.5. Bulk Erase Timing Diagram

The Flash area can be read from directly via the memory address. Writing of Flash memory can be done through Boot mode or in-application programming. The execution for the writing of Flash must occur from the RAM area. The Flash controller cannot read Flash memory (including instructions) once the program bit has been set.
Caution: If the vector table is not placed in RAM, you MUST disable interrupts so as to prevent reading the interrupt service routine in Flash.

To write to Flash memory:

1. Disable the Watch Dog Timer (if enabled).
2. Set the clock to internal oscillator (20 MHz).
3. Write configuration sequence to the MR register to enable Control Register upper bits (24-31).
4. Configure upper bits of the Control Register (HRESPD and Flash access of 4 cycles).
5. Lock the Flash controller by writing `0x00` to the MR register.

TnCR2 Timer n Control Register 2

Timer Control Register 2 is an 8-bit register.

T0CR2=0x4000_3004, T1CR2=0x4000_3024
T2CR2=0x4000_3044, T3CR2=0x4000_3064
T8CR2=0x4000_3104, T9CR2=0x4000_3124

7	6	5	4	3	2	1	0
						TCLR	TEN
0	0	0	0	0	0	0	0
R	R	R	R	R	R	WO	RW

1	TCLR	Timer Count register clear
	0	No
	1	Initialize timer. If set to '1', count register will be cleared. This is write-only.
0	TEN	Timer enable bit
	0	Disable timer
	1	Enable timer

TnPRS Timer n Prescaler Register

Timer Prescaler Register sets the pre-scale of the input clock for the timer counter.

T0PRS=0x4000_3008, T1PRS=0x4000_3028
T2PRS =0x4000_3048, T3PRS=0x4000_3068
T8PRS=0x4000_3108, T9PRS=0x4000_3128

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
						PRS									
0	0	0	0	0	0	000									
						RW									

9	PRS	Pre-scale value of count clock
0		TCLK = CLOCK_IN/(PRS+1)
		(*CLOCK_IN* is a selected timer input clock in TnCR1[CKSEL])

TnGRA Timer n General Register A

Timer General Register A is a 16-bit register.

T0GRA=0x4000_300C, T1GRA=0x4000_302C
T2GRA =0x4000_304C, T3GRA=0x4000_306C
T8GRA=0x4000_310C, T9GRA=0x4000_312C

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GRA															
0x0000															
RW															

15 0	GRA	Timer n General Register A Periodic mode - Period value of time internal. - When the counter value is matched with this value, GRA Match interrupt is requested PWM mode - Duty value of PWM Output - When the counter value is matched with this value, GRA Match interrupt is requested One-shot mode - One-shot delay timing before output pulse. - When the counter value is matched with this value, GRA Match interrupt is requested Capture mode - Falling edge of TnC port will capture the count value when rising edge clear mode - Rising edge of TnC port will capture the count value when falling edge clear mode

TnSR Timer n Status Register

Timer Status Register is a 16-bit register. This register indicates the current status of the timer module.

T0SR=0x4000_3018, T1SR=0x4000_3038
T2SR=0x4000_3058, T3SR=0x4000_3078
T8SR=0x4000_3118, T9SR=0x4000_3138

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
					QDIR	QDIRCH	QRF						MFA	MFB	OVF
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
					RW	RW	RW						RW	RW	RW

10	QDIR	Current Direction
		0 Phase A leading Phase B (clockwise)
		1 Phase B leading Phase A (counterclockwise)
9	QDIRCH	Quadrature direction change
		0 No direction change
		1 Direction is changed. Write '1' to this bit for clear
8	QRF	Quadrature revolution flag
		0 No revolution flag
		1 Revolution flag is detected. Write '1' to this bit for clear
2	MFA	GRA Match flag
		0 Not match with GRA
		1 Match flag with GRA. Write '1' to this bit for clear
1	MFB	GRB Match flag
		0 Not match with GRB
		1 Match flag with GRB. Write '1' to this bit for clear
0	OVF	Counter overflow flag
		0 No overflow event
		1 Counter overflowed. Write '1' to this bit for clear

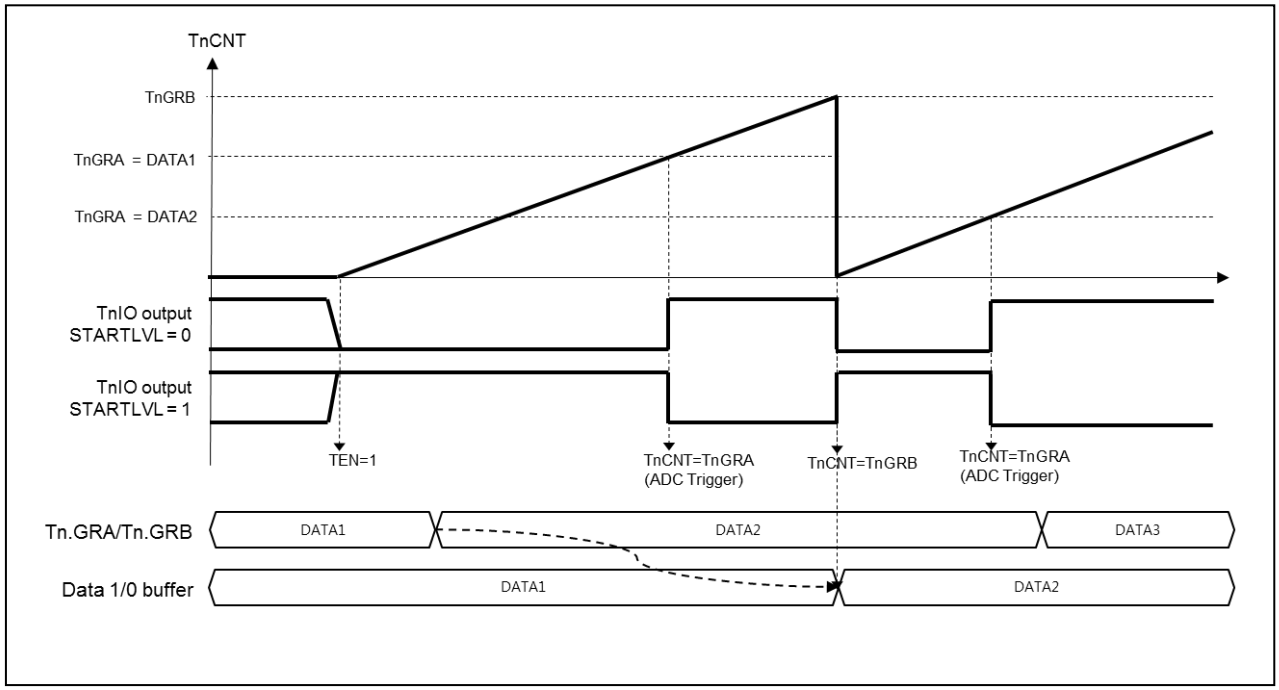

Figure 11.5. PWM Output Operation

The PWM pulse period can be calculated as follows:

The period = TMCLK Period * Tn.GRB value

Match A interrupt time = TMCLK Period * Tn.GRA value

If Tn.GRB = 0, the timer cannot be started even if TnCR2.TEN is “1” because the period is “0”.

The values in Tn.GRA and Tn.GRB are loaded into the internal compare data buffers 0 and 1 when the loading condition occurs. In this mode, the Tn.CR2.TCLR write operation and the GRB match event will load the data buffer.

The TnIO output signal generates a PWM pulse. The Tn.GRB value defines the output pulse period and the Tn.GRA value defines the pulse width of one shot pulse. The active level of PWM pulse can be controlled by the Tn.CR1.STARTLVL bit value.

ADC Trigger generation is available at Match A interrupt time.

Capture Mode

Figure 11.6 shows the timing diagram in capture mode operation. The TnIO input signal is used for the capture pulse. Both rising and falling edges can capture the counter values in each capture condition.

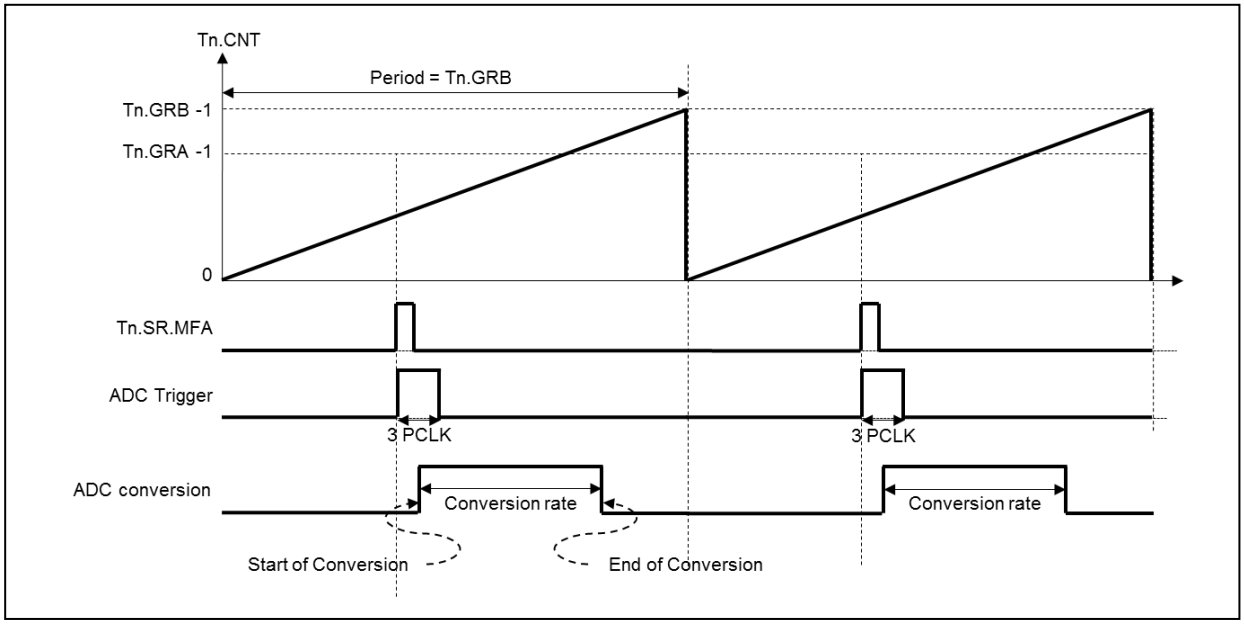

Figure 11.7. ADC Trigger Function Timing Diagram

Setup Example: Using the 16-bit Timer0 for Continuous Mode Operation

1. Enable the Timer0 peripheral by writing the appropriate value to the Peripheral Enable Register (PER1).
2. Enable the Timer0 peripheral clock by writing the appropriate value to the Peripheral Clock Enable Register (PCER).
3. Stop Timer0 before modifying the Timer0 registers by resetting bit0 in the Timer Control Register2 (TnCR2).
4. In Timer Control Register1 (TnCR1), write the appropriate value to enable the Timer0 Normal Period Operation Mode (e.g. 0x0000).
5. Write the appropriate Timer prescalar value to the Timer Prescalar Register (TnPRS).
6. Write the appropriate Timer count match value to the Timer General Register A (TnGRA) register. This timer count match value is compared to the actual count value in the Timer Count Register (TnCNT).
7. Write the appropriate value to Timer Interrupt Enable Register (TnIER) to enable or disable the Timer interrupt.
8. Start the Timer by setting bit0 and bit1; Timer Control Register2 (TnCR2) is enabled and initialized.

Note: Timer General Register A (TnGRA) is used for normal Timer operations. Timer General Register B (TnGRB) is used for Timer PWM modes.

UnTHR Transmit Data Hold Register

The UART Transmit Data Hold Register is an 8-bit write-only register.

U0THR=0x4000_8000, U1THR=0x4000_8100
U2THR=0x4000_8200, U3THR=0x4000_8300

7	6	5	4	3	2	1	0
THR							
-							
WO							

7 0	THR	Transmit Data Hold Register

UnIER UART Interrupt Enable Register

The UART Interrupt Enable Register is an 8-bit register.

U0IER=0x4000_8004, U1IER=0x4000_8104
U2IER=0x4000_8204, U3IER=0x4000_8304

7	6	5	4	3	2	1	0
-	-	DTXIEN	DRXIEN	-	RLSIE	THREIE	DRIE
0	0	0	0	0	0	0	0
		RW	RW		RW	RW	RW

5	DTXIEN	DMA transmit done interrupt enable
		0 DMA transmit done interrupt is disabled
		1 DMA transmit done interrupt is enabled
4	DRXIEN	DMA receive done interrupt enable
		0 DMA receive done interrupt is disabled
		1 DMA receive done interrupt is enabled
2	RLSIE	Receiver line status interrupt enable
		0 Receive line status interrupt is disabled
		1 Receive line status interrupt is enabled
1	THREIE	Transmit holding register empty interrupt enable
		0 Transmit holding register empty interrupt is disabled
		1 Transmit holding register empty interrupt is enabled
0	DRIE	Data receive interrupt enable
		0 Data receive interrupt is disabled
		1 Data receive interrupt is enabled

SP*n*SR SPI n Status Register

SPnSR is a 10-bit read/write register. It contains the status of the SPI interface.

SP0SR=0x4000_9008, SP1SR=0x4000_9108

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
						TXDMAF	RXDMAF		SSDET	SSON	OVRF	UDRF	TXIDLE	TRDY	RRDY
0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0
						RC1	RC1		RC1	RC1	RC1	RC1	R	R	R

9	**TXDMAF**	DMA Transmit Operation Complete flag. (DMA to SPI)
		0 DMA Transmit Op is working or is disabled.
		1 DMA Transmit Op is done.
8	**RXDMAF**	DMA Receive Operation Complete flag. (SPI to DMA)
		0 DMA Receive Operation is working or is disabled.
		1 DMA Transmit Op is done.
7		Reserved
6	**SSDET**	The rising or falling edge of SS signal Detect flag.
		0 SS edge is not detected.
		1 SS edge is detected. - The bit is cleared when it is written as “0”.
5	**SSON**	SS signal Status flag.
		0 SS signal is inactive.
		1 SS signal is active.
4	**OVRF**	Receive Overrun Error flag.
		0 Receive Overrun error is not detected.
		1 Receive Overrun error is detected. - This bit is cleared by writing or reading SPnRDR.
3	**UDRF**	Transmit Underrun Error flag.
		0 Transmit Underrun is not occurred.
		1 Transmit Underrun is occurred. - This bit is cleared by writing or reading SPnTDR.
2	**TXIDLE**	Transmit/Receive Operation flag.
		0 SPI is transmitting data
		1 SPI is in IDLE state.
1	**TRDY**	Transmit buffer Empty flag.
		0 Transmit buffer is busy.
		1 Transmit buffer is ready. - This bit is cleared by writing data to SPnTDR.
0	**RRDY**	Receive buffer Ready flag.
		0 Receive buffer has no data.
		1 Receive buffer has data. - This bit is cleared by reading data to SPnRDR.

ICnSAR I²C Slave Address Register

ICnSAR is an 8-bit read/write register. It shows the address in slave mode.

IC0SAR=0x4000_A00C, IC1SAR=0x4000_A10C

7	6	5	4	3	2	1	0
SVAD							GCEN
0x00							0
RW							RW

7 1	SVAD	7-bit Slave Address
0	GCEN	General call enable bit
		0 General call is disabled.
		1 General call is enabled.

START/Repeated START/STOP

Within the procedure of the I^2C-bus, unique situations arise which are defined as START(S) and STOP(P) conditions; see Figure 14.6.

An “H” to “L” transition on the SDA line while SCL is “H” is one such unique case. This situation indicates a START condition. An “L” to “H” transition on the SDA line while SCL is “H” defines a STOP condition.

START and STOP conditions are always generated by the master. The bus is considered to be busy after the START condition. The bus is considered to be free again a certain time after the STOP condition.

The bus is busy if a repeated START(Sr) is generated instead of a STOP condition. In this respect, the START(S) and repeated START(Sr) conditions are functionally identical. Therefore, for the remainder of this document, the S symbol will be used as a generic term to represent both the START and repeated START conditions, unless Sr is particularly relevant.

Detection of START and STOP conditions by devices connected to the bus is easy if they incorporate the necessary interfacing hardware. However, microcontrollers with no such interface have to sample the SDA line at least twice per clock period to sense the transition.

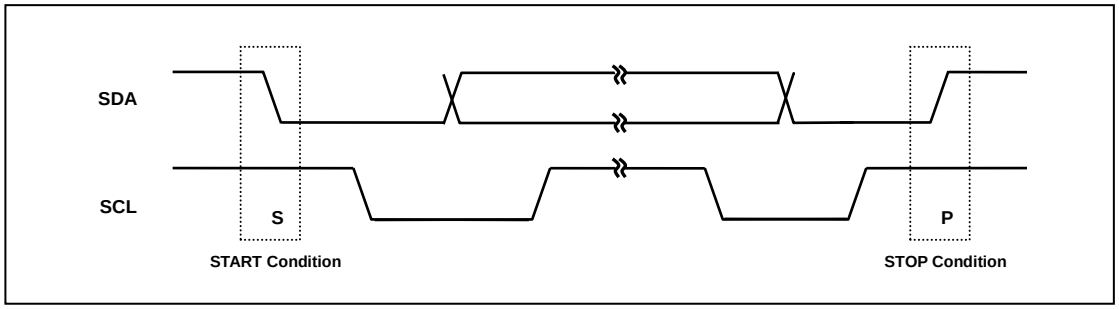

Figure 14.6. START and STOP Condition

OPAnCR OPAMP 0/1/2/3 Control Registers

Analog-front-end OPAMP 0/1/2/3 Control Registers are 8-bit registers. All four registers (AFEOPA0~AFEOPA3) have the same functions.

OPA0CR=0x4000_B300, OPA1CR =0x4000_B304
OPA2CR =0x4000_B308, OPA3CR =0x4000_B30C

7	6	5	4	3	2	1	0
			OPAEN	GAIN			
0	0	0	0	0x0			
			RW	RW			

4	OPAEN	0	OPAMP n Disable		
		1	OPAMP n Enable		
3	GAIN	0000	Gain = 2.19	1000	Gain = 4.37
0		0001	Gain = 2.33	1001	Gain = 5.0
		0010	Gain = 2.5	1010	Gain = 5.83
		0011	Gain = 2.69	1011	Gain = 7.0
		0100	Gain = 2.92	1100	Gain = 8.74
		0101	Gain = 3.18	1101	Reserved
		0110	Gain = 3.5	1110	Reserved
		0111	Gain = 3.89	1111	Gain = 1.00

CMPnCR Comparator 0/1/2/3 Control Register

Analog-front-end Comparator0/1/2/3 Control Registers are 8-bit registers. All four registers (AFECOMP0~AFECOMP3) have the same functions.

CMP0CR=0x4000_B320,CMP1CR =0x4000_B324
CMP2CR =0x4000_B328, CMP3CR =0x4000_B32C

7	6	5	4	3	2	1	0
			CMPEN			CINSEL	REFSEL
0	0	0	1	0	0	0	0
			RW			RW	RW

4	CMPEN	0	Comparator 0~3 Enable
		1	Comparator 0~3 Disable
1	CINSEL		Comparator input selection
		0	Input from OPAMP 0~3 each
		1	Input from external pin (see pin mux table)
0	REFSEL		Comparator reference selection
		0	Reserved
		1	REF input from external pin (see pin mux table)

When OPAMP is disabled, the OPAMP output is unknown (floating). Therefore, the user should set (write 1) CINSELx to choose the external input when OPAMP is an inactive state.

Current Consumption

Table 18.4. Current Consumption in Each Mode (Temperature: +25℃)

Parameter	Symbol	Condition	Min	Typ.	Max	unit
Normal Operation	IDD_{NORMAL}	ROSC=RUN IOSC20=RUN MXOSC=8MHz HCLK=72MHz	-	35	-	mA
Sleep Mode	IDD_{SLEEP}	ROSC=RUN IOSC20=RUN MXOSC=STOP HCLK =RUN	-	3	-	mA

POR Electrical Characteristics

Table 18.5. POR Electrical Characteristics (Temperature: -40 ~ +85℃)

Parameter	Symbol	Condition	Min	Typ.	Max	unit
Operating Voltage	VDD18		1.6	1.8	2.0	V
Operating Current	IDD_{PoR}	Typ. <6uA If always on	-	60	-	nA
POR Set Level	VR_{PoR}	VDD rising (slow)	1.3	1.4	1.55	V
POR Reset Level	VF_{PoR}	VDD falling (slow)	1.1	1.2	1.4	V

LVD Electrical Characteristics

Table 18.6. LVD Electrical Characteristics (Temperature: -40 ~ +85℃)

Parameter	Symbol	Condition	Min	Typ.	Max	unit
Operating Voltage	VDD		1.7		5	V
Operating Current	IDD_{LVD}	Typ. <6uA when always on	-	1	-	mA
LVD Set Level 0	VLVD0	VDD falling (slow)	1.6	1.8	2.0	V
LVD Set Level 1	VLVD1	VDD falling (slow)	2.0	2.2	2.5	V
LVD Set Level 2	VLVD2	VDD falling (slow)	2.5	2.7	3.0	V
LVD Set Level 3	VLVD3	VDD falling (slow)	3.9	4.3	4.6	V

OP-Amp Electrical Characteristics

Table 18.12. ADC Electrical Characteristics (Temperature: -40 ~ +85℃)

Parameter	Symbol	Condition	Min	Typ.	Max	unit
Operating Voltage	AVDD		3.0	5	5.5	V
Operating Current	IDDA				2.2	mA
Analog Input Range			0		AVDD-1.4	V
Slew Rate		@ CL = 20pF		15		V/us
Gain Error		Gain=2.19~4.37	-3		+3	%
		Gain=5.0~8.74	-4		+4	%
Common Mode Rejection Ratio			50	70		dB
Power Supply Rejection Ratio			40	70		dB
Gain Bandwidth		@CL=20pF		16		MHz
Open Loop Voltage Gain				100		dB
Open Loop Phase Margin		@CL=20pF		45		°
Closed Loop Phase Margin				70		°
Turn On time				2		us
Gain			2.19		8.74	

Comparator Electrical Characteristics

Table 18.13. Comparator Electrical Characteristics (Temperature: -40 ~ +85℃)

Parameter	Symbol	Condition	Min	Typ.	Max	unit
Operating Voltage	AVDD		3.0	5	5.5	V
Analog Input Range	VIN		AVSS		AVDD	V
Reference Input Range	VREF		0.9		AVDD-0.2	V
Input Offset Voltage			-4		+4	%
Response Time					1	us