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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, LVD, POR, PWM, WDT
Number of I/O	68
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z32f12811ats

1. Overview

Introduction

Zilog's Z32F1281 MCU, a member of the ZNEO32! Family of microcontrollers is a cost-effective and high-performance 32-bit microcontroller. The Z32F1281 MCU provides 3-phase PWM generator units which are suitable for inverter bridges, including motor drive systems. The two built-in channels of these generators control two inverter motors simultaneously.

Three 12-bit high speed ADC units with 16-channel analog multiplexed inputs are included to gather information from the motor. The Z32F1281 MCU can control up to two inverter motors or one inverter motor and the Power Factor Correction (PFC) function simultaneously. Four on-chip operational AMPs and four analog comparators are available to measure analog input signals. The operational amplifier can amplify the input signal to the proper signal range and transfer it to the ADC input channel. The comparator monitors external signals and helps create an internal emergency signal. Multiple powerful external serial interface engines communicate with on-board sensors.

Figure 1.1 shows a block diagram of the Z32F1281 MCU.

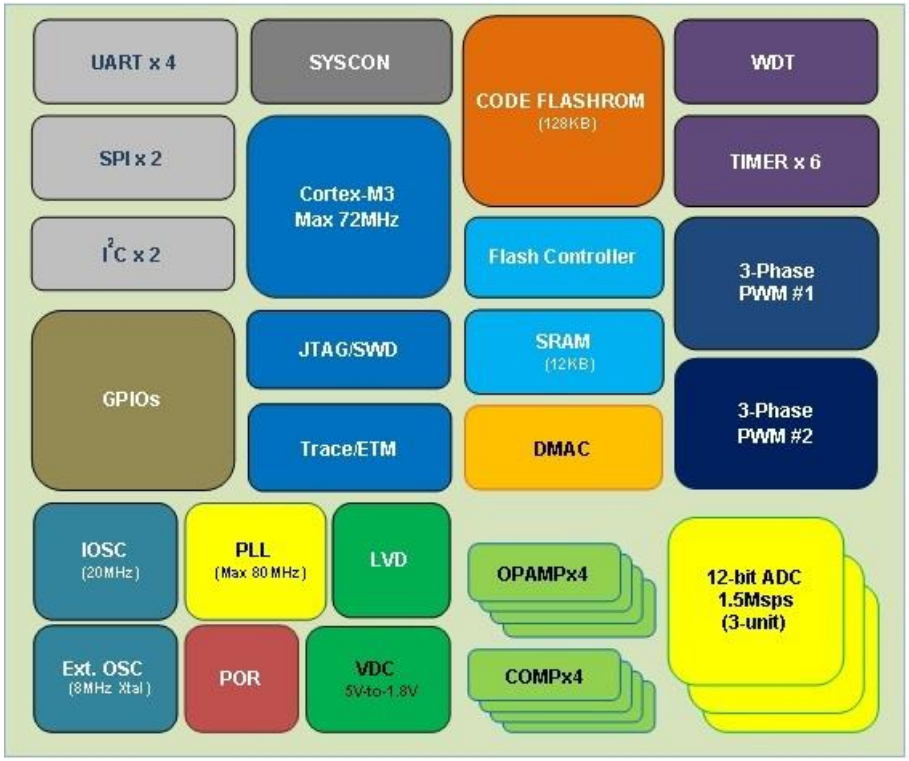


Figure 1.1. Z32F1281 MCU Block Diagram

PWM Generator

- Two channels of the 3-phase PWM generator are implemented. 16 bit up/down counter with prescaler supports triangular and saw tooth waveforms.
- The PWM generates an internal ADC trigger signal to measure the signal on time.
- Dead time insertion and emergency stop functionality ensure that the chip and system operate under safe conditions.

Serial Peripheral Interface (SPI)

- Synchronous serial communication is provided by the SPI block. The Z32F1281 MCU has 2 channel SPI modules. The DMA function is supported by the DMA controller. Transfer data is moved to/from the memory area without CPU operation.
- Boot mode uses this SPI block to download the Flash program.

Inter-Integrated Circuit Interface (I^2C)

- The Z32F1281 MCU has a 2-channel I^2C block and it supports up to 400 kHz I^2C communication. Master and the slave modes are supported.

Universal Asynchronous Receiver/Transmitter (UART)

- The Z32F1281 MCU includes a 4-channel UART block. For accurate baud rate control, a fractional baud rate generator is provided.
- The DMA function is supported by the DMA controller. Transfer data is moved to/from memory area without CPU operation.

General PORT I/Os

- 16-bit PA, PB, PC, PD ports are available and provide multiple functionality:
- General I/O port
- Independent bit set/clear function
- External interrupt input port
- Pull-up/Open-drain
- On chip debounce Filter

12-bit Analog-to-Digital Converter (ADC)

- 3 built-in ADCs can convert analog signal up to 1usec conversion rate. 16-channel analog mux and OP-AMP provides various combinations from external analog signals.

Analog Front End (AFE)

- Operational Amplifier (OPAMP)
  - 4 built-in OPAMPs amplify analog signals up to x8.74 gain
- Analog Comparator (COMP)
  - 4 built-in analog comparators

Pin Description

The pin configurations are shown in Table 1.2. 16 pins are reserved for power/ground pair and dedicated pins.

39	-	PD8	IOUS	PORT D Bit 8 Input/Output	
		WDTO	Output	WDT Output	
30	-	PD9	IOUS	PORT D Bit 9 Input/Output	
		STBYO	Output	Power-down mode indication signal	
41	33	VDD	P	VDD	
42	34	GND	P	Ground	
43	35	PB9	IOUS	PORT B Bit 9 Input/Output	
		OVIN1	Input	PWM1 Over-voltage Input signal 1	
		TXD3	Output	UART3 TXD Output	
44	36	PB10	IOUS	PORT B Bit 10 Input/Output	
		PWM1H0	Output	PWM Channel 1 Phase 0 H-side Output	
45	37	PB11	IOUS	PORT B Bit 11 Input/Output	
		PWM1L0	Output	PWM Channel 1 Phase 0 L-side Output	
46	38	PB12	IOUS	PORT B Bit 12 Input/Output	
		PWM1H1	Output	PWM Channel 1 Phase 1 H-side Output	
47	39	PB13	IOUS	PORT B Bit 13 Input/Output	
		PWM1L1	Output	PWM Channel 1 Phase 1 L-side Output	
48	40	PB14	IOUS	PORT B Bit 14 Input/Output	
		PWM1H2	Output	PWM Channel 1 Phase 2 H-side Output	
49	41	PB15	IOUS	PORT B Bit 15 Input/Output	
		PWM1L2	Output	PWM Channel 1 Phase 2 L-side Output	
50	42	GND	P	Ground	
51	43	VDD	P	VDD	
52	44	PC0	IOUS	PORT C Bit 0 Input/Output	
		TCK/SWCK	Input	JTAG TCK, SWD Clock Input	
53	45	PC1	IOUS	PORT C Bit 1 Input/Output	
		TMS/SWDIO	I/O	JTAG TMS, SWD Data Input/Output	
54	-	PD10	IOUS	PORT D Bit 10 Input/Output	
		AD0SOC	Output	ADC0 Start-of-Conversion	
		T0C/PHA	Input	Timer 0 Clock/Capture/Phase-A Input	
55	-	PD11	IOUS	PORT D Bit 10 Input/Output	
		AD0EOC	Output	ADC0 End-of-Conversion	
		T1C/PHB	Input	Timer 1 Clock/Capture/Phase-B Input	
56	46	NMI	Input	Non-maskable Interrupt Input	
57	-	PD12	IOUS	PORT D Bit 12 Input/Output	
		AD1SOC	Output	ADC1 Start-of-Conversion	
		T2C/PHZ0	Input	Timer 2 Clock/Capture/Phase-Z Input	
58	-	PD13	IOUS	PORT D Bit 13 Input/Output	
		AD1EOC	Output	ADC1 End-of-Conversion	
		T3C	Input	Timer 3 Clock/Capture Input	
59	47	VDD	P	VDD	
60	48	GND	P	Ground	
61	49	PC2	IOUS	PORT C Bit 2 Input/Output	
		TDO/SWO	Output	JTAG TDO, SWO Output	
62	50	PC3	IOUS	PORT C Bit 3 Input/Output	
		TDI	Input	JTAG TDI Input	
63	51	PC4	IOUS	PORT C Bit 4Input/Output	
		nTRST	Input	JTAG nTRST Input	
		T0C/PHA	Input	Timer 0 Clock/Capture/Phase-A Input	
64	52	PC5	IOUS	PORT C Bit 5Input/Output	
		RXD1	Input	UART1 RXD Input	
		T1C/PHB	Input	Timer 1 Clock/Capture/Phase-B Input	
65	53	PC6	IOUS	PORT C Bit 6Input/Output	

		TXD1	Output	UART1 TXD Output	
		T2C/PHZ	Input	Timer 2 Clock/Capture/Phase-Z Input	
66	54	PC7	IOUS	PORT C Bit 7Input/Output	
		SCL0	Output	I^2C Channel 0 SCL In/Out	
		T3C	Input	Timer 3 Clock/Capture input	
67	55	PC8	IOUS	PORT C Bit 8 Input/Output	
		SDA0	Output	I^2C Channel 0 SDA In/Out	
68	56	PC9	IOUS	PORT C Bit 9 Input/Output	
		CLKO	Output	System Clock Output	
		T8O	Output	Timer 8 Output	
69	57	PC10	IOUS	PORT C Bit 10 Input/Output	
		nRESET	Input	External Reset Input	Pull-up
70	58	PC11	IOUS	PORT C Bit 11 Input/Output	
		BOOT	Input	Boot mode Selection Input	
		T8C	Input	Timer 8 Clock/Capture Input	
71	-	PD14	IOUS	PORT D Bit 14 Input/Output	
		AD2SOC	Output	ADC2 Start-of-Conversion Output signal	
72	-	TD15	IOUS	PORT D Bit 15 Input/Output	
		AD2EOC	Output	ADC2 Start-of-Conversion Output signal	
73	59	PC15	IOUS	PORT C Bit 14 Input/Output	
		TXD0	Output	UART0 TXD Output	
		MISO0	I/O	SPI0 Master-Input/Slave-Output	
74	60	PC14	IOUS	PORT C Bit 14 Input/Output	
		RXD0	Input	UART0 RXD Input	
		MOSI0	I/O	SPI0 Master-Output/Slave-Input	
		VMARGIN	OA	Not used. (test purpose)	
75	61	PC13	IOUS	PORT C Bit 13 Input/Output	
		XOUT	OA	External Crystal Oscillator Output	
76	62	PC12	IOUS	PORT C Bit 12 Input/Output	
		XIN	IA	External Crystal Oscillator Input	
77	-	PD0	IOUS	PORT D Bit 0 Input/Output	
		SS1	I/O	SPI1 Slave Select	
78	-	PD1	IOUS	PORT D Bit 1 Input/Output	
		SCK1	I/O	SPI1 Clock Input/Output	

*Notation: I=Input, O=Output, U=Pull-up, D=Pull-down,
S=Schmitt-Trigger Input Type, C=CMOS Input Type, A=Analog, P=Power
(*) Selected pin function after reset condition
Pin order may be changed with revision notice

PRER2 Peripheral Reset Enable Register 2

The reset of each peripheral by an event reset can be masked by user settings. The PRER1/2 register controls enabling of the event reset. If the corresponding bit is **1**, the peripheral corresponding to this bit accepts the reset event. Otherwise, the peripheral is protected from the reset event and maintains its current operation.

PRER2=0x4000_0024

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								AFE	ADC2	ADC1	ADC0			MPWM1	MWPM0					UART3	UART2	UART1	UART0			I2C1	I2C0			SPI1	SPI0
0	0	0	0	0	0	0	0	1	1	1	1	0	0	1	1	0	0	0	0	1	1	1	1	0	0	1	1	0	0	1	1
								RW	RW	RW	RW			RW	RW					RW	RW	RW	RW			RW	RW			RW	RW

23	AFE	AFE reset enable
22	ADC2	ADC2 reset enable
21	ADC1	ADC1 reset enable
20	ADC0	ADC0 reset enable
17	MPWM1	MPWM1 reset enable
16	MPWM0	MPWM0 reset enable
11	UART3	UART3 reset enable
10	UART2	UART2 reset enable
9	UART1	UART1 reset enable
8	UART0	UART0 reset enable
5	I2C1	I²C1 reset enable
4	I2C0	I²C0 reset enable
1	SPI1	SPI1 reset enable
0	SPI0	SPI0 reset enable

100	N = 6
101	N = 8
110	Not available
111	N =16

MCCR2 Miscellaneous Clock Control Register 2

The Miscellaneous Clock Control Register 2 controls the configuration of MPWM0 and MPWM1 clocks.

MCCR2=0x4000_0094

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
					PWM1CSEL			PWM1DIV														PWM0CSEL			PWM0DIV							
0	0	0	0	0	000			0x00								0	0	0	0	0	000			0x00							
					RW			RW														RW			RW							

26 24	PWM1CSEL	PWM1 Clock source select bit 0xx RING OSC 1Mhz 100 MCLK (bus clock) 101 INT OSC 20MHz 110 External Main OSC 111 PLL Clock
23 16	PWM1DIV	PWM1 Clock N divider PWM1 input clock = Clock source / PWM1DIV (If PWM1DIV is 0, input clock will be stopped)
10 8	PWM0CSEL	PWM0 Clock source select bit 0xx RING OSC 1Mhz 100 MCLK (bus clock) 101 INT OSC 20MHz 110 External Main OSC 111 PLL Clock
7 0	PWM0DIV	PWM0 Clock N divider PWM0 input clock = Clock source / PWM0DIV (If PWM0DIV is 0, input clock will be stopped)

Functional Description

All the GPIO pins can be configured for different operations – inputs, outputs, and triggered interrupts (both level and edge) through the PDU. The system is also able to disable ports by setting the PER1 and PCER1 registers in the SCU. By default, all pins are disabled (except for UART0/SPI0) so the developer must enable these to operate.
All configuration parameters are protected by the Port Access Enable register. You must write the sequence in order (`0x15`, `0x51`) to the PORTEN register to configure any pin(s). Once the configuration is complete, write any other value to the PORTEN register to lock it.

Note: Do not read in between the sequence; it will prevent the configuration registers from being unlocked.

When the input function of I/O port is used by the Pin Control Register, the output function of I/O port is disabled. The Port Function differs according to the Pin Mux Register. The Input Data Register captures the data present on the I/O pin or debounced input data at every GPIO clock cycle.

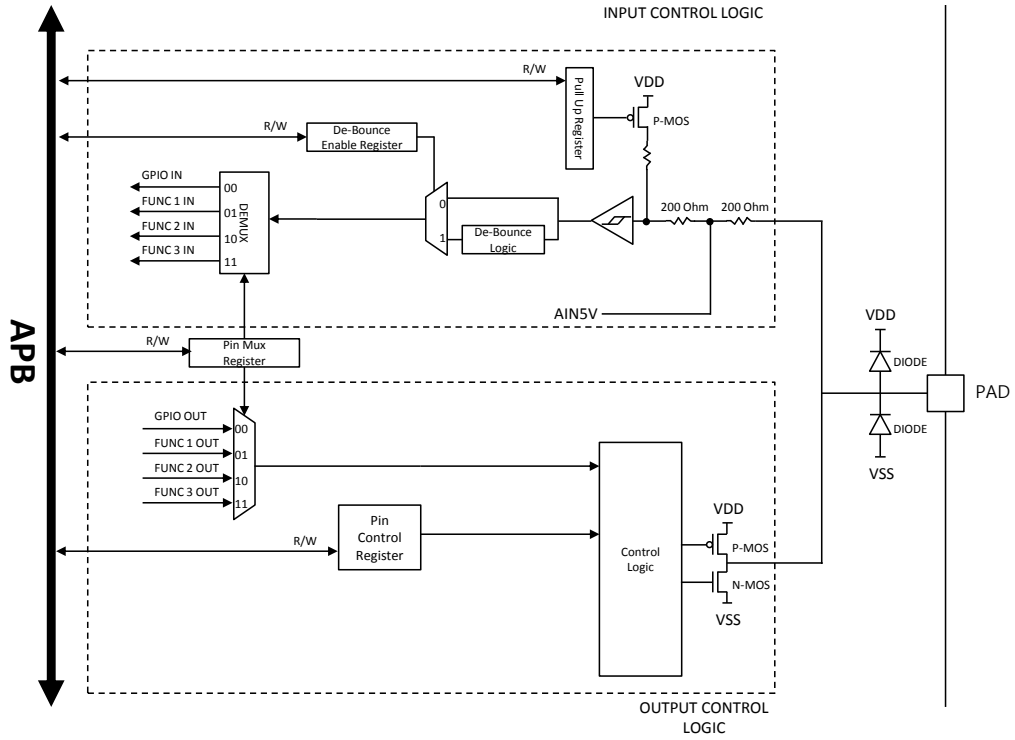


Figure 5.4. Port Diagram

FMDRTY Flash Memory Dirty Bit Register

FMDRTY is the internal Flash memory dirty bit clear register.

FMDRTY=0x4000_0118

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FDRTY																															
-																															
WO																															

31 0	FDRTY	Write any value here, cache line fill flag will be cleared.

FMTICK Flash Memory Tick Timer Register

FMTICK is the internal Flash memory Burst Mode channel selection register.

FMTICK=0x4000_011C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
														FTICK																	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x00000															
																RW															

17 0	FTICK	TICK goes to 0x3FFFF from written TICK value while TRM runs by PCLK clock

FMCRC Flash Memory CRC Value Register

The register shows the CRC value resulting from read accesses on internal Flash memory.

FMTICK=0x4000_0120

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																CRC															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	--															
																RO															

15 0	CRC	CRC16 value

9. Direct Memory Access Controller

Introduction

The Direct Memory Access (DMA) controller includes the following features:

- 15 channels
- Single transfer only
- Supports 8/16/32-bit data size
- Supports multiple buffers with the same size
- Interrupt condition is transferred through a peripheral interrupt

A block diagram of the DMA controller is shown in Figure 9.1.

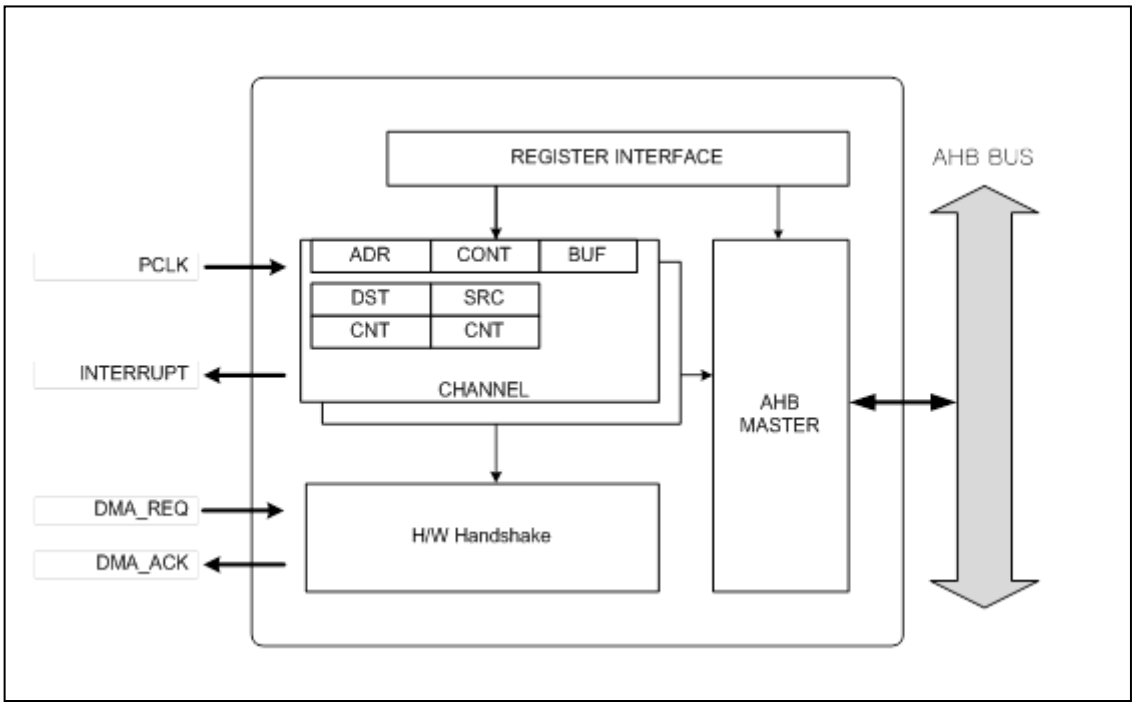


Figure 9.1. DMAC Block Diagram

Pin Description

There are no external interface pins.

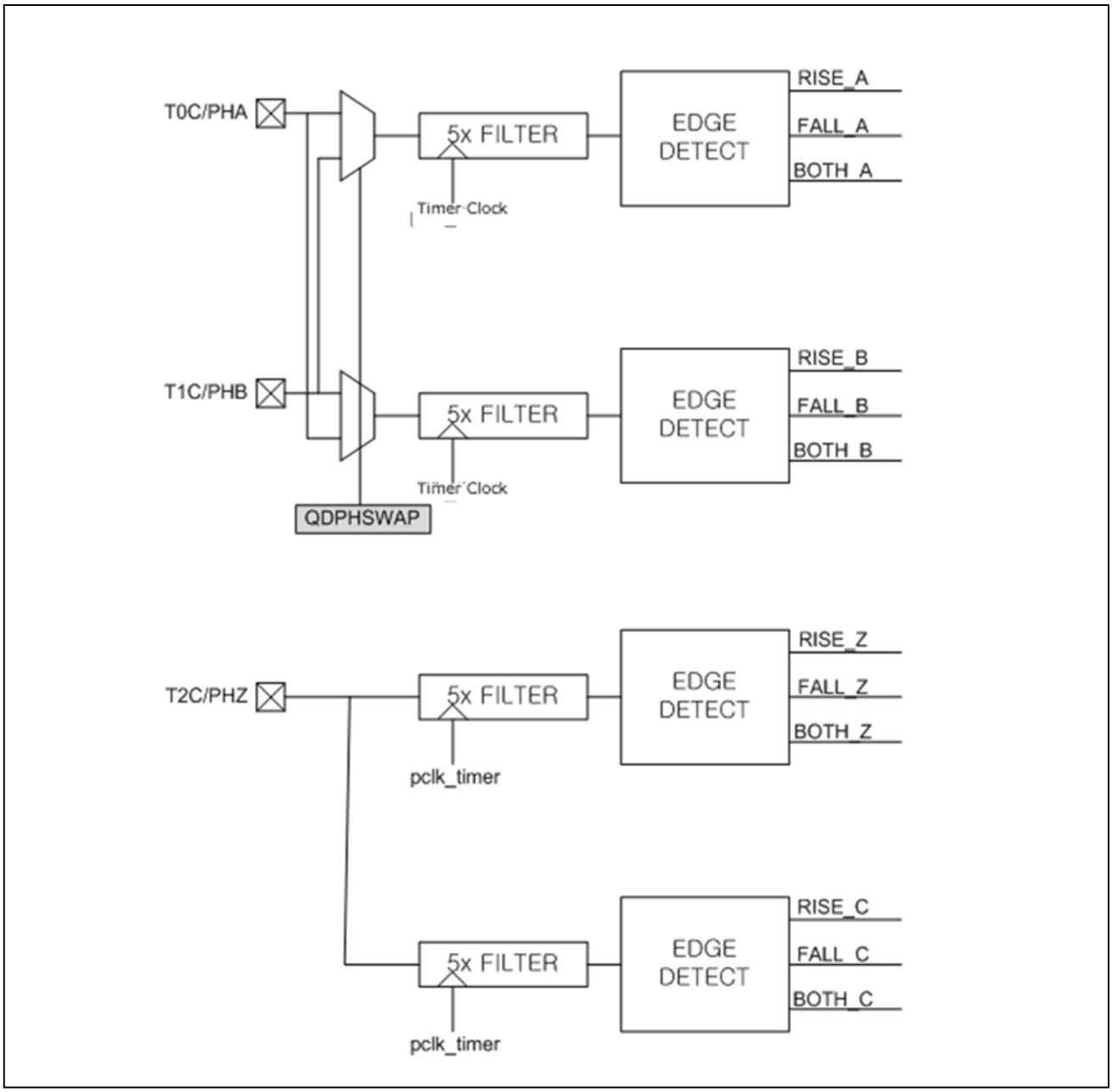


Figure 11.9. Quadrature Encoder Interface Input Block

Pin Description

Table 14.1. I²C Interface External Pins

PIN NAME	TYPE	DESCRIPTION
SCL0	I/O	I²C channel 0 Serial clock bus line (open-drain)
SDA0	I/O	I²C channel 0 Serial data bus line (open-drain)
SCL1	I/O	I²C channel 1 Serial clock bus line (open-drain)
SDA1	I/O	I²C channel 1 Serial data bus line (open-drain)

Registers

The base address of I²C0 is `0x4000_A000` and the base address of I²C1 is `0x4000_A100`. The register map is described in Table 14.2 and Table 14.3.

Table 14.2.I²C Interface Base Address

Channel	Base address
I²C0	0x4000_A000
I²C1	0x4000_A100

Table 14.3.I²C Register Map

Name	Offset	R/W	Description	Reset
IC0DR	0xA000	R/W	I²C0 Data Register	0xFF
IC0SR	0xA008	R, R/W	I²C0 Status Register	0x00
IC0SAR	0xA00C	R/W	I²C0 Slave Address Register	0x00
IC0CR	0xA014	R/W	I²C0 Control Register	0x00
IC0SCLL	0xA018	R/W	I²C0 SCL LOW duration Register	0xFFFF
IC0SCLH	0xA01C	R/W	I²C0 SCL HIGH duration Register	0xFFFF
IC0SDH	0xA020	R/W	I²C0 SDA Hold Register	0x7FFF
IC1DR	0xA100	R/W	I²C1 Data Register	0xFF
IC1SR	0xA108	R, R/W	I²C1 Status Register	0x00
IC1SAR	0xA10C	R/W	I²C1 Slave Address Register	0x00
IC1CR	0xA114	R/W	I²C1 Control Register	0x00
IC1SCLL	0xA118	R/W	I²C1 SCL LOW duration Register	0xFFFF
IC1SCLH	0xA11C	R/W	I²C1 SCL HIGH duration Register	0xFFFF
IC1SDH	0xA120	R/W	I²C1 SDA Hold Register	0x7FFF

START/Repeated START/STOP

Within the procedure of the I^2C-bus, unique situations arise which are defined as START(S) and STOP(P) conditions; see Figure 14.6.

An “H” to “L” transition on the SDA line while SCL is “H” is one such unique case. This situation indicates a START condition. An “L” to “H” transition on the SDA line while SCL is “H” defines a STOP condition.

START and STOP conditions are always generated by the master. The bus is considered to be busy after the START condition. The bus is considered to be free again a certain time after the STOP condition.

The bus is busy if a repeated START(Sr) is generated instead of a STOP condition. In this respect, the START(S) and repeated START(Sr) conditions are functionally identical. Therefore, for the remainder of this document, the S symbol will be used as a generic term to represent both the START and repeated START conditions, unless Sr is particularly relevant.

Detection of START and STOP conditions by devices connected to the bus is easy if they incorporate the necessary interfacing hardware. However, microcontrollers with no such interface have to sample the SDA line at least twice per clock period to sense the transition.

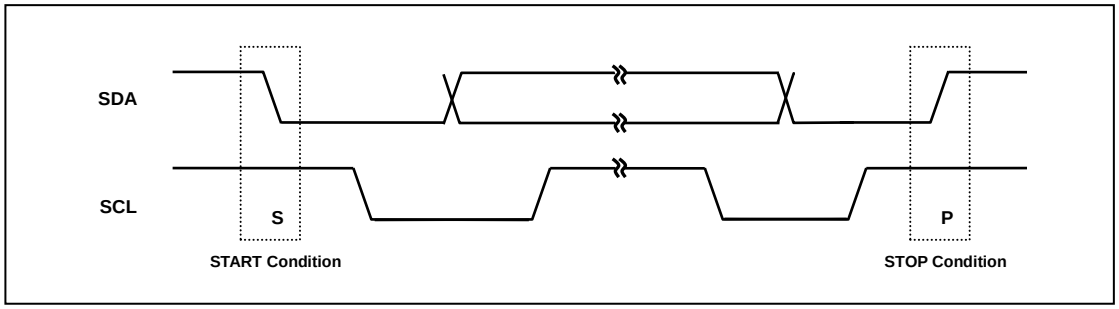


Figure 14.6. START and STOP Condition

initiated by the winning master.

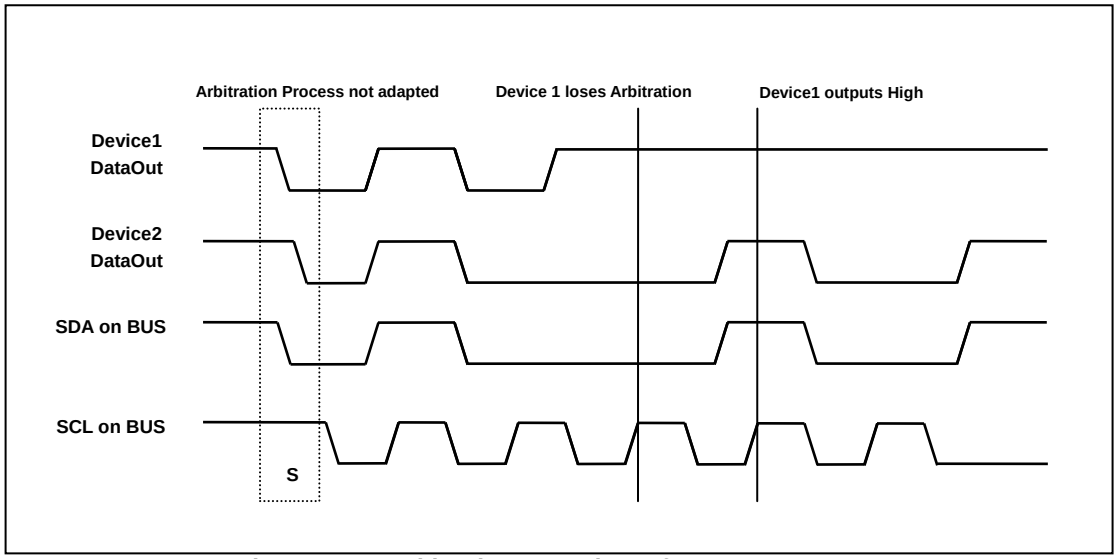


Figure 14.10. Arbitration Procedure of Two Masters

I²C Operation

I²C supports the interrupt operation. Once an interrupt is serviced, the IIF (ICnCR[7]) flag is set. ICnSR shows I²C-bus status information and the SCL line stays “L” before the register is written as a certain value. The status register can be cleared by writing a zero.

Master Transmitter

The master transmitter shows the flow of the transmitter in Master Mode as shown in Figure 14.11.

Pin Description

Table 15.1. External Signals

PIN NAME	TYPE	DESCRIPTION
MP0UH	O	MPWM 0 Phase-U H-side output
MP0UL	O	MPWM 0 Phase-U L-side output
MP0VH	O	MPWM 0 Phase-V H-side output
MP0VL	O	MPWM 0 Phase-V L-side output
MP0WH	O	MPWM 0 Phase-W H-side output
MP0WL	O	MPWM 0 Phase-W L-side output
MP1UH	O	MPWM 1 Phase-U H-side output
MP1UL	O	MPWM 1 Phase-U L-side output
MP1VH	O	MPWM 1 Phase-V H-side output
MP1VL	O	MPWM 1 Phase-V L-side output
MP1WH	O	MPWM 1 Phase-W H-side output
MP1WL	O	MPWM 1 Phase-W L-side output
PRTIN0	I	MPWM 0 Protection Input 0
OVIN0	I	MPWM 0 Over-voltage Input 1
PRTIN1	I	MPWM 1 Protection Input 0
OVIN1	I	MPWM 1 Over-voltage Input 1

Registers

The base address of MPWM is shown in Table 15.2.

Table 15.2. MPWM Base Address

	BASE ADDRESS
MPWM0	0x4000_4000
MPWM1	0x4000_5000

MPnMR MPWM Mode Register

The MPWM operation mode register is a 16-bit register.

MP0MR=0x4000_4000, MP1MR=0x4000_5000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOTOR		MCHMOD				UPDATE	UALL	FORCEN		FORCM				PDUP	UPDOWN
0	0	00		0	0	0	0	0	0	00		0	0	0	0
RW		RW				RW	RW	RW		RW				RW	RW

15	**MOTOR**	0	Normal PWM mode
		1	Motor PWM mode In Motor mode initial outputs of H-ch become LOW and outputs of L-ch become High (before PWM START)
13 12	**MCHMOD**	00	Motor control channel mode 2 channels symmetric mode Duty H decides the duty value of H-ch Duty L decides the duty value of L-ch
		01	1 channel asymmetric mode Duty H decides the up-counting duty value of H-ch Duty L decides the down-counting duty value of H-ch L channel become the inversion of H channel
		10	1 channel symmetric mode Duty H decides the duty value of H-ch L channel become the inversion of H channel
		11	Not valid (same with 00)
9	**UPDATE**	0	Update all duty, period register after
		1	Update all duty, period register enable. When UPDATE set, Duty and Period V registers are updated after two PWM clocks It should be cleared before PWM start(set PSTART)
8	**UALL**	0	No effect.
		1	Duty V and Duty W register will be stored with the same value of Duty U value when Duty U is written.
7	**FORCEN**	0	Force mode disable(normal mode)
		1	user can enable and disable each channels by Output control register
5 4	**FORCM**	00	Each channel is “AND”ed with MPnOCR (when port enable is low, output becomes low)
		01	Each channel is “OR”ed with MPnOCR (when port enable is high, output becomes high)
		10	Each channel is “XOR”ed with MPnOCR (when port enable is low, output becomes low)
		11	Each channel is “AND”ed with MPnOCR but when port is disabled, output becomes high-Z
1	**PDUP**	0	Period, duty value updated at every period match (both up count mode and BTB mode)
		1	Period, duty value updated at every period match and bottom(valid in up/down count mode)
0	**UPDOWN**	0	PWM Up count mode
		1	PWM Up and Down count mode Note: See Figure 15.2 for timing and operation.

MPnSR MPWM Status Register

The PWM Status Register is a 16-bit register.

MP0SR=0x4000_4030, MP1CR=0x4000_5030

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DOWN	IRQCNT							PRDIRQ	BOTIRQ	DUHIRQ	DULIRQ	DVHIRQ	DVLIRQ	DWHIRQ	DWLIRQ
0	000			0	0	0	0	0	0	0	0	0	0	0	0
RW	RW							RW	RW	RW	RW	RW	RW	RW	RW

15	DOWN	0	PWM Count Up
		1	PWM Count Down (in BTB mode)
14 12	IRQCNT[2:0]		Interrupt count number of period match (Interval PRDIRQ mode)
7	PRDIRQ		PWM period interrupt flag (0: no int / 1: int occurred) Write “1” to clear flag
6	BOTIRQ		PWM bottom interrupt flag (0: no int / 1: int occurred) Write “1” to clear flag
5	DUHIRQ		PWM duty UH interrupt flag (0: no int / 1: int occurred) Write “1” to clear flag
4	DULIRQ		PWM duty UL interrupt flag (0: no int / 1: int occurred) Write “1” to clear flag
3	DVHIRQ		PWM duty VH interrupt flag (0: no int / 1: int occurred) Write “1” to clear flag
2	DVLIRQ		PWM duty VL interrupt flag (0: no int / 1: int occurred) Write “1” to clear flag
1	DWHIRQ		PWM duty UH interrupt flag (0: no int / 1: int occurred) Write “1” to clear flag *This flag will be enabled by DUHIEN bit.
0	DWLIRQ		PWM duty WL interrupt flag (0: no int / 1: int occurred) Write “1” to clear flag

AD*n*IER Interrupt Enable Register

ADC interrupt enable register. Individual interrupt sources can be enabled by writing a **1**.

AD0IER=0x4000_B028, AD1IER=0x4000_B128, AD2IER=0x4000_B228,

7	6	5	4	3	2	1	0
			DIEN	TIEN	BIEN	CIEN	SIEN
0	0	0	0	0	0	0	0
			RW	RW	RW	RW	RW

4	DIEN	DMA done interrupt enable 0: interrupt disable 1: interrupt enable
3	TIEN	ADC trigger conversion interrupt enable
2	BIEN	ADC burst conversion interrupt enable
1	CIEN	ADC continuous conversion interrupt enable
0	SIEN	ADC single conversion interrupt enable

AD*n*DDR ADC 0/1/2 DMA Data Register

ADC DMA Data Registers are 16-bit registers.

ADC conversion result register for DMA and single conversion (AD data of just completed conversion)

AD0DDR=0x4000B02C, AD1DDR=0x4000B12C, AD2DDR=0x4000B22C

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDMAR												ADMACH			
0x000												0x0			
R												R			

15 4	ADDMAR	ADC conversion result data (12-bit)
3 0	ADMACH	ADC data channel indicator

CMPDBR Comparator Debounce Register

The Analog Front End Comparator Debounce Register is a 32-bit register.

CMPDBR=0x4000_B330

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								DBNCTB								C3DBNC				C2DBNC				C1DBNC				C0DBNC			
0	0	0	0	0	0	0	0	0x00								0x0				0x0				0x0				0x0			
								RW								RW				RW				RW				RW			

23 16	DBNCTB[3:0]	Debounce time base counter System clock/(DBNCTB *2) becomes shift clock of debounce logic When DBNCTB is 0, system clock would be debounce clock.
15 0	CxDBNC[4:0]	Debounce shift Selection When it is 0x0, debounce function is disable Shift number of debounce logic is (CxDBNC + 1) when CxDBNC is more than 1.

CMPICR Comparator Interrupt Control Register

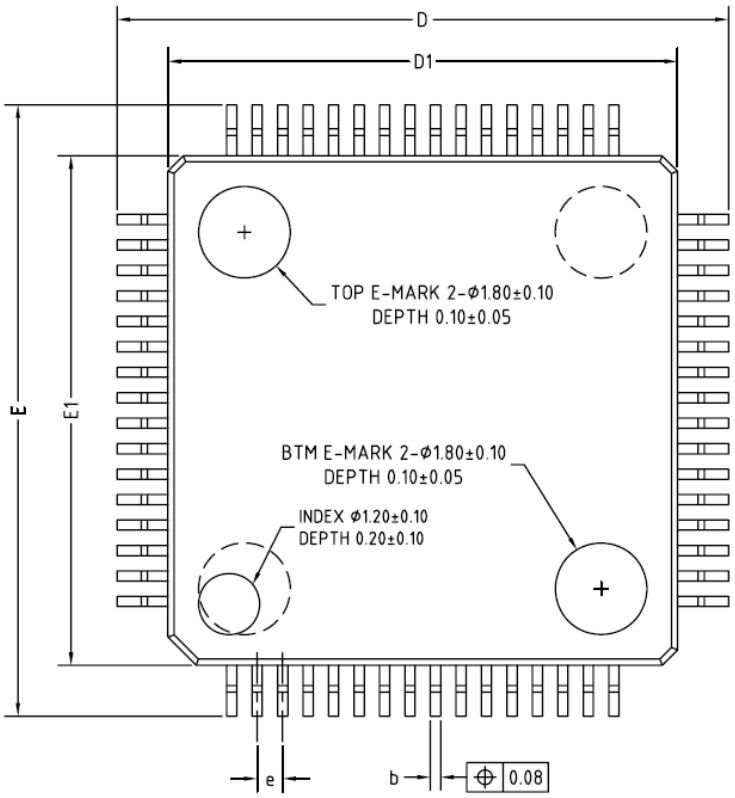
The Analog Front End Comparator Interrupt Control Register is a 16-bit register.

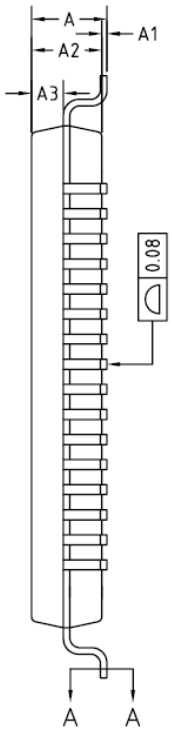
CMPICR=0x4000_B334

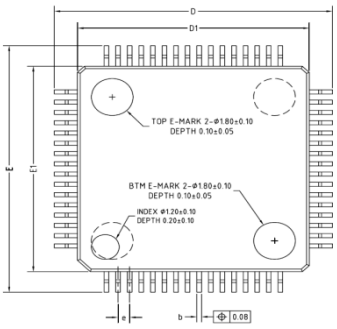
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PPOL3	PPOL2	PPOL1	PPOL0	IPOL3	IPOL2	IPOL1	IPOL0	C3IMOD		C2IMOD		C1IMOD		C0IMOD	
-	-	-	-	-	-	-	-	00		00		00		00	
R	R	R	R	R	R	R	R	RW		RW		RW		RW	

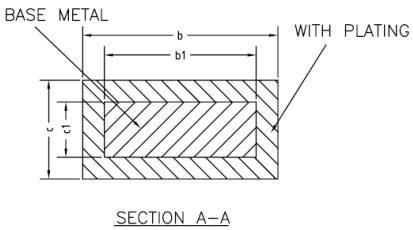
15 14 13 12	PPOL3 PPOL2 PPOL1 PPOL0	0	Comparator outs for PWM protection will not be inverted
		1	Comparator outs for PWM protection will be inverted (if debounce is enable, debounced output will be inverted)
11 10 9 8	IPOL3 IPOL2 IPOL1 IPOL0	0	When comparator output is high, IRQ bit is set (CxIMODE = 00)
		1	When comparator output is low, IRQ bit is set (CxIMODE = 00)
3 2 1 0	C3IMODE C2IMODE C1IMODE C0IMODE	00	Comparator interrupt mode IRQ at level output
		01	IRQ at rising edge of comparator output
		10	IRQ at falling edge of comparator output
		11	IRQ at both edge of comparator output

LQFP-64 Package









SECTION A–A

COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	–	0.27
b1	0.17	0.20	0.23
c	0.13	–	0.18
c1	0.12	0.127	0.134
D	11.80	12.00	12.20
D1	9.90	10.00	10.10
E	11.80	12.00	12.20
E1	9.90	10.00	10.10
e		0.50BSC	
L	0.45	0.60	0.75
L1		1.00REF	
L2		0.25BSC	
R1	0.08	–	–
R2	0.08	–	0.20
S	0.20	–	–
θ	0°	3.5°	7°
θ 1	0°	–	–
θ 2	11°	12°	13°
θ 3	11°	12°	13°

NOTE:
ALL DIMENSIONS REFER TO JEDEC STANDARD MS-026 BDD DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

Figure 19.3. Package Dimension (LQFP-64 10X10)