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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	FlexIO, I²C, IrDA, SPI, UART/USART
Peripherals	DMA, PWM, WDT
Number of I/O	54
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 20x16b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mkl13z32vlh4

Table of Contents

Table 9. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• at 50 °C	—	3.12	4.50		
	• at 70 °C	—	4.96	7.71		
	• at 85 °C	—	7.93	10.75		
	• at 105 °C	—	16.02	22.99		
I_{DD_LLS}	Low-leakage stop mode current with RTC current, at 1.8 V				μA	3
	• at 25 °C and below	—	2.03	2.55		
	• at 50 °C	—	2.81	3.95		
	• at 70 °C	—	4.53	7.30		
	• at 85 °C	—	7.31	10.25		
	• at 105 °C	—	14.93	22.72		
I_{DD_VLLS3}	Very-low-leakage stop mode 3 current, all peripheral disable, at 3.0 V				μA	
	• at 25 °C and below	—	1.16	1.65		
	• at 50 °C	—	1.72	2.65		
	• at 70 °C	—	3.04	5.70		
	• at 85 °C	—	5.21	7.79		
	• at 105 °C	—	11.33	17.63		
I_{DD_VLLS3}	Very-low-leakage stop mode 3 current with RTC current, at 3.0 V				μA	3
	• at 25 °C and below	—	1.83	2.35		
	• at 50 °C	—	2.43	3.39		
	• at 70 °C	—	3.78	5.95		
	• at 85 °C	—	5.98	8.14		
	• at 105 °C	—	12.02	17.89		
I_{DD_VLLS3}	Very-low-leakage stop mode 3 current with RTC current, at 1.8 V				μA	3
	• at 25 °C and below	—	1.58	1.98		
	• at 50 °C	—	2.13	3.17		
	• at 70 °C	—	3.37	5.80		
	• at 85 °C	—	5.4	7.83		
	• at 105 °C	—	10.99	16.86		
I_{DD_VLLS1}	Very-low-leakage stop mode 1 current all peripheral disabled at 3.0 V				μA	
	• at 25 °C and below	—	0.62	1.06		
	• at 50°C	—	0.99	1.43		
	• at 70°C	—	1.88	2.65		
		—	3.41	4.53		

Table continues on the next page...

Table 10. Low power mode peripheral adders — typical value

Symbol	Description	Temperature (°C)						Unit
		-40	25	50	70	85	105	
$I_{IRC8MHz}$	8 MHz internal reference clock (IRC) adder. Measured by entering STOP or VLPS mode with 8 MHz IRC enabled, MCG_SC[FCRDIV]=000b, MCG_MC[LIRC_DIV2]=000b.	85	87	88	88	89	90	µA
$I_{IRC2MHz}$	2 MHz internal reference clock (IRC) adder. Measured by entering STOP mode with the 2 MHz IRC enabled, MCG_SC[FCRDIV]=000b, MCG_MC[LIRC_DIV2]=000b.	28	28	28	28	28	28	µA
$I_{EREFSTEN4MHz}$	External 4 MHz crystal clock adder. Measured by entering STOP or VLPS mode with the crystal enabled.	206	224	230	238	245	253	µA
$I_{EREFSTEN32KHz}$	External 32 kHz crystal clock adder by means of setting the OSC0_CR[EREFSTEN and EREFSTEN] bits to 1 and SIM_SOPT1[OSC32KSEL] to 01. Measured by entering all modes with the crystal enabled. • VLLS1 • VLLS3 • LLS • VLPS • STOP	440 440 490 510 510	490 490 490 560 560	540 540 540 560 560	560 560 560 560 560	570 570 570 610 610	580 580 680 680 680	nA
I_{LPTMR}	LPTMR peripheral adder measured by placing the device in VLLS1 mode with LPTMR enabled using LPO.	30	30	30	85	100	200	nA
I_{CMP}	CMP peripheral adder measured by placing the device in VLLS1 mode with CMP enabled using the 6-bit DAC and a single external input for compare. Includes 6-bit DAC power consumption.	16	16	16	16	16	16	µA
I_{RTC}	RTC peripheral adder measured by placing the device in VLLS1 mode with external 32 kHz crystal enabled by means of the RTC_CR[OSCE] bit and the RTC ALARM set for 1 minute. Includes ERCLK32K (32 kHz external crystal) power consumption.	582	627	638	662	682	760	nA
I_{UART}	UART peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source waiting for RX data at 115200 baud rate.							

Table continues on the next page...

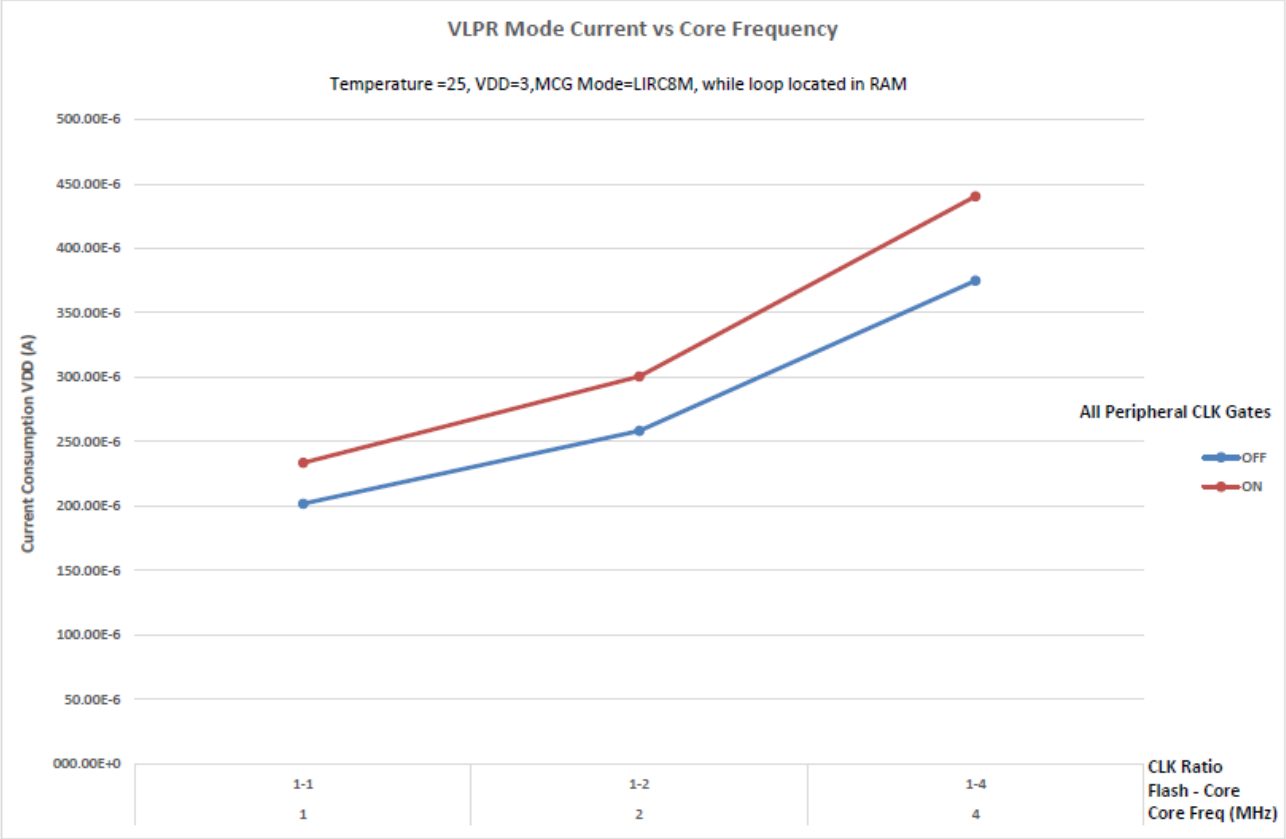


Figure 3. VLPR mode current vs. core frequency

2.2.6 EMC performance

Electromagnetic compatibility (EMC) performance is highly dependent on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components, and MCU software operation play a significant role in the EMC performance. The system designer can consult the following Freescale applications notes, available on freescale.com for advice and guidance specifically targeted at optimizing EMC performance.

- AN2321: Designing for Board Level Electromagnetic Compatibility
- AN1050: Designing for Electromagnetic Compatibility (EMC) with HCMOS Microcontrollers
- AN1263: Designing for Electromagnetic Compatibility with Single-Chip Microcontrollers
- AN2764: Improving the Transient Immunity Performance of Microcontroller-Based Applications

Table 16. SWD full voltage range electricals (continued)

Symbol	Description	Min.	Max.	Unit
	• Serial wire debug	0	25	MHz
J2	SWD_CLK cycle period	1/J1	—	ns
J3	SWD_CLK clock pulse width • Serial wire debug	20	—	ns
J4	SWD_CLK rise and fall times	—	3	ns
J9	SWD_DIO input data setup time to SWD_CLK rise	10	—	ns
J10	SWD_DIO input data hold time after SWD_CLK rise	0	—	ns
J11	SWD_CLK high to SWD_DIO data valid	—	32	ns
J12	SWD_CLK high to SWD_DIO high-Z	5	—	ns

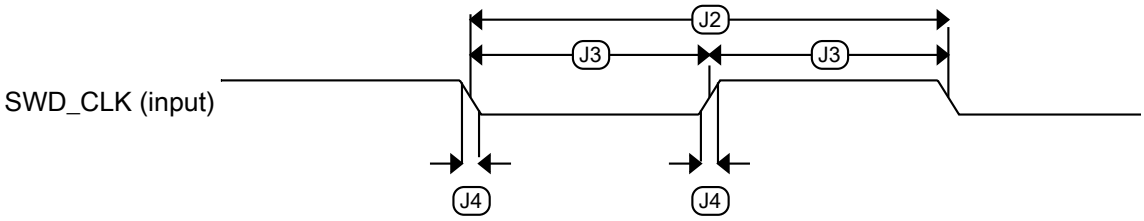


Figure 4. Serial wire clock input timing

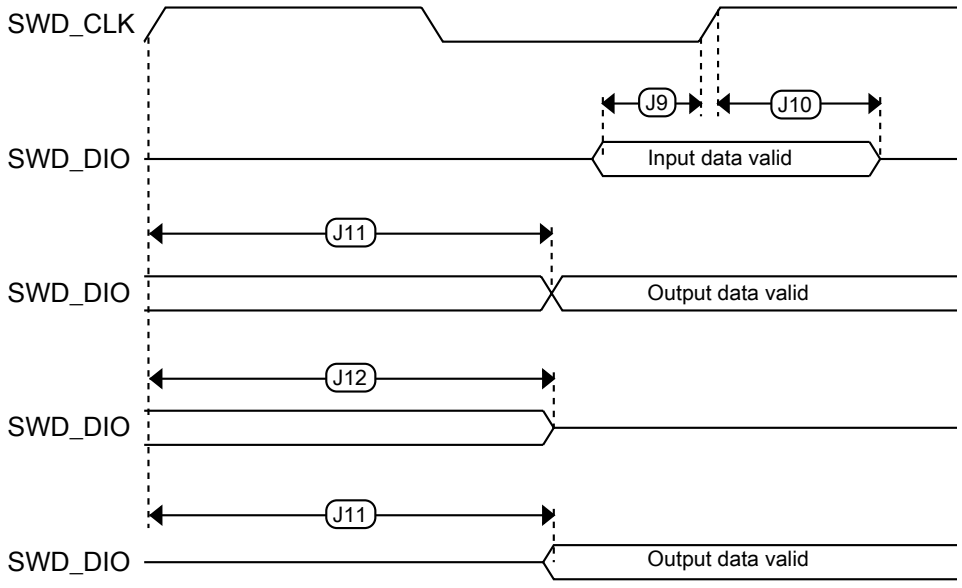


Figure 5. Serial wire data timing

2. Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 2.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
3. The ADC supply current depends on the ADC conversion clock speed, conversion rate and ADC_CFG1[ADLPC] (low power). For lowest power operation, ADC_CFG1[ADLPC] must be set, the ADC_CFG2[ADHSC] bit must be clear with 1 MHz ADC conversion clock speed.
4. 1 LSB = $(V_{REFH} - V_{REFL})/2^N$
5. ADC conversion clock < 16 MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
6. Input data is 100 Hz sine wave. ADC conversion clock < 12 MHz.
7. Input data is 1 kHz sine wave. ADC conversion clock < 12 MHz.
8. ADC conversion clock < 3 MHz

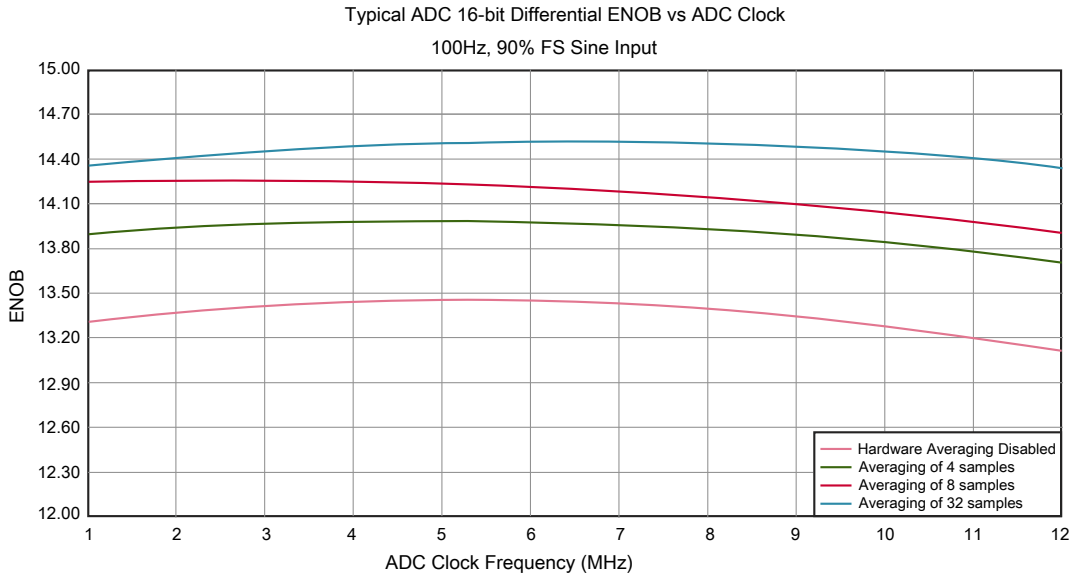


Figure 7. Typical ENOB vs. ADC_CLK for 16-bit differential mode

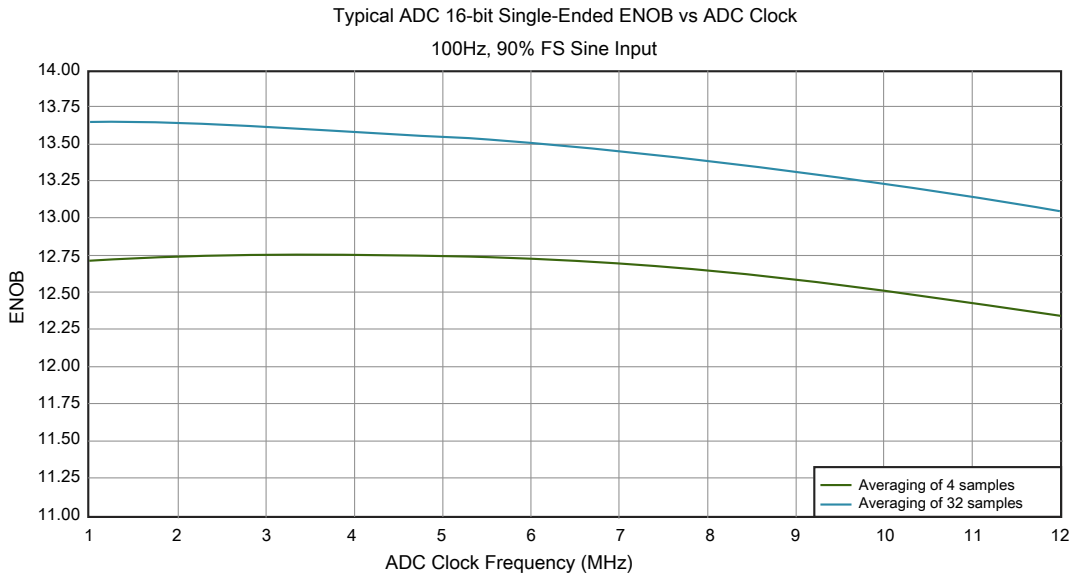


Figure 8. Typical ENOB vs. ADC_CLK for 16-bit single-ended mode

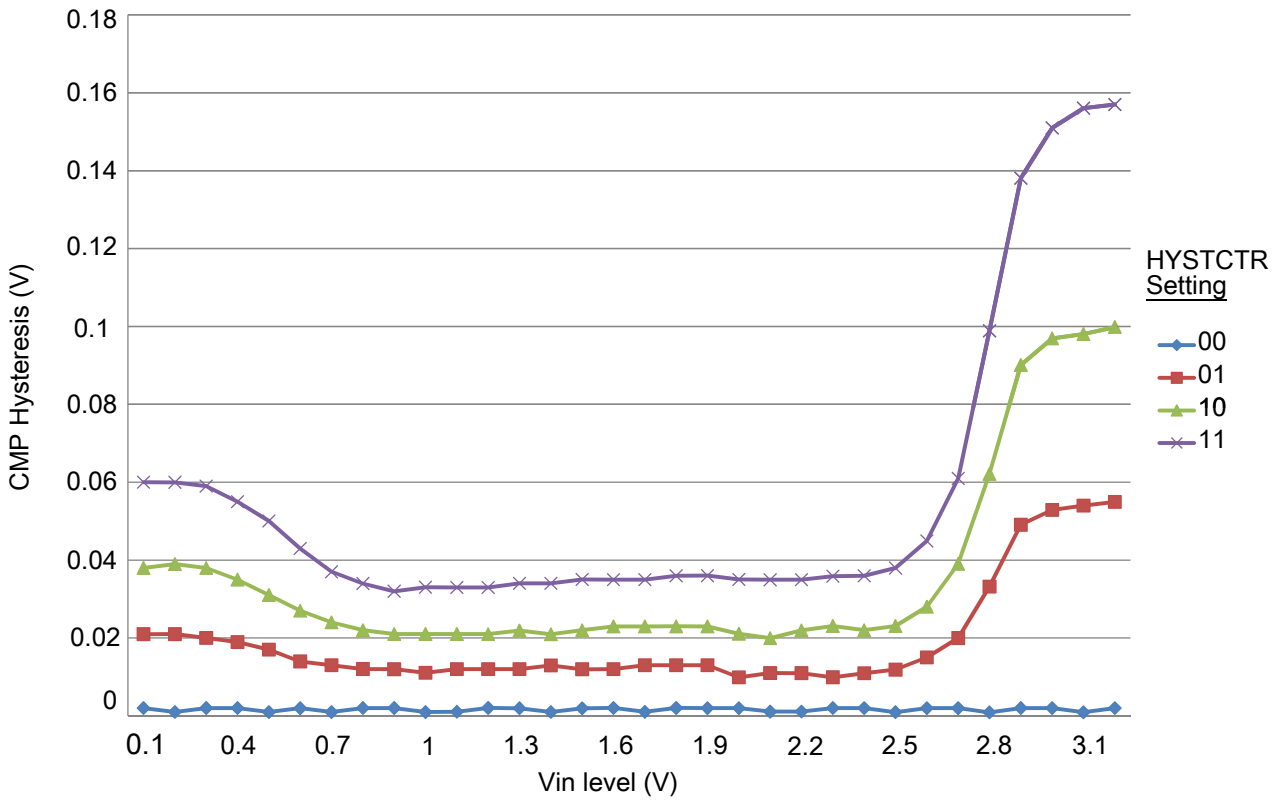


Figure 10. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 1)

3.6.4 12-bit DAC electrical characteristics

3.6.4.1 12-bit DAC operating requirements

Table 32. 12-bit DAC operating requirements

Symbol	Desciption	Min.	Max.	Unit	Notes
V_{DDA}	Supply voltage		3.6	V	
V_{DACR}	Reference voltage	1.13	3.6	V	1
C_L	Output load capacitance	—	100	pF	2
I_L	Output load current	—	1	mA	

1. The DAC reference can be selected to be V_{DDA} or V_{REFH}.
2. A small load capacitance (47 pF) can improve the bandwidth performance of the DAC.

5.1 SPI switching specifications

The Serial Peripheral Interface (SPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic SPI timing modes. See the SPI chapter of the chip's Reference Manual for information about the modified transfer formats used for communicating with slower peripheral devices.

All timing is shown with respect to 20% V_{DD} and 80% V_{DD} thresholds, unless noted, as well as input signal transitions of 3 ns and a 30 pF maximum load on all SPI pins.

Table 34. SPI master mode timing on slew rate disabled pads

Num.	Symbol	Description	Min.	Max.	Unit	Note
1	f_{op}	Frequency of operation	$f_{periph}/2048$	$f_{periph}/2$	Hz	1
2	t_{SPSCK}	SPSCK period	2 x t_{periph}	2048 x t_{periph}	ns	2
3	t_{Lead}	Enable lead time	1/2	—	t_{SPSCK}	—
4	t_{Lag}	Enable lag time	1/2	—	t_{SPSCK}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	t_{periph} - 30	1024 x t_{periph}	ns	—
6	t_{SU}	Data setup time (inputs)	18	—	ns	—
7	t_{HI}	Data hold time (inputs)	0	—	ns	—
8	t_{v}	Data valid (after SPSCK edge)	—	15	ns	—
9	t_{HO}	Data hold time (outputs)	0	—	ns	—
10	t_{RI}	Rise time input	—	t_{periph} - 25	ns	—
	t_{FI}	Fall time input				
11	t_{RO}	Rise time output	—	25	ns	—
	t_{FO}	Fall time output				

1. For SPI0 f_{periph} is the bus clock (f_{BUS}). For SPI1 f_{periph} is the system clock (f_{SYS}).
2. $t_{periph} = 1/f_{periph}$

Table 35. SPI master mode timing on slew rate enabled pads

Num.	Symbol	Description	Min.	Max.	Unit	Note
1	f_{op}	Frequency of operation	$f_{periph}/2048$	$f_{periph}/2$	Hz	1
2	t_{SPSCK}	SPSCK period	2 x t_{periph}	2048 x t_{periph}	ns	2
3	t_{Lead}	Enable lead time	1/2	—	t_{SPSCK}	—
4	t_{Lag}	Enable lag time	1/2	—	t_{SPSCK}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	t_{periph} - 30	1024 x t_{periph}	ns	—
6	t_{SU}	Data setup time (inputs)	96	—	ns	—
7	t_{HI}	Data hold time (inputs)	0	—	ns	—

Table continues on the next page...

Table 37. SPI slave mode timing on slew rate enabled pads

Num.	Symbol	Description	Min.	Max.	Unit	Note
1	f_{op}	Frequency of operation	0	$f_{periph}/4$	Hz	1
2	t_{SPSCK}	SPSCK period	4 x t_{periph}	—	ns	2
3	t_{Lead}	Enable lead time	1	—	t_{periph}	—
4	t_{Lag}	Enable lag time	1	—	t_{periph}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	t_{periph} - 30	—	ns	—
6	t_{SU}	Data setup time (inputs)	2	—	ns	—
7	t_{HI}	Data hold time (inputs)	7	—	ns	—
8	t_a	Slave access time	—	t_{periph}	ns	3
9	t_{dis}	Slave MISO disable time	—	t_{periph}	ns	4
10	t_v	Data valid (after SPSCK edge)	—	130	ns	—
11	t_{HO}	Data hold time (outputs)	0	—	ns	—
12	t_{RI}	Rise time input	—	t_{periph} - 25	ns	—
	t_{FI}	Fall time input				
13	t_{RO}	Rise time output	—	36	ns	—
	t_{FO}	Fall time output				

1. For SPI0 f_{periph} is the bus clock (f_{BUS}). For SPI1 f_{periph} is the system clock (f_{SYS}).
2. $t_{periph} = 1/f_{periph}$
3. Time to data active from high-impedance state
4. Hold time to high-impedance state

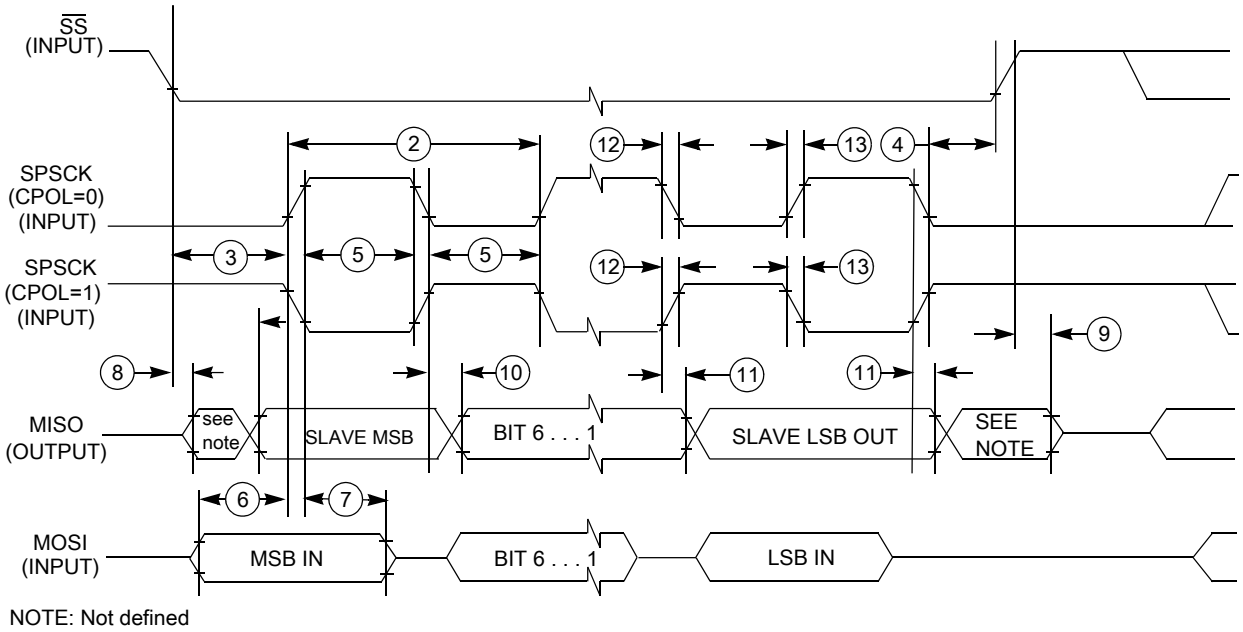
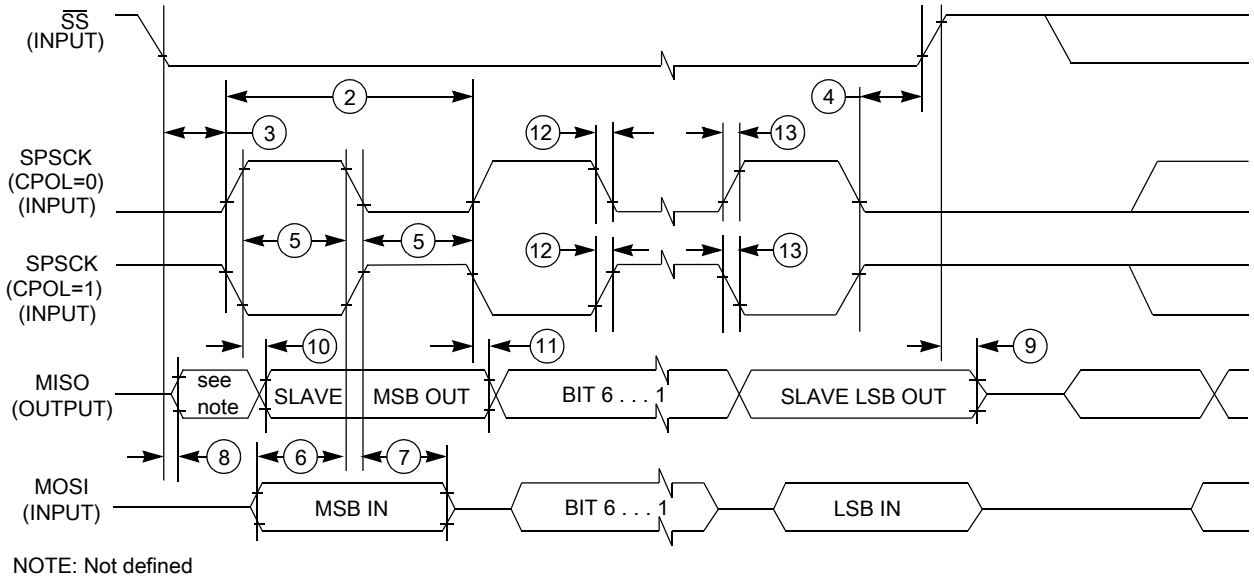


Figure 15. SPI slave mode timing (CPHA = 0)



NOTE: Not defined

Figure 16. SPI slave mode timing (CPHA = 1)

5.2 I²C

5.2.1 Inter-Integrated Circuit Interface (I2C) timing

Table 38. I2C timing

Characteristic	Symbol	Standard Mode		Fast Mode		Unit
		Minimum	Maximum	Minimum	Maximum	
SCL Clock Frequency	f_{SCL}	0	100	0	400[1]	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	t_{HD}; STA	4	—	0.6	—	µs
LOW period of the SCL clock	t_{LOW}	4.7	—	1.25	—	µs
HIGH period of the SCL clock	t_{HIGH}	4	—	0.6	—	µs
Set-up time for a repeated START condition	t_{SU}; STA	4.7	—	0.6	—	µs
Data hold time for I²C bus devices	t_{HD}; DAT	0[2]	3.45[3]	0[4]	0.9[2]	µs
Data set-up time	t_{SU}; DAT	250[5]	—	100[3, 6]	—	ns
Rise time of SDA and SCL signals	t_r	—	1000	20 +0.1C_b[7]	300	ns
Fall time of SDA and SCL signals	t_f	—	300	20 +0.1C_b[6]	300	ns
Set-up time for STOP condition	t_{SU}; STO	4	—	0.6	—	µs
Bus free time between STOP and START condition	t_{BUF}	4.7	—	1.3	—	µs
Pulse width of spikes that must be suppressed by the input filter	t_{SP}	N/A	N/A	0	50	ns

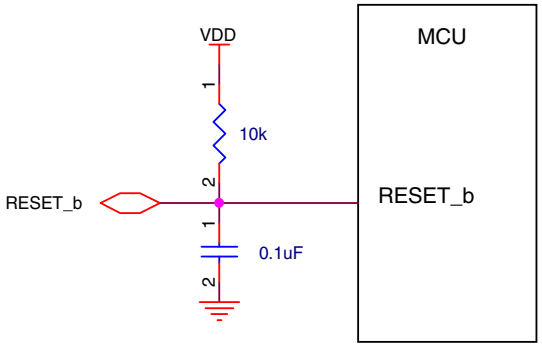


Figure 20. Reset circuit

When an external supervisor chip is connected to the RESET_b pin, a series resistor should be used to avoid damaging the supervisor chip or the RESET_b pin, as shown in Figure 55. The series resistor value (RS below) should be in the range of 100Ω to 1kΩ depending on the external reset chip drive strength. The supervisor chip must have an active high, open-drain output.

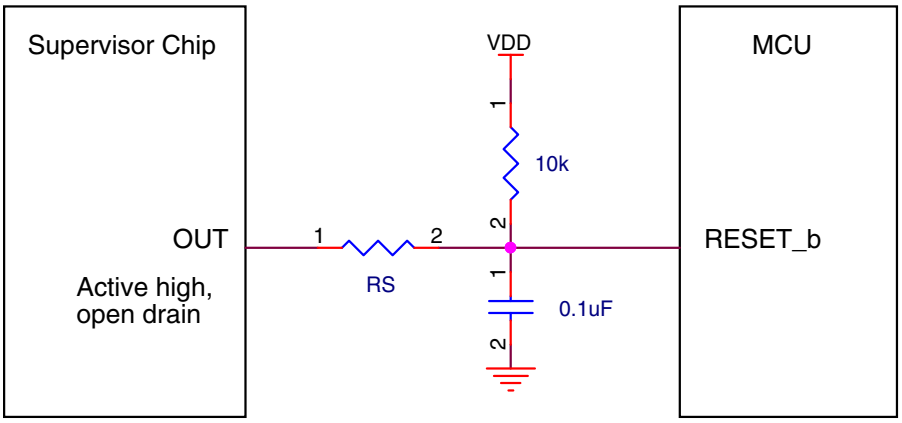


Figure 21. Reset signal connection to external reset chip

- NMI pin

  Because a low level on the NMI_b pin will trigger the Non-maskable interrupt, it is not recommended to add a pull-down resistor or capacitor on this pin. When this pin is enabled as the NMI function an external pull-up resistor (10k) as shown in the following figure is recommended for robustness.

  If the NMI_b pin is used as an I/O pin the Non-maskable interrupt handler is required to disable the NMI function by remapping to another function. The NMI function is disabled by programming the FOPT[NMI_DIS] bit to zero.

- Freescale Freedom Development Platform: http://www.freescale.com/freedom
- Tower System Development Platform: http://www.freescale.com/tower

IDEs for Kinetis MCUs

- Kinetis Design Studio IDE: http://www.freescale.com/kds
- Partner IDEs: http://www.freescale.com/kide

Development Tools

- PEG Graphics Software: http://www.freescale.com/peg
- Processor Expert Software and Embedded Components: http://www.freescale.com/processorexpert)

Run-time Software

- Kinetis SDK: http://www.freescale.com/ksdk
- Kinetis Bootloader: http://www.freescale.com/kboot
- ARM mbed Development Platform: http://www.freescale.com/mbed
- MQX RTOS: http://www.freescale.com/mqx

For all other partner-developed software and tools, visit http://www.freescale.com/partners.

7 Dimensions

7.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to freescale.com and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
32-pin QFN	98ASA00615D
48-pin QFN	98ASA00616D
64-pin LQFP	98ASS23234W
64-pin MAPBGA	98ASA00420D
80-pin LQFP	98ASS23174W

80 LQFP	64 LQFP	48 QFN	64 MAP BGA	32 QFN	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
37	—	—	—	—	PTA17	DISABLED		PTA17	SPI0_MISO			SPI0_MOSI		
38	30	22	G7	15	VDD	VDD	VDD							
39	31	23	H7	16	VSS	VSS	VSS							
40	32	24	H8	17	PTA18	EXTAL0	EXTAL0	PTA18		LPUART1_ RX	TPM_ CLKIN0			
41	33	25	G8	18	PTA19	XTAL0	XTAL0	PTA19		LPUART1_ TX	TPM_ CLKIN1		LPTMR0_ ALT1	
42	34	26	F8	19	PTA20	RESET_b		PTA20						RESET_b
43	35	27	F7	20	PTB0/ LLWU_P5	ADC0_SE8	ADC0_SE8	PTB0/ LLWU_P5	I2C0_SCL	TPM1_CH0	SPI1_MOSI	SPI1_MISO		
44	36	28	F6	21	PTB1	ADC0_SE9	ADC0_SE9	PTB1	I2C0_SDA	TPM1_CH1	SPI1_MISO	SPI1_MOSI		
45	37	29	E7	—	PTB2	ADC0_ SE12	ADC0_ SE12	PTB2	I2C0_SCL	TPM2_CH0				
46	38	30	E8	—	PTB3	ADC0_ SE13	ADC0_ SE13	PTB3	I2C0_SDA	TPM2_CH1				
47	—	—	—	—	PTB8			PTB8	SPI1_PCS0	EXTRG_IN				
48	—	—	—	—	PTB9			PTB9	SPI1_SCK					
49	—	—	—	—	PTB10			PTB10	SPI1_PCS0					
50	—	—	—	—	PTB11			PTB11	SPI1_SCK					
51	39	31	E6	—	PTB16			PTB16	SPI1_MOSI	LPUART0_ RX	TPM_ CLKIN0	SPI1_MISO		
52	40	32	D7	—	PTB17			PTB17	SPI1_MISO	LPUART0_ TX	TPM_ CLKIN1	SPI1_MOSI		
53	41	—	D6	—	PTB18			PTB18		TPM2_CH0				
54	42	—	C7	—	PTB19			PTB19		TPM2_CH1				
55	43	33	D8	—	PTC0	ADC0_ SE14	ADC0_ SE14	PTC0		EXTRG_IN		CMP0_OUT		
56	44	34	C6	22	PTC1/ LLWU_P6/ RTC_CLKIN	ADC0_ SE15	ADC0_ SE15	PTC1/ LLWU_P6/ RTC_CLKIN	I2C1_SCL		TPM0_CH0			
57	45	35	B7	23	PTC2	ADC0_ SE11	ADC0_ SE11	PTC2	I2C1_SDA		TPM0_CH1			
58	46	36	C8	24	PTC3/ LLWU_P7			PTC3/ LLWU_P7	SPI1_SCK	LPUART1_ RX	TPM0_CH2	CLKOUT		
59	47	—	E3	—	VSS	VSS	VSS							
60	48	—	E4	—	VDD	VDD	VDD							
61	49	37	B8	25	PTC4/ LLWU_P8			PTC4/ LLWU_P8	SPI0_PCS0	LPUART1_ TX	TPM0_CH3	SPI1_PCS0		
62	50	38	A8	26	PTC5/ LLWU_P9			PTC5/ LLWU_P9	SPI0_SCK	LPTMR0_ ALT2			CMP0_OUT	
63	51	39	A7	27	PTC6/ LLWU_P10	CMP0_IN0	CMP0_IN0	PTC6/ LLWU_P10	SPI0_MOSI	EXTRG_IN		SPI0_MISO		
64	52	40	B6	28	PTC7	CMP0_IN1	CMP0_IN1	PTC7	SPI0_MISO			SPI0_MOSI		

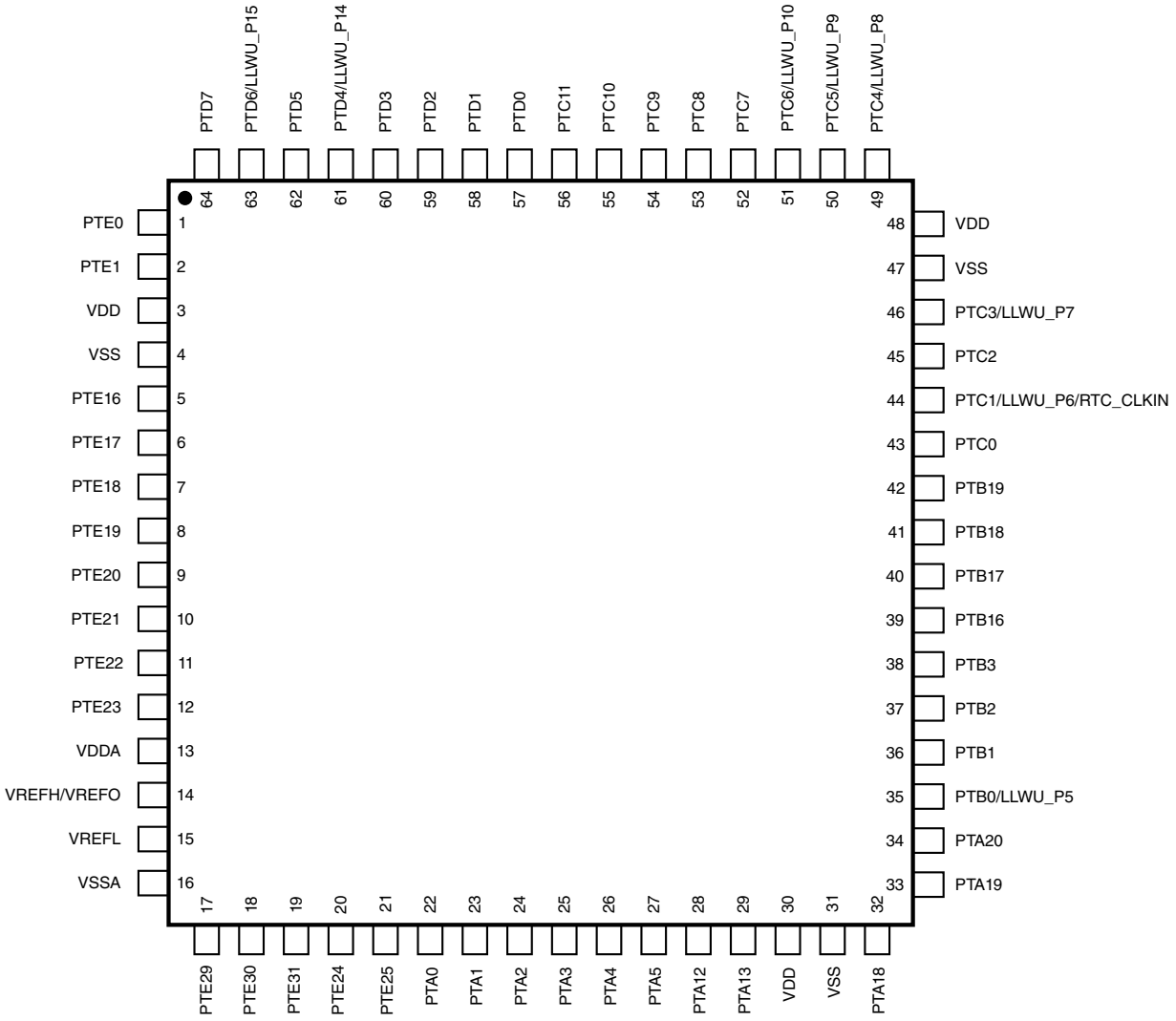


Figure 28. 64 LQFP Pinout diagram

Figure below shows the 80 LQFP pinouts:

	1	2	3	4	5	6	7	8	
A	PTE0	PTD7	PTD4/ LLWU_P14	PTD1	PTC11	PTC8	PTC6/ LLWU_P10	PTC5/ LLWU_P9	A
B	PTE1	PTD6/ LLWU_P15	PTD3	PTC10	PTC9	PTC7	PTC2	PTC4/ LLWU_P8	B
C	PTD5	PTD2	PTD0	VSS	NC	PTC1/ LLWU_P6/ RTC_CLKIN	PTB19	PTC3/ LLWU_P7	C
D	PTE17	PTE19	PTA0	PTA1	PTA3	PTB18	PTB17	PTC0	D
E	PTE16	PTE18	VSS	VDD	PTA2	PTB16	PTB2	PTB3	E
F	PTE21	PTE23	VSSA	VDDA	PTA5	PTB1	PTB0/ LLWU_P5	PTA20	F
G	PTE20	PTE22	VREFL	VREFH/ VREFO	PTA4	PTA13	VDD	PTA19	G
H	PTE29	PTE30	PTE31	PTE24	PTE25	PTA12	VSS	PTA18	H
	1	2	3	4	5	6	7	8	

Figure 30. 64 MAPBGA Pinout diagram

Figure below shows the 48 QFN pinouts:

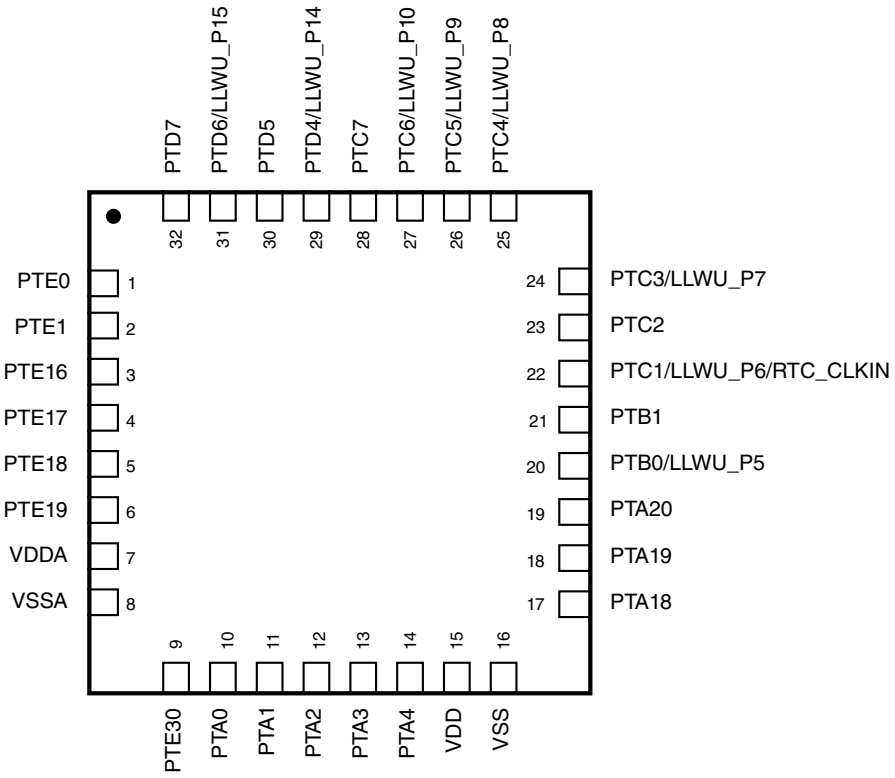


Figure 32. 32 QFN Pinout diagram

9 Ordering parts

9.1 Determining valid orderable parts

Valid orderable part numbers are provided on the Web. To determine the orderable part numbers for this device, go to freescale.com and perform a part number search for the following device numbers:

10 Part identification

10.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

10.2 Format

Part numbers for this device have the following format:

Q KL## A FFF R T PP CC N

10.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Table 41. Part number fields description

Field	Description	Values
Q	Qualification status	• M = Fully qualified, general market flow • P = Prequalification
KL##	Kinetis family	• KL13
A	Key attribute	• Z = Cortex-M0+
FFF	Program flash memory size	• 32 = 32 KB • 64 = 64 KB
R	Silicon revision	• (Blank) = Main • A = Revision after main
T	Temperature range (°C)	• V = –40 to 105
PP	Package identifier	• FM = 32 QFN (5 mm x 5 mm) [1] • FT = 48 QFN (7 mm x 7 mm)[1,] • LH = 64 LQFP (10 mm x 10 mm) • MP = 64 MAPBGA (5 mm x 5 mm)[1] • LK = 80 LQFP (12 mm x 12 mm)
CC	Maximum CPU frequency (MHz)	• 4 = 48 MHz
N	Packaging type	• R = Tape and reel

1. This package for this product is not yet available. However, it is included in Package Your Way program for Kinetis MCUs. Visit freescale.com/KPYW for more details.

10.4 Example

This is an example part number:

MKL13Z32VLH4

11 Terminology and guidelines

11.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

11.1.1 Example

This is an example of an operating requirement:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	0.9	1.1	V

11.2 Definition: Operating behavior

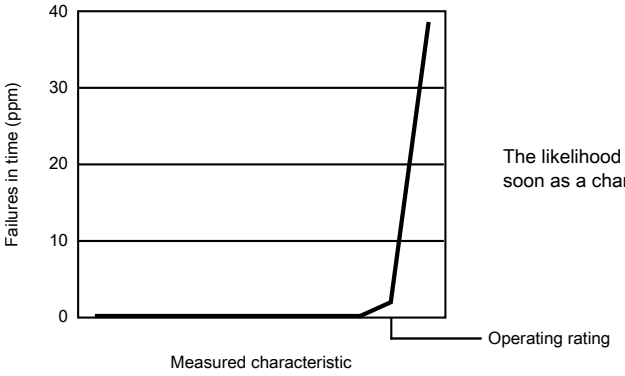
Unless otherwise specified, an *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

11.2.1 Example

This is an example of an operating behavior:

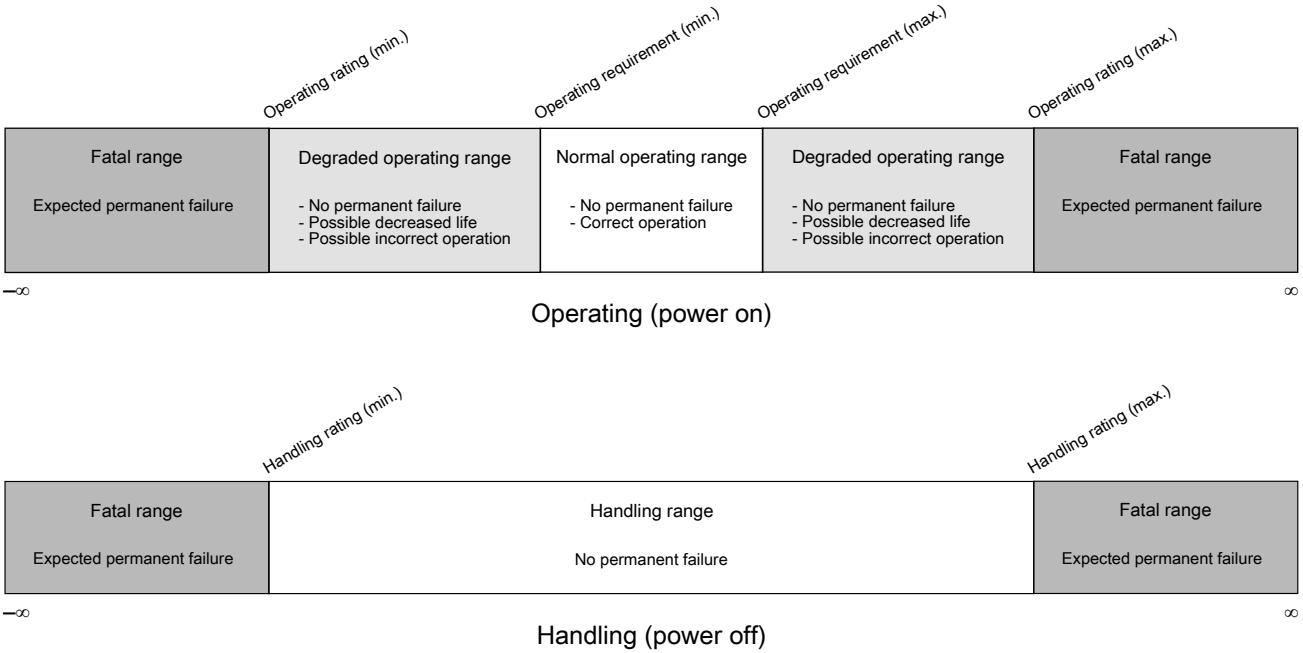
Symbol	Description	Min.	Max.	Unit
I_{WP}	Digital I/O weak pullup/ pulldown current	10	130	µA

11.5 Result of exceeding a rating



The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.

11.6 Relationship between ratings and operating requirements



11.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

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