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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	-
Core Size	8-Bit
Speed	20MHz
Connectivity	EBI/EMI, UART/USART
Peripherals	DMA, WDT
Number of I/O	32
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	-
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	68-LCC (J-Lead)
Supplier Device Package	68-PLCC (24.21x24.21)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/ia88c00plc68ir1

Data Sheet Contents

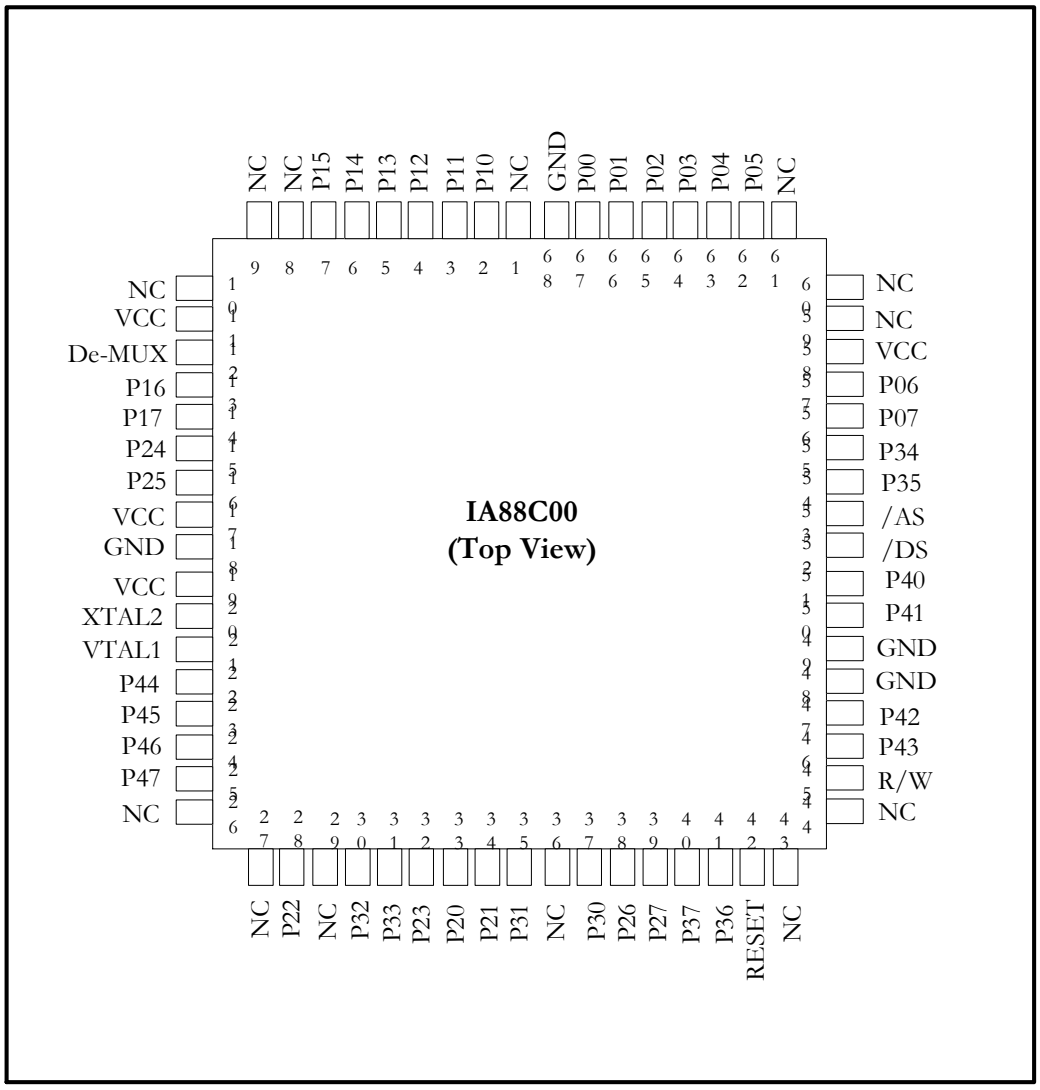

Figure 4. 68-Lead PLCC Package

67	NC	Not Connected	Input/Output
68	GND	Ground	Input

1. High order bit of the 4-bit address selects one of the two register pointers (0 selects RP0; 1 selects RP1).
2. Live high order bits in the register pointer select an 8-register (contiguous) slice of the register space.
3. Three low order bits of the 4-bit address select one of the eight registers in the slice.

The process results in linking together the five bits from the register pointer to the three bits from the address to form an 8-bit address. The three bits from the address will always point to an address within the same eight registers, as long as the address in the register pointer remains unchanged.

Changing the five high bits in control registers R214 for RP9 and R215 for RP1 allows the register pointers to be moved.

Using full 8-bit addressing allows the working registers to be accessed. The lower nibble is used similarly to the 4-bit addressing described above when an 8-bit logical address in the range 192 to 207 (C0 to CF) is specified. This is shown in section b. of Figure 8.

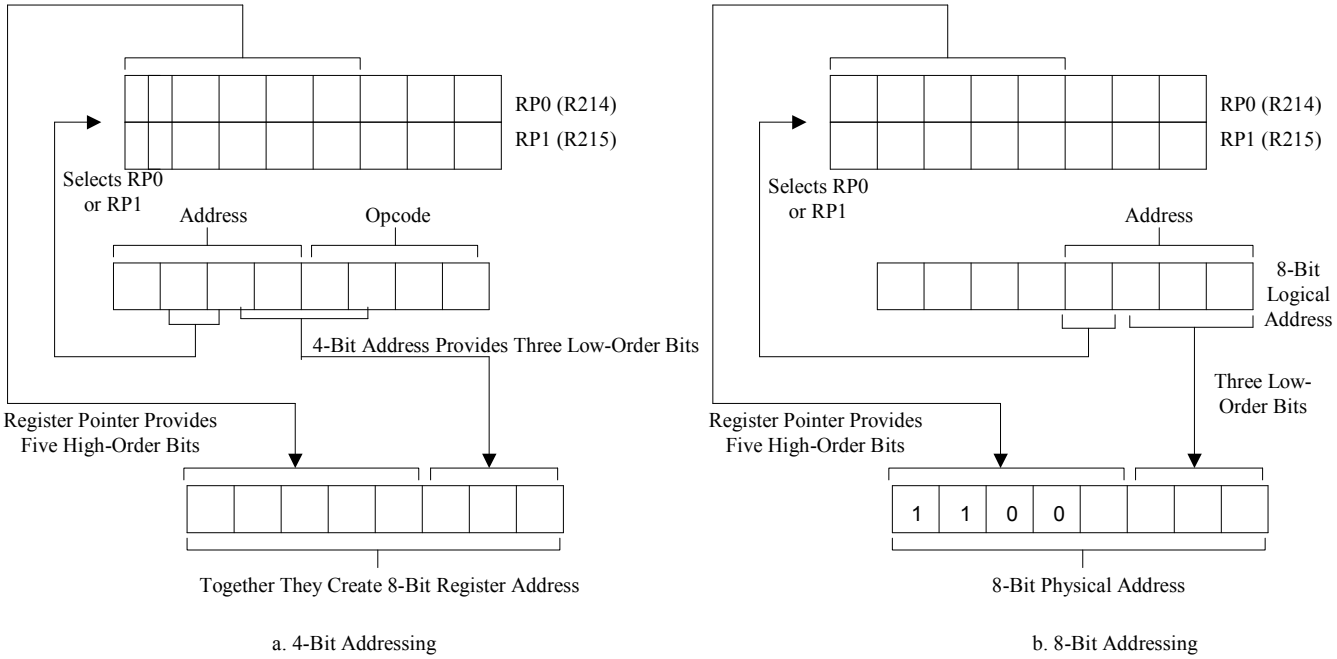

Figure 8. Working Register Window

Physical registers 192 to 207 can be accessed only when selected by a register pointer. This is because any direct access to logical addresses 192 to 207 involves the register pointers. After a reset, RP0 points to R192 and RP1 points to R200.

Figure 15. Instruction Pointer High (IPH), R218

Bit	7	6	5	4	3	2	1	0
	IP15	IP14	IP13	IP12	IP11	IP10	IP9	IPO8
Initial Value	?	?	?	?	?	?	?	?
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

A special register called the Instruction Pointer (IP) provides hardware support for threaded-code languages. It consists of register-pair R218-R219 and contains memory addresses. The MSB is R218. Threaded-code languages deal with an imaginary higher-level machine within the existing hardware machine. The IP acts like the PC for that machine. The command NEXT passes control to or from the hardware machine to the imaginary machine. And the commands ENTER and EXIT are imaginary machine equivalents of real machine CALLS and RETURNS.

If the commands NEXT, ENTER and EXIT are not used, the IP can be used by the fast interrupt processing, as described in the interrupts section.

Figure 16. Instruction Pointer Low (IPL), R219

Bit	7	6	5	4	3	2	1	0
	IP7	IP6	IP5	IP4	IP3	IP2	IP1	IP0
Initial Value	?	?	?	?	?	?	?	?
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

A special register called the Instruction Pointer (IP) provides hardware support for threaded-code languages. This register consists of register pair R218-R219 and contains memory addresses. The MSB is R218. Threaded-code languages deal with an imaginary higher-level machine within the existing hardware machine. The IP acts like the PC for that machine. The command NEXT passes control to or from the hardware machine to the imaginary machine. And the commands ENTER and EXIT are imaginary machine equivalents of real machine CALLS and RETURNS.

The IP can be used by the fast interrupt processing, as described in the interrupts section, if the commands NEXT, ENTER and EXIT are not used.

Figure 17. Interrupt Mask (IRM), R221

Bit	7	6	5	4	3	2	1	0
	Level 7	Level 7	Level 7	Level 7	Level 7	Level 7	Level 7	Level 7
Initial Value	?	?	?	?	?	?	?	?
Read/Write	R	R	R	R	R	R	R	R

Figure 20. Counter 0 Control Register (C0CT), R224 Bank 0

Bit	7	6	5	4	3	2	1	0
	D7	D6	D5	D4	D3	D2	D1	D0
Initial Value	X	X	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

D0 - When this bit is set to 1, the counter/timer is enabled. Operation begins on the rising edge of the first processor clock period following the setting of this bit from a previously cleared value. Writing a 1 in this field when the previous value was 1 has no effect on the operation of the counter/timer. When this bit is cleared to 0, the counter/timer performs no operation during the next (and subsequent) processor clock periods. A hardware reset forces this bit to 0.

Both counters are clocked by the rising edge of the incoming signal on P26 or p36 after the counter is enabled. The maximum frequency of the external clock signal applied to P36 (or P26) equals the maximum Xtal frequency divided by 4. The maximum gauaranteed Xtal frequency is 20 MHz, which implies a maximum counter frequency of 5 MHz.

D1 - Reset/End of Count Status - This bit is set to 1 each time the counter reaches 0. Writing a 1 to this bit resets it, while writing a 0 has no effect.

D2 - Zero Count Interrupt Enable - When this bit is set to 1, the counter/timer generates an interrupt request when it counts to 0. A hardware reset forces this bit to 0.

D3 - Software Capture - When this bit is set to 1, the current counter value is loaded into the capture register. This bit is automatically cleared following the capture.

D4 - Software Trigger - This bit is effectively "ORed" with the external rising-edge trigger input and can be used by the software to force a trigger signal. This bit produces a trigger signal regardless of the setting of the Input Pin Assignment field of the Mode register. This bit is automatically cleared following the trigger.

D5 - Load Counter - The contents of the Time Constant register are transferred to the Counter prescaler one clock period after this bit is set. This operation alone does not start the counter. This bit is automatically cleared following the load.

D6 - Count Up/Down - This bit determines the count direction if internal up/down control is specified in the Mode register. 1 indicates up; 0 indicates down.

D7 - Continuous/Single Cycle - When this bit is set to 1, the counter is reloaded with the time-constant value when the counter reaches the end of the terminal count. The terminal count for down counting is 0000, while the one for up counting is FFFF. When this bit is cleared to 0, no reloading occurs.

Figure 21. Counter 0 Mode, R224

Bit	7	6	5	4	3	2	1	0
	D7	D6	D5	D4	D3	D2	D1	D0
Initial Value	X	X	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

D0 - When this bit is set to 1, the counter/timer is enabled. Operation begins on the rising edge of the first processor clock period following the setting of this bit from a previously cleared value. Writing a 1 in this field when the previous value was 1 has no effect on the operation of the counter/timer. When this bit is cleared to 0, the counter/timer performs no operation during the next (and subsequent) processor clock periods. A hardware reset forces this bit to 0.

Both counters are clocked by the rising edge of the incoming signal on P26 or p36 after the counter is enabled. The maximum frequency of the external clock signal applied to P36 (or P26) equals the maximum Xtal frequency divided by 4. The maximum gauaranteed Xtal frequency is 20 MHz, which implies a maximum counter frequency of 5 MHz.

D1 - Reset/End of Count Status - This bit is set to 1 each time the counter reaches 0. Writing a 1 to this bit resets it, while writing a 0 has no effect.

D2 - Zero Count Interrupt Enable - When this bit is set to 1, the counter/timer generates an interrupt request when it counts to 0. A hardware reset forces this bit to 0.

D3 - Software Capture - When this bit is set to 1, the current counter value is loaded into the capture register. This bit is automatically cleared following the capture.

D4 - Software Trigger - This bit is effectively "ORed" with the external rising-edge trigger input and can be used by the software to force a trigger signal. This bit produces a trigger signal regardless of the setting of the Input Pin Assignment field of the Mode register. This bit is automatically cleared following the trigger.

D5 - Load Counter - The contents of the Time Constant register are transferred to the Counter prescaler one clock period after this bit is set. This operation alone does not start the counter. This bit is automatically cleared following the load.

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D7 - Continuous/Single Cycle - When this bit is set to 1, the counter is reloaded with the time-constant value when the counter reaches the end of the terminal count. The terminal count for down counting is 0000, while the one for up counting is FFFF. When this bit is cleared to 0, no reloading occurs.

Figure 28b. Watch Dog Timer and Stop Mode Recovery Register (WDT/SMR) R230 Bank0

Bit	7	6	5	4	3	2	1	0
	D7	D6	D5	D4	D3	D2	D1	D0
	WDT time-out		WDT Enable	WDT in Stop	WDT Source	SMR On	SMR Source	
Initial Value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

This register controls the Watchdog Timer time-out and Stop recovery mode.

D1, D0 Stop Mode Recovery source select.
Bit D0 and D1 determine the Stop Mode Recovery source.

D1	D0	
0	0	Recovery from RESET only
0	1	Recovery from P22 and RESET
1	0	Recovery from P32 and RESET
1	1	Recovery from any input for Port 4 and RESET

A hardware reset forces D0 and D1 to zero.

D2 Stop Recovery Edge
A 1 in this position indicates that a rising edge on any one of the recovery sources wakes the IA88C00 from Stop mode. A 0 indicates falling edge recovery. The reset value is 0.

D3 XTAL1/RC Select for WDT
When a zero is written to D3, the clock of the WDT is driven by the on-board RC oscillator. If D3 is set to 1, the WDT is driven by XTAL1. D3 has a zero reset value.

D4 WDT Enable During STOP or HALT
When this bit is set, WDT is enabled during STOP or HALT. In this case, recovery from STOP or HALT should be performed before the selected time-out. A 0 in this bit location disables the WDT while the IA88C00 is stopped or halted. A hardware reset forces this bit to a zero.

D5 WDT
The Watch-Dog Timer is initially enabled by writing a 1 to D5 and retriggered on subsequent writings to the same bit. Reset value = 0. Writing a 0 to this bit has no effect. Once a 1 is written to D5, it persists until a hardware reset occurs.

D6, D7 WDT Time-Out
Two sets of four different time-out values can be selected, depending on the logical state of these bits. A normal reset signal must be active low during 5 XTAL clock periods. Using the reset signal input to recover from STOP mode requires 10 XTAL clock periods. This is so that XTAL oscillation starts up and stabilizes, generating a good oscillator output level.

The reset pin is held low in source during WDT timer time-out to accomplish a system reset with other peripherals of the Super8. When the reset pin is held low, the capability of sink current via the reset pin should be considered. (See DC Characteristics.)

Figure 29. UART Transmit Control (UTC), R235 Bank 0

Bit	7	6	5	4	3	2	1	0
	D7	D6	D5	D4	D3	D2	D1	D0
Initial Value	0	0	0	0	0	0	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

This register cont ains the status and command bits needed to control the transmit sections of the UART.

0 - TDMAENB - Transmit DMA Enable - When this bit is set to 1, the DMA function for the UART transmit section is enabled. If this bit is set and the Transmit Buffer Empty signal becomes true, a DMA request is made. When the DMA channel gains control of the bus, it transfers bytes from the external memory or the register file to the UART transmit section. A hardware reset forces this bit to 0.

D1 - TBE - Transmit Buffer Empty - This status bit is set to 1 whenever the transmit buffer is empty. It is cleared to 0 when a data byte is written in the transmit buffer. A hardware reset forces this bit to 1.

D2 - ZC - Zero Count - This status bit is set to 1 and latched when the counter in the baud-rate generator reaches the count of 0. This bit can be cleared to 0 by writing a 1 to this bit position. A hardware reset forces this bit to 0.

D3 - TENB - Transmit Enable - Data is not transmitted until this bit is set to 1. When cleared to 0, the Transmit Data pin continuously outputs 1s unless Auto-Echo mode is selected. This bit should be cleared only after the desired transmission of data in the buffer is completed. A hardware reset forces this bit to 0.

D4 - REIE - Receive Error Interrupt Enable - If this bit is set to 1, any receiver error condition will cause an interrupt request. Possible receive error conditions include parity error, overrun error and framing error.

D5 - BRKIE - Break Interrupt Enable - If this bit is set to 1, a transition in either direction on the break signal will cause an interrupt request.

D6 - CCIE - Control Character Interrupt Enable - If this bit is set to 1, an ASCII Control Character Detect signal in the URC register will cause an interrupt.

D7 - WUIE - Wake-Up Interrupt Enable - If this bit is set to 1, any of the wake-up conditions that set the Wake-Up Detect bit (WUD) in the URC register will cause an interrupt request.

Figure 32. UART Transmit Interrupt Register, UTI R238 Bank 0

Bit	7	6	5	4	3	2	1	0
	D7	D6	D5	D4	D3	D2	D1	D0
Initial Value	0	0	0	0	0	0	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/O	R/W

The timing for the transmit buffer empty interrupt is software programmable. There are two different interrupt timings selectable with 1 bit.

Option 1: Interrupt is activated at the moment the contents of the TUIO register are transferred to the Tx FIFO.

Option 2: Interrupt is activated at the moment the last stop bit in the Tx FIFO is sent.

After loading the transmit shift register, UART control generates a buffer empty flag to indicate that TUIO is ready to be filled with new data.

A new flag will indicate when the transmit shift register is empty.

D0 - If this bit is zero, a high value of D2 in the UIE register will cause an interrupt on Transmit UIO empty. If this bit is set, a high value of D2 in the UIE register will cause an interrupt on transmit shift register empty. That is when the last stop bit is transmitted. This bit should be programmed prior to writing to the UIO register.

D1 - This flag is set when the transmit shift register is empty and is reset when a new value is loaded into the UIO. This flag will not be set during a send break.

Figure 33. Uart Data Register (UIO), R239 Bank 0

Bit	7	6	5	4	3	2	1	0
	D7	D6	D5	D4	D3	D2	D1	D0
Initial Value	X	X	X	X	X	X	X	X
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/O	R/W

Writing to this register automatically writes the data in the Transmit Data register (UIOT). A read from this register gets the data from the UART Receive Data register (UIOR).

D0 - Handshake Enable - When this bit is set to 1, the handshake function is enabled.

D1 - Port Select - This bit selects which port is controlled by Handshake Channel 0. When it is set to 1, Port 1 is selected and when it is cleared to 0, Port 4 is selected.

D2 - DMA Enable - When this bit is set to 1, the DMA function is enabled for Handshake Channel 0. When it is cleared to 0, the DMA function is not used by the handshake channel and may be used by the UART.

D3 - Mode - When this bit is set to 1, the "fully interlocked" mode is enabled. When it is cleared to 0, the "strobed" mode is enabled.

D4-D7 - Deskew Counter - This 4-bit field is used to select a count value from 1 to 16 (0000-1111). This value is the number of processor clocks used to generate the set-up and strobe when using the "strobed" mode, or the set-up when using the "fully-interlocked" mode.

Figure 37. Handshake 1 Control (H1C), R245 Bank 0

Bit	7	6	5	4	3	2	1	0
	D7	D6	D5	D4	D3	D2	D1	D0
Initial Value	X	X	X	X	X	X	X	0
Read/Write	W/O	W/O	W/O	W/O	W/O	W/O	W/O	W/O

This register controls Handshake Channel 1.

D0 - Handshake Enable - When this bit is set to 1, the handshake function is enabled.

D1 - Not Used.

D2 - Not Used.

D3 - Mode - When this bit is set to 1, the "fully interlocked" mode is enabled. When it is cleared to 0, the "strobed" mode is enabled.

D4-D7 - Deskew Counter - This 4-bit field is used to select a count value from 1 to 16 (0000-1111). This value is the number of processor clocks used to generate the set-up and strobe when using the "strobed" mode, or the set-up when using the "fully-interlocked" mode.

Figure 38. Port 4 Direction Control Register (P4D), R246 Bank 0

Bit	7	6	5	4	3	2	1	0
	D7	D6	D5	D4	D3	D2	D1	D0
Initial Value	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Figure 42. Port 2/3 B Mode Register, R249 Bank 0

Bit	7	6	5	4	3	2	1	0
	D7	D6	D5	D4	D3	D2	D1	D0
Initial Value	0	0	0	0	0	0	0	0
Read/Write	W/O	W/O	W/O	W/O	W/O	W/O	W/O	W/O

The Port 2/3 A Mode, Port 2/3 B Mode, Port 2/3 C Mode and Port 2/3 D Mode registers control the modes of Ports 2 and 3. A separate 2-bit field for each of the bits of Ports 2 and 3 configures the bit as input or output. The field also controls whether the bit is enabled as an external interrupt source and selects the oputpus as open-drain or push-pull.

Figure 43. Port 2/3 C Mode Register, R250 Bank 0

Bit	7	6	5	4	3	2	1	0
	D7	D6	D5	D4	D3	D2	D1	D0
Initial Value	0	0	0	0	0	0	0	0
Read/Write	W/O	W/O	W/O	W/O	W/O	W/O	W/O	W/O

The Port 2/3 A Mode, Port 2/3 B Mode, Port 2/3 C Mode and Port 2/3 D Mode registers control the modes of Ports 2 and 3. A separate 2-bit field for each of the bits of Ports 2 and 3 configures the bit as input or output. The field also controls whether the bit is enabled as an external interrupt source and selects the oputpus as open-drain or push-pull.

Figure 44. Port 2/3 D Mode Register, R251 Bank 0

Bit	7	6	5	4	3	2	1	0
	D7	D6	D5	D4	D3	D2	D1	D0
Initial Value	0	0	0	0	0	0	0	0
Read/Write	W/O	W/O	W/O	W/O	W/O	W/O	W/O	W/O

The Port 2/3 A Mode, Port 2/3 B Mode, Port 2/3 C Mode and Port 2/3 D Mode registers control the modes of Ports 2 and 3. A separate 2-bit field for each of the bits of Ports 2 and 3 configures the bit as input or output. The field also controls whether the bit is enabled as an external interrupt source and selects the oputpus as open-drain or push-pull.

Instruction Summary

This section provides a summary of the IA88C00 instructions.

NOTE

Assignment of a value is indicated by the symbol "←".

For example:

Dst ← dst + src

indicates that the source data is added to the destination data and the result is stored in the destination location.

The notation "addr (n) " is used to refer to bit (n) of a given operand location.

For example:

dst (7)

refers to bit 7 of the destination operand.

Figure 49. Instruction Summary

Instruction and Operation	Address Mode dst scr		Opcode Byte (Hex)	Flags Affected C	Z	S	V	D	H
ADC dst, src dst←dst + src + C	†		1[ ]	*	*	*	-	0	*
ADD dst, src dst←dst + src	†		0[ ]	*	*	*	*	0	*
ADD dst, src dst←dst AND src	†		5[ ]	-	*	*	0	-	-
BAND dst, src dst←dst AND src	r0 Rb	Rb r0	67 67	-	*	0	U	-	-
BCP dst, src dst - src	r0	Rb	17	-	*	0	U	-	-
BITC dst dst←NOT dst	rb		57	-	*	0	U	-	-
BITR dst dst←0	rb	77	-	-	-	-	-	-	-

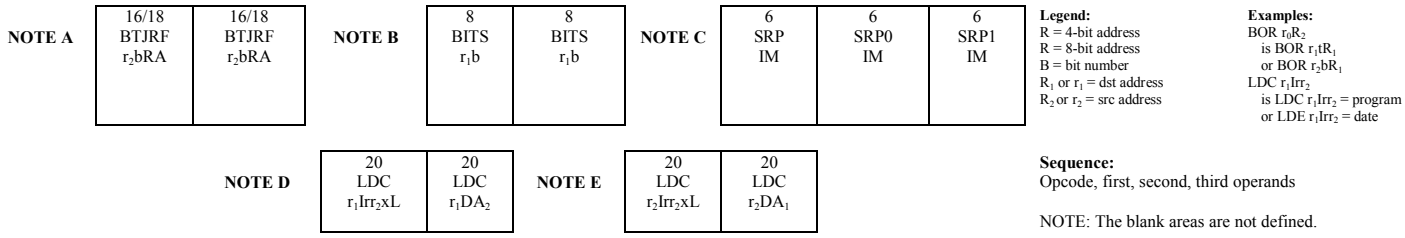
dst←dst
XOR src

† These instructions have an identical set of addressing modes, which are encoded for brevity. The first opcode nibble is found in the instruction set table above. The second nibble is expressed symbolically by a '[ ]' in this table. Its value is found in the following table to the left of the applicable addressing mode pair.

For example, the opcode of an ADC instruction using the addressing modes r (destination) and ir (source) is 13.

Address dst	Mode src	Lower Opcode Nibble
r	r	[2]
r	Ir	[3]
R	R	[4]
R	IR	[5]
R	IM	[6]

Notes:
0 = Cleared to Zero
1 = Set to One
– = Unaffected
* = Set or reset, depending on result of operation.
U = Undefined



Instructions

Figure 51. Load Instructions

Mnemonic	Operands	Instructions
CLR	dst	Clear
LD	dst, src	Load
LDB	dst, src	Load bit
LDC	dst, src	Load program memory
LDE	dst, src	Load data memory
LDCD	dst, src	Load program memory and decrement
LDED	dst, src	Load data memory and decrement
LDCI	dst, src	Load program memory and increment
LDEI	dst, src	Load data memory and increment
LDCPD	dst, src	Load program memory with pre-decrement
LDEPD	dst, src	Load data memory with pre-decrement
LDCPI	dst, src	Load program memory with pre-increment
LDEPI	dst, src	Load data memory with pre-increment
LDW	dst, src	Load word
POP	dst	Pop stack
POPUD	dst, src	Pop user stack (decrement)
POPUI	dst, src	Pop user stack (increment)
PUSH	src	Push stack
PUSHUD	dst, src	Push user stack (decrement)
PUSHUI	dst, src	Push user stack (increment)

Figure 52. Arithmetic Instructions

Mnemonic	Operands	Instructions
ADC	dst, src	Add with carry
ADD	dst, src	Add
CP	dst, src	Compare
DA	dst	Decimal adjust
DEC	dst	Decrement
DECW	dst	Decrement word
DIV	dst, src	Divide
INC	dst	Increment

INCW	dst	Increment word
MULT	dst, src	Multiply
SBC	dst, src	Subtract with carry
SUB	dst, src	Subtract

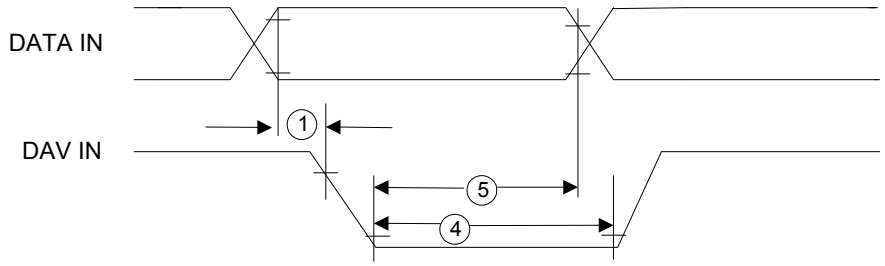


Figure 69. Strobed Mode (Input Handshake)

AC Electrical Characteristics

Input Handshake

No.	Symbol	Parameter	Min	Max	Notes*†
1	TsDI(DAV)	Data In to Setup Time	0		
2	TdDAVlf(RDY)	/DAV Fall Input to RDY Fall Delay		200	1
3	ThDI(RDY)	Data In Hold Time from RDY Fall	0		
4	TwDAV	/DAV In Width	45		
5	ThD(DAV)	Data In Hold Time from /DAV Fall	130		
6	TdDAV(RDY)	/DAV Rise Input to RDY Rise Delay		100	2
7	TdRDYf(DAV)	RDY Rise Output to /DAV Rise Delay	0		

NOTES
1. Standard Test Load
2. This time assumes user program reads data before /DAV Input goes High. RDY will not go high before data is read.

* Times are given in nanoseconds.
† Times are preliminary and subject to change.

Output Handshake Timing

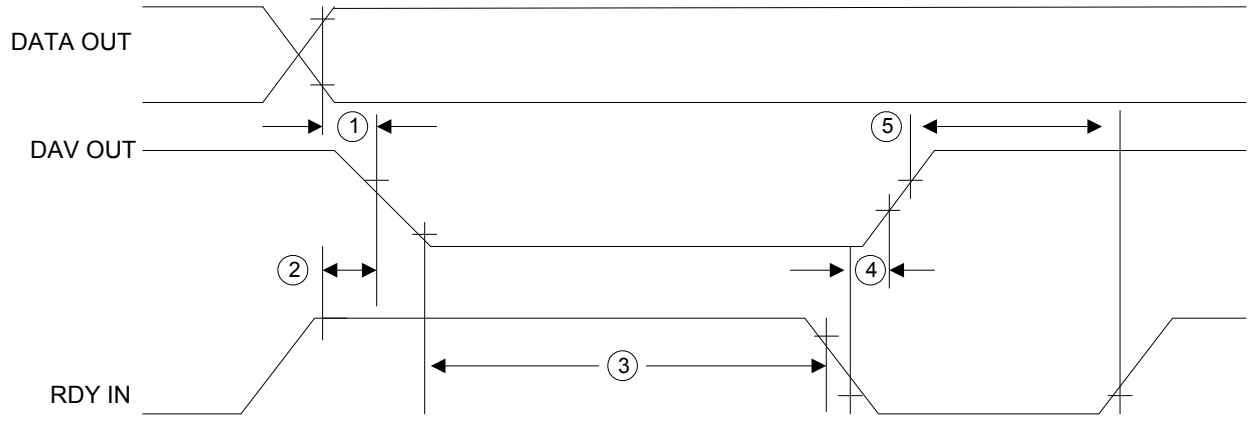


Figure 70. Fully Interlocked Mode (Output Handshake)

Ordering Information

Innovasic Semiconductor® Part Number	Package Type	Temperature Grades
IA88C00-PDW48C (standard packaging) **IA88C00-PDW48I** (standard packaging) **IA88C00-PDW48C-R** (RoHS packaging) **IA88C00-PDW48I-R** (RoHS packaging)	48-Pin Plastic Dual In-line Package (DIP)	Commercial Industrial Commercial Industrial
IA88C00-PLC68C (standard packaging) **IA88C00-PLC68I** (standard packaging) **IA88C00-PLC68C-R** (RoHS packaging) **IA88C00-PLC68I-R** (RoHS packaging)	68-Pin Plastic Leaded Chip Carrier (PLCC)	Commercial Industrial Commercial Industrial