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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M4 |
| Core Size | 32-Bit Single-Core |
| Speed | 120MHz |
| Connectivity | CANbus, I²C, SPI, UART/USART, USB OTG |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, LVD, POR, PWM, WDT |
| Number of I/O | 40 |
| Program Memory Size | 128KB (128K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 64K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.71V ~ 3.6V |
| Data Converters | A/D 1x16b; D/A 1x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-LQFP |
| Supplier Device Package | 64-LQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mks20fn128vlh12 |

### 2.1.8 Power management

The Power Management Controller (PMC) expands upon ARM's operational modes of Run, Sleep, and Deep Sleep, to provide multiple configurable modes. These modes can be used to optimize current consumption for a wide range of applications. The WFI or WFE instruction invokes a Wait or a Stop mode, depending on the current configuration. For more information on ARM's operational modes, See the ARM® Cortex® User Guide.

The PMC provides High Speed Run (HSRUN), Normal Run (RUN), and Very Low Power Run (VLPR) configurations in ARM's Run operation mode. In these modes, the MCU core is active and can access all peripherals. The difference between the modes is the maximum clock frequency of the system and therefore the power consumption. The configuration that matches the power versus performance requirements of the application can be selected.

The PMC provides Wait (Wait) and Very Low Power Wait (VLPW) configurations in ARM's Sleep operation mode. In these modes, even though the MCU core is inactive, all of the peripherals can be enabled and operate as programmed. The difference between the modes is the maximum clock frequency of the system and therefore the power consumption.

The PMC provides Stop (Stop), Very Low Power Stop (VLPS), Low Leakage Stop (LLS), and Very Low Leakage Stop (VLLS) configurations in ARM's Deep Sleep operational mode. In these modes, the MCU core and most of the peripherals are disabled. Depending on the requirements of the application, different portions of the analog, logic, and memory can be retained or disabled to conserve power.

The Battery Backup mode allows the VBAT voltage domain to operate while the rest of the device is disabled to conserve power. All modules in the VBAT domain are functional in this mode of operation.

The Nested Vectored Interrupt Controller (NVIC), the Asynchronous Wake-up Interrupt Controller (AWIC), and the Low Leakage Wake-Up Controller (LLWU) are used to wake up the MCU from low power states. The NVIC is used to wake up the MCU core from WAIT and VLPW modes. The AWIC is used to wake up the MCU core from STOP and VLPS modes. The LLWU is used to wake up the MCU core from LLS and VLLSx modes.

For additional information regarding operational modes, power management, the NVIC, AWIC, or the LLWU, please refer to the Reference Manual.

- USB 1.1 and 2.0 compliant full-speed device controller
- 16 bidirectional end points
- DMA or FIFO data stream interfaces
- Low-power consumption
- IRC48M with clock-recovery is supported to eliminate the 48 MHz crystal. It is used for USB device-only implementation.

### 2.2.17 I2S

The I2S module provides a synchronous audio interface (SAI), which can be clocked by bus clock, PLL/FLL output clock or external oscillator clock. The module supports asynchronous bit clocks (BCLKs) that can be generated internally from the audio master clock or supplied externally. And also supports the option for synchronous operation between the receiver and transmitter. And it can be functional in stop or very low power mode.

I2S module has the following features:

- Transmitter with independent bit clock and frame sync supporting 1 data channel
- Receiver with independent bit clock and frame sync supporting 1 data channel
- Maximum frame size of 16 words
- Word size of between 8-bits and 32-bits
- Word size configured separately for first word and remaining words in frame
- Asynchronous 8 × 32-bit FIFO for each transmit and receive channels
- Supports graceful restart after FIFO error
- Supports automatic restart after FIFO error without software intervention
- Supports packing of 8-bit and 16-bit data into each 32-bit FIFO word

### 2.2.18 FlexIO

The FlexIO is a highly configurable module providing a wide range of protocols including, but not limited to UART, I2C, SPI, I2S, and PWM/Waveform generation. The module supports programmable baud rates independent of bus clock frequency, with automatic start/stop bit generation.

The FlexIO module has the following features:

- Functional in VLPR/VLPW/Stop/VLPS mode provided the clock it is using remains enabled
- Four 32-bit double buffered shift registers with transmit, receive, and data match modes, and continuous data transfer

| 100 LQFP | 64 LQFP | 48 QFN | Pin Name | Default | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 21 | 12 | — | ADC0_DM3 | ADC0_DM3 | ADC0_DM3 | | | | | | | |
| 22 | 13 | 12 | VDDA | VDDA | VDDA | | | | | | | |
| 23 | 14 | 12 | VREFH | VREFH | VREFH | | | | | | | |
| 24 | 15 | 13 | VREFL | VREFL | VREFL | | | | | | | |
| 25 | 16 | 13 | VSSA | VSSA | VSSA | | | | | | | |
| 26 | 17 | — | CMP0_IN5 | CMP0_IN5 | CMP0_IN5 | | | | | | | |
| 27 | 18 | — | DAC0_OUT/ ADC0_SE23 | DAC0_OUT/ ADC0_SE23 | DAC0_OUT/ ADC0_SE23 | | | | | | | |
| 28 | 19 | 14 | XTAL32 | XTAL32 | XTAL32 | | | | | | | |
| 29 | 20 | 15 | EXTAL32 | EXTAL32 | EXTAL32 | | | | | | | |
| 30 | 21 | 16 | VBAT | VBAT | VBAT | | | | | | | |
| 31 | — | — | PTE24 | ADC0_SE17 | ADC0_SE17 | PTE24 | CAN1_TX | TPM0_CH0 | I2S1_TX_FS | LPI2C0_SCL | EWM_OUT_b | |
| 32 | — | — | PTE25 | ADC0_SE18 | ADC0_SE18 | PTE25 | CAN1_RX | TPM0_CH1 | I2S1_TX_ BCLK | LPI2C0_SDA | EWM_IN | |
| 33 | — | — | PTE26/ CLKOUT32K | DISABLED | | PTE26/ CLKOUT32K | | | I2S1_TXD0 | | RTC_ CLKOUT | USB_CLKIN |
| 34 | 22 | 17 | PTA0 | JTAG_TCLK/ SWD_CLK | | PTA0 | UART0_ CTS_b | TPM0_CH5 | | EWM_IN | | JTAG_TCLK/ SWD_CLK |
| 35 | 23 | 18 | PTA1 | JTAG_TDI | | PTA1 | UART0_RX | | CMP0_OUT | LPI2C1_ HREQ | TPM1_CH1 | JTAG_TDI |
| 36 | 24 | 19 | PTA2 | JTAG_TDO/ TRACE_ SWO | | PTA2 | UART0_TX | | | | TPM1_CH0 | JTAG_TDO/ TRACE_ SWO |
| 37 | 25 | 20 | PTA3 | JTAG_TMS/ SWD_DIO | | PTA3 | UART0_ RTS_b | TPM0_CH0 | | EWM_OUT_b | | JTAG_TMS/ SWD_DIO |
| 38 | 26 | 21 | PTA4/ LLWU_P3 | NMI_b | | PTA4/ LLWU_P3 | | TPM0_CH1 | | | I2S0_MCLK | NMI_b |
| 39 | 27 | — | PTA5 | DISABLED | | PTA5 | USB_CLKIN | TPM0_CH2 | | | I2S0_TX_ BCLK | JTAG_TRST_ b |
| 40 | — | — | VDD | VDD | VDD | | | | | | | |
| 41 | — | — | VSS | VSS | VSS | | | | | | | |
| 42 | 28 | — | PTA12 | DISABLED | | PTA12 | CAN0_TX | TPM1_CH0 | | | I2S0_TXD0 | |
| 43 | 29 | — | PTA13/ LLWU_P4 | DISABLED | | PTA13/ LLWU_P4 | CAN0_RX | TPM1_CH1 | | | I2S0_TX_FS | |
| 44 | — | — | PTA14 | DISABLED | | PTA14 | SPI0_PCS0 | UART0_TX | | | I2S0_RX_ BCLK | |
| 45 | — | — | PTA15 | DISABLED | | PTA15 | SPI0_SCK | UART0_RX | | | I2S0_RXD0 | |
| 46 | — | — | PTA16 | DISABLED | | PTA16 | SPI0_SOUT | UART0_ CTS_b | | | I2S0_RX_FS | |
| 47 | — | — | PTA17 | DISABLED | | PTA17 | SPI0_SIN | UART0_ RTS_b | | | I2S0_MCLK | |
| 48 | 30 | 22 | VDD | VDD | VDD | | | | | | | |
| 49 | 31 | 23 | VSS | VSS | VSS | | | | | | | |
| 50 | 32 | 24 | PTA18 | EXTAL0 | EXTAL0 | PTA18 | | | TPM_CLKIN0 | | | |

| 100LQFP | 64LQFP | 48QFN | Pin Name | Driver Strength | Default Status after POR | Pull-up/ pull-down Setting after POR | Slew Rate after POR | Passive Pin Filter after POR | Open Drain | Pin Interrupt |
|---|---|---|---|---|---|---|---|---|---|---|
| 20 | 11 | | ADC0_DP3 | - | Hi-Z | - | - | - | - | - |
| 21 | 12 | | ADC0_DM3 | - | Hi-Z | - | - | - | - | - |
| 22 | 13 | 12 | VDDA | - | - | - | - | - | - | - |
| 23 | 14 | 12 | VREFH | - | Hi-Z | - | - | - | - | - |
| 24 | 15 | 13 | VREFL | - | Hi-Z | - | - | - | - | - |
| 25 | 16 | 13 | VSSA | - | Hi-Z | - | - | - | - | - |
| 26 | 17 | | CMP0_IN5 | - | Hi-Z | - | - | - | - | - |
| 27 | 18 | | DAC0_OUT/ ADC0_SE23 | - | Hi-Z | - | - | - | - | - |
| 28 | 19 | 14 | XTAL32 | - | Hi-Z | - | - | - | - | - |
| 29 | 20 | 15 | EXTAL32 | - | Hi-Z | - | - | - | - | - |
| 30 | 21 | 16 | VBAT | - | - | - | - | - | - | - |
| 31 | | | PTE24 | ND | Hi-Z | - | FS | N | N | Y |
| 32 | | | PTE25 | ND | Hi-Z | - | FS | N | N | Y |
| 33 | | | PTE26/ CLKOUT32K | ND | Hi-Z | - | FS | N | N | Y |
| 34 | 22 | 17 | PTA0 | ND | L | PD | FS | N | N | Y |
| 35 | 23 | 18 | PTA1 | ND | H | PU | FS | N | N | Y |
| 36 | 24 | 19 | PTA2 | ND | H | PU | FS | N | N | Y |
| 37 | 25 | 20 | PTA3 | ND | H | PU | FS | N | N | Y |
| 38 | 26 | 21 | PTA4/ LLWU_P3 | ND | H | PU | FS | N | N | Y |
| 39 | 27 | | PTA5 | ND | Hi-Z | - | FS | N | N | Y |
| 40 | | | VDD | - | - | - | - | - | - | - |
| 41 | | | VSS | - | - | - | - | - | - | - |
| 42 | 28 | | PTA12 | ND | Hi-Z | - | FS | N | N | Y |
| 43 | 29 | | PTA13/ LLWU_P4 | ND | Hi-Z | - | FS | N | N | Y |
| 44 | | | PTA14 | ND | Hi-Z | - | FS | N | N | Y |
| 45 | | | PTA15 | ND | Hi-Z | - | FS | N | N | Y |
| 46 | | | PTA16 | ND | Hi-Z | - | FS | N | N | Y |

*Table continues on the next page...*

| 100LQFP | 64LQFP | 48QFN | Pin Name | Driver Strength | Default Status after POR | Pull-up/ pull-down Setting after POR | Slew Rate after POR | Passive Pin Filter after POR | Open Drain | Pin Interrupt |
|---|---|---|---|---|---|---|---|---|---|---|
| 100 | 64 | 48 | PTD7 | HD | Hi-Z | - | FS | N | N | Y |

| Properties | Abbreviation | Descriptions |
|---|---|---|
| Driver strength | ND | Normal drive |
| | HD | High drive |
| Default status after POR | Hi-Z | High impendence |
| | H | High level |
| | L | Low level |
| Pull-up/pull-down setting after POR | PU | Pull-up |
| | PD | Pull-down |
| Slew rate after POR | FS | Fast slew rate |
| | SS | Slow slew rate |
| Passive Pin Filter after POR | N | Disabled |
| | Y | Enabled |
| Open drain | N | Disabled[1] |
| | Y | Enabled |
| Pin interrupt | Y | Yes |

1. When UART or LPUART module is enabled and a pin is functional for UART or LPUART, this pin is (pseudo-) open drain configurable.

## 4.3 Module Signal Description Tables

The following sections correlate the chip-level signal name with the signal name used in the module's chapter. They also briefly describe the signal function and direction.

### 4.3.1 Core Modules

**Table 9. JTAG Signal Descriptions**

| Chip signal name | Module signal name | Description | I/O |
|---|---|---|---|
| JTAG_TMS | JTAG_TMS/ SWD_DIO | JTAG Test Mode Selection | I |

*Table continues on the next page...*

**Table 9. JTAG Signal Descriptions (continued)**

| Chip signal name | Module signal name | Description | I/O |
|---|---|---|---|
| JTAG_TCLK | JTAG_TCLK/ SWD_CLK | JTAG Test Clock | I |
| JTAG_TDI | JTAG_TDI | JTAG Test Data Input | I |
| JTAG_TDO | JTAG_TDO/ TRACE_SWO | JTAG Test Data Output | O |
| JTAG_TRST | JTAG_TRST_b | JTAG Reset | I |

**Table 10. SWD Signal Descriptions**

| Chip signal name | Module signal name | Description | I/O |
|---|---|---|---|
| SWD_DIO | JTAG_TMS/ SWD_DIO | Serial Wire Data | I |
| SWD_CLK | JTAG_TCLK/ SWD_CLK | Serial Wire Clock | I |

**Table 11. TPIU Signal Descriptions**

| Chip signal name | Module signal name | Description | I/O |
|---|---|---|---|
| TRACE_SWO | JTAG_TDO/ TRACE_SWO | Trace output data from the ARM CoreSight debug block over a single pin | O |

## 4.3.2 System Modules

**Table 12. EWM Signal Descriptions**

| Chip signal name | Module signal name | Description | I/O |
|---|---|---|---|
| EWM_IN | EWM_in | EWM input for safety status of external safety circuits. The polarity of EWM_in is programmable using the EWM_CTRL[ASSIN] bit. The default polarity is active-low. | I |
| $\overline{\text{EWM\_OUT}}$ | $\overline{\text{EWM\_out}}$ | EWM reset out signal | O |

## Table 26. CAN 1 (for KS22 only) Signal Descriptions

| Chip signal name | Module signal name | Description | I/O |
|---|---|---|---|
| CAN1_RX | CAN Rx | CAN Receive Pin | Input |
| CAN1_TX | CAN Tx | CAN Transmit Pin | Output |

## Table 27. SPI 0 Signal Descriptions

| Chip signal name | Module signal name | Description | I/O |
|---|---|---|---|
| SPI0_PCS0 | PCS0/$\overline{SS}$ | Peripheral Chip Select 0 (O) | I/O |
| SPI0_PCS[3:1] | PCS[1:3] | Peripheral Chip Selects 1–3 | O |
| SPI0_PCS4 | PCS4 | Peripheral Chip Select 4 | O |
| SPI0_PCS5 | PCS5/ $\overline{PCSS}$ | Peripheral Chip Select 5 /Peripheral Chip Select Strobe | O |
| SPI0_SIN | SIN | Serial Data In | I |
| SPI0_SOUT | SOUT | Serial Data Out | O |
| SPI0_SCK | SCK | Serial Clock (O) | I/O |

## Table 28. SPI 1 Signal Descriptions

| Chip signal name | Module signal name | Description | I/O |
|---|---|---|---|
| SPI1_PCS0 | PCS0/$\overline{SS}$ | Peripheral Chip Select 0 (O) | I/O |
| SPI1_PCS[3:1] | PCS[1:3] | Peripheral Chip Selects 1–3 | O |
| SPI1_SIN | SIN | Serial Data In | I |
| SPI1_SOUT | SOUT | Serial Data Out | O |
| SPI1_SCK | SCK | Serial Clock (O) | I/O |

## Table 29. LPI$^2$C 0 Signal Descriptions

| Chip signal name | Module signal name | Description | I/O |
|---|---|---|---|
| LPI2C0_SCL | SCL | LPI2C clock line. | I/O |
| LPI2C0_SDA | SDA | LPI2C data line. | I/O |
| LPI2C0_HREQ | HREQ | Host request, can initiate an LPI2C master transfer if asserted and the I2C bus is idle. | I |
| LPI2C0_SCLS | SCLS | Secondary I2C clock line. If LPI2C master/slave are configured to use separate pins, this the LPI2C slave SCL pin. | I/O |
| LPI2C0_SDAS | SDAS | Secondary I2C data line. If LPI2C master/slave are configured to use separate pins, this the LPI2C slave SDA pin. | I/O |

## Table 34. UART 2 Signal Descriptions

| Chip signal name | Module signal name | Description | I/O |
|---|---|---|---|
| UART2_CTS | CTS | Clear to send | I |
| UART2_RTS | RTS | Request to send | O |
| UART2_TX | TXD | Transmit data | O |
| UART2_RX | RXD | Receive data | I |

## Table 35. I²S0 Signal Descriptions

| Chip signal name | Module signal name | Description | I/O |
|---|---|---|---|
| I2S0_MCLK | SAI_MCLK | Audio Master Clock. The master clock is an input when externally generated and an output when internally generated. | I/O |
| I2S0_RX_BCLK | SAI_RX_BCLK | Receive Bit Clock. The bit clock is an input when externally generated and an output when internally generated. | I/O |
| I2S0_RX_FS | SAI_RX_SYNC | Receive Frame Sync. The frame sync is an input sampled synchronously by the bit clock when externally generated and an output generated synchronously by the bit clock when internally generated. | I/O |
| I2S0_RXD | SAI_RX_DATA | Receive Data. The receive data is sampled synchronously by the bit clock. | I |
| I2S0_TX_BCLK | SAI_TX_BCLK | Transmit Bit Clock. The bit clock is an input when externally generated and an output when internally generated. | I/O |
| I2S0_TX_FS | SAI_TX_SYNC | Transmit Frame Sync. The frame sync is an input sampled synchronously by the bit clock when externally generated and an output generated synchronously by the bit clock when internally generated. | I/O |
| I2S0_TXD | SAI_TX_DATA | Transmit Data. The transmit data is generated synchronously by the bit clock and is tristated whenever not transmitting a word. | O |

## Table 36. I²S1 Signal Descriptions

| Chip signal name | Module signal name | Description | I/O |
|---|---|---|---|
| I2S1_MCLK | SAI_MCLK | Audio Master Clock. The master clock is an input when externally generated and an output when internally generated. | I/O |
| I2S1_RX_BCLK | SAI_RX_BCLK | Receive Bit Clock. The bit clock is an input when externally generated and an output when internally generated. | I/O |
| I2S1_RX_FS | SAI_RX_SYNC | Receive Frame Sync. The frame sync is an input sampled synchronously by the bit clock when externally generated and an output generated synchronously by the bit clock when internally generated. | I/O |
| I2S1_RXD | SAI_RX_DATA | Receive Data. The receive data is sampled synchronously by the bit clock. | I |

*Table continues on the next page...*

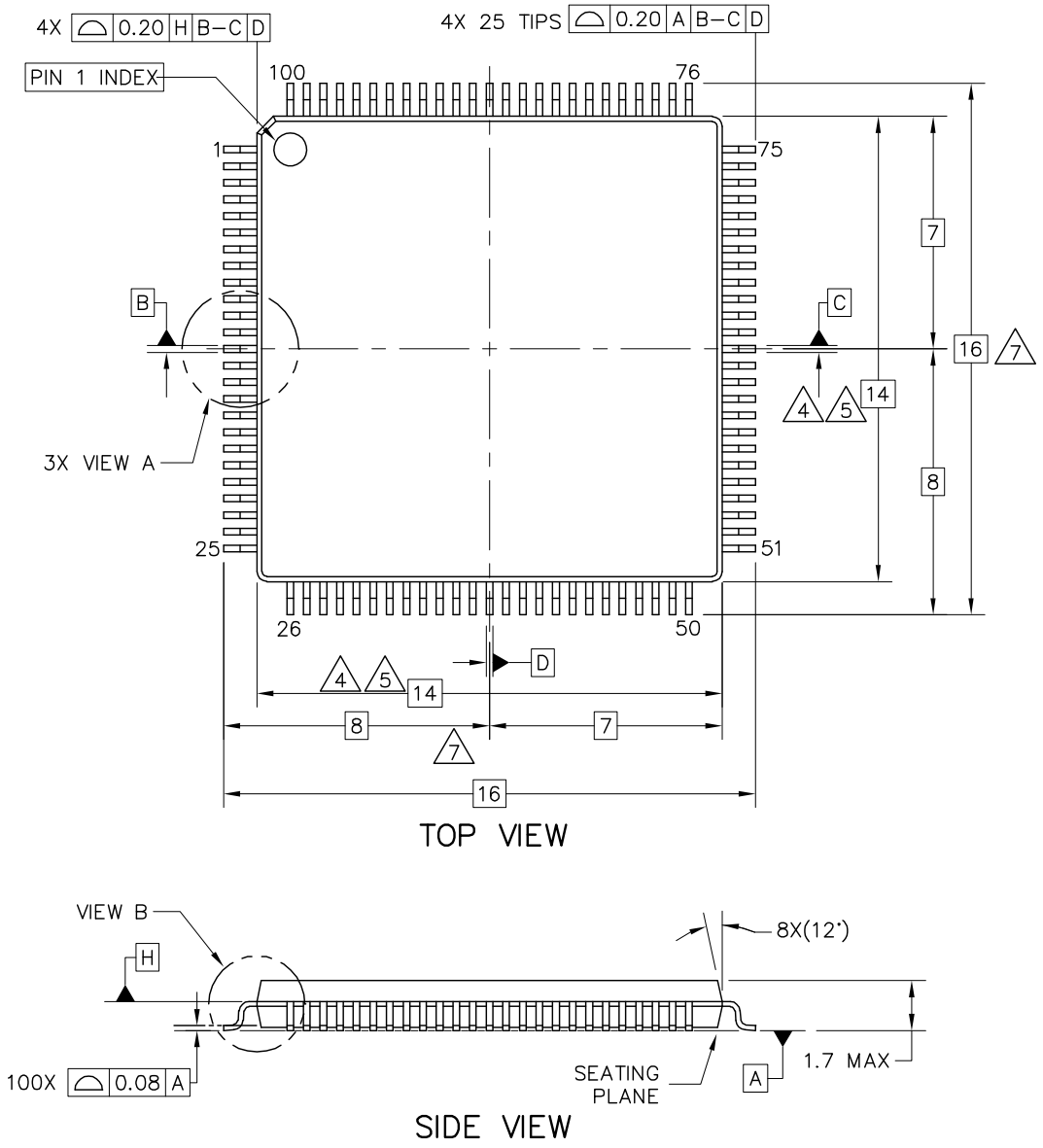
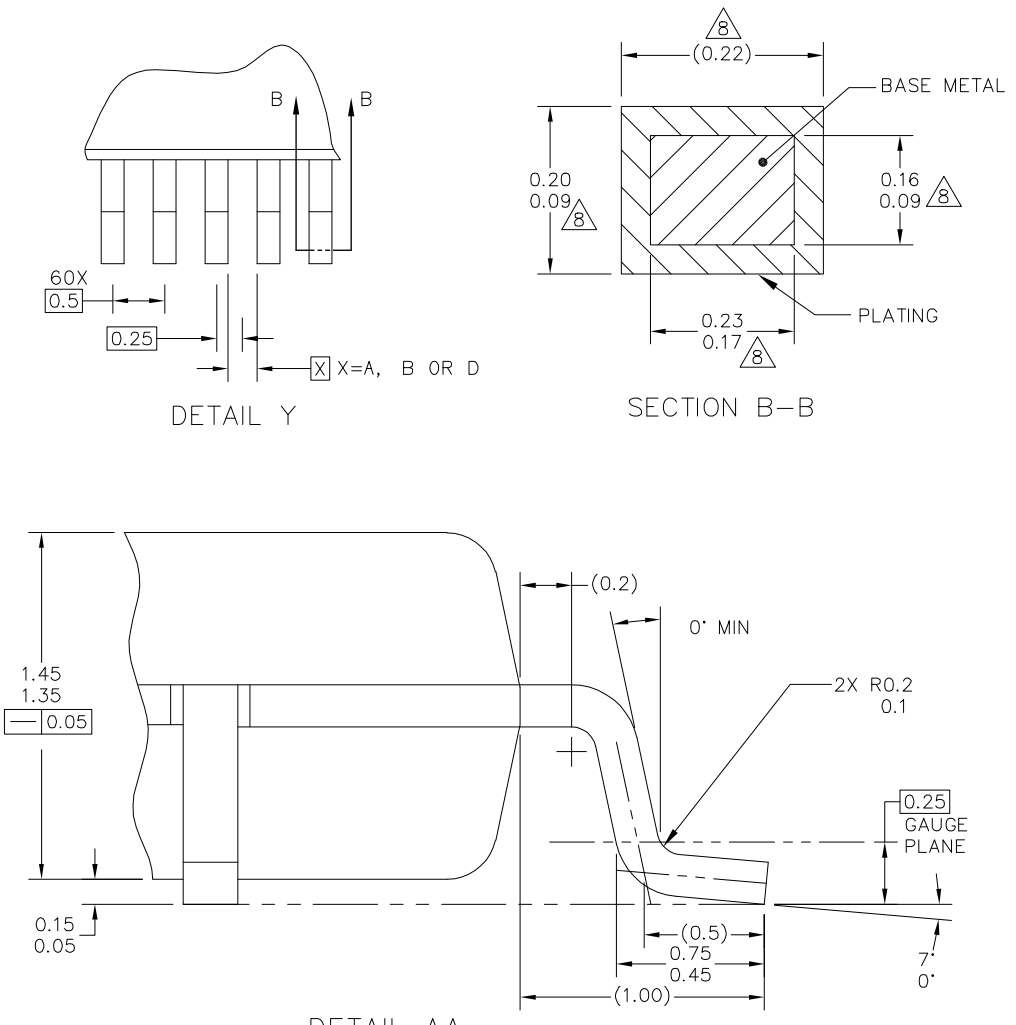


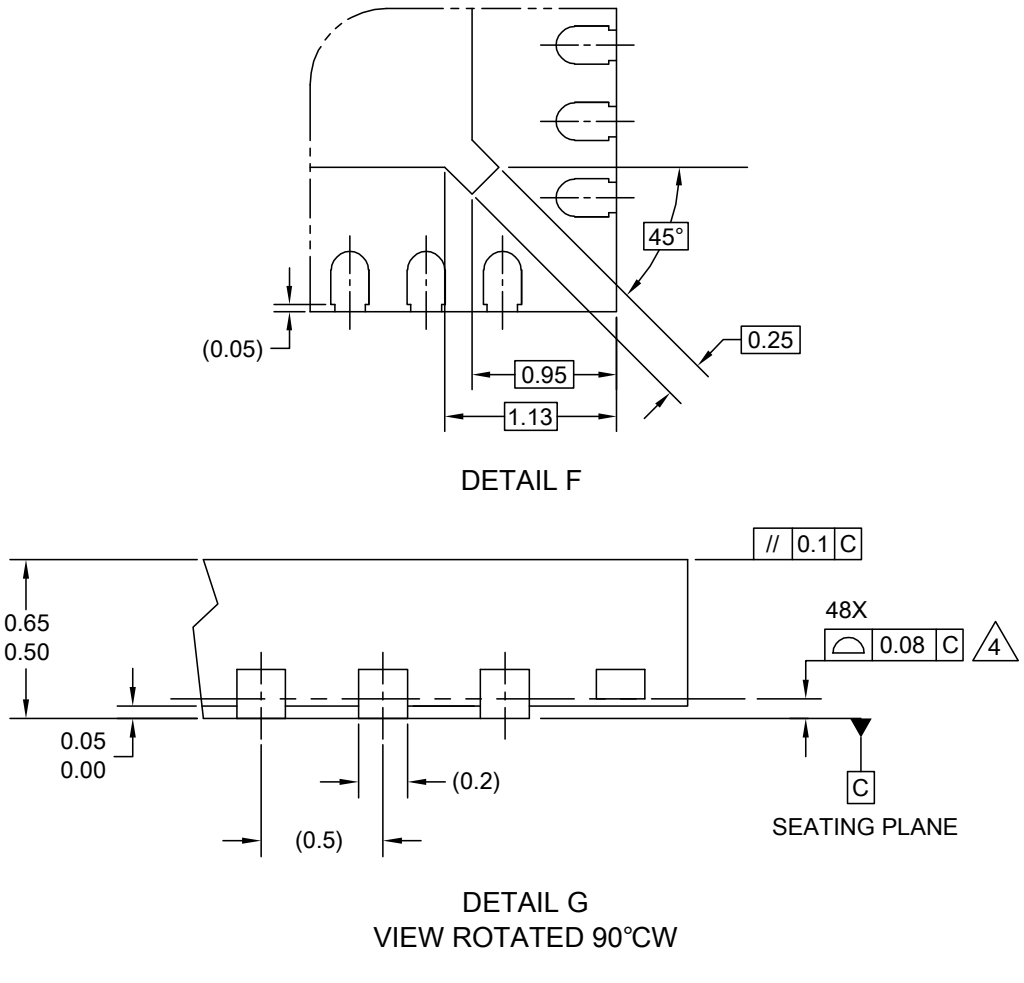

**Figure 9. 100-pin LQFP package dimensions 1**




NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.
5. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE UPPER LIMIT BY MORE THAN 0.08 MM AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07 MM.
6. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 MM PER SIDE. THIS DIMENSION IS MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 MM AND 0.25 MM FROM THE LEAD TIP.

**Figure 12. 64-pin LQFP package dimensions 2**




NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. THIS IS A NON-JEDEC REGISTERED PACKAGE.
4. COPLANARITY APPLIES TO LEADS AND DIE ATTACH FLAG.
5. MIN. METAL GAP SHOULD BE 0.2 MM.

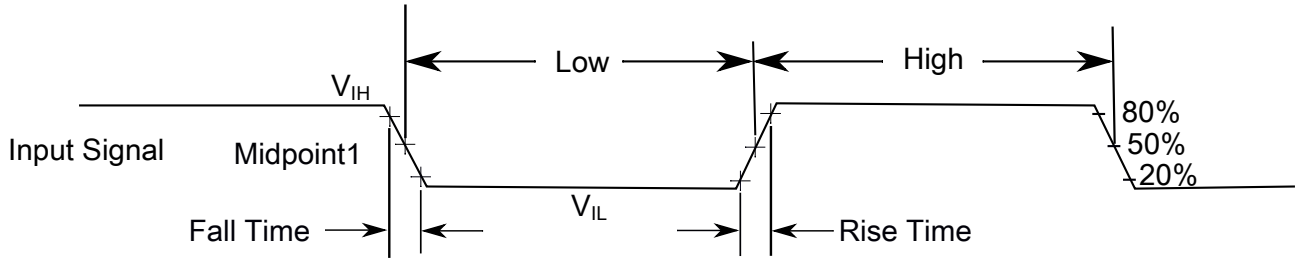
**Figure 14. 48-pin QFN package dimension 2**

# 5 Electrical characteristics

## 5.1 Terminology and guidelines

### 5.3.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.




The midpoint is $V_{IL}$ + ($V_{IH}$ - $V_{IL}$) / 2

**Figure 15. Input signal measurement reference**

All digital I/O switching characteristics, unless otherwise specified, assume that the output pins have the following characteristics.

- $C_L$=30 pF loads
- Slew rate disabled
- Normal drive strength

### 5.3.2 Nonswitching electrical specifications

#### 5.3.2.1 Voltage and current operating requirements

**Table 40. Voltage and current operating requirements**

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | 1.71 | 3.6 | V | |
| $V_{DDA}$ | Analog supply voltage | 1.71 | 3.6 | V | |
| $V_{DD} – V_{DDA}$ | $V_{DD}$-to-$V_{DDA}$ differential voltage | –0.1 | 0.1 | V | |
| $V_{SS} – V_{SSA}$ | $V_{SS}$-to-$V_{SSA}$ differential voltage | –0.1 | 0.1 | V | |
| $V_{BAT}$ | RTC battery supply voltage | 1.71 | 3.6 | V | |
| $USBV_{DD}$ | USB Transceiver supply voltage | 3.0 | 3.6 | V | 1 |
| $V_{IH}$ | Input high voltage<br>• 2.7 V ≤ $V_{DD}$ ≤ 3.6 V<br>• 1.7 V ≤ $V_{DD}$ ≤ 2.7 V | 0.7 × $V_{DD}$<br>0.75 × $V_{DD}$ | —<br>— | V<br>V | |

*Table continues on the next page...*

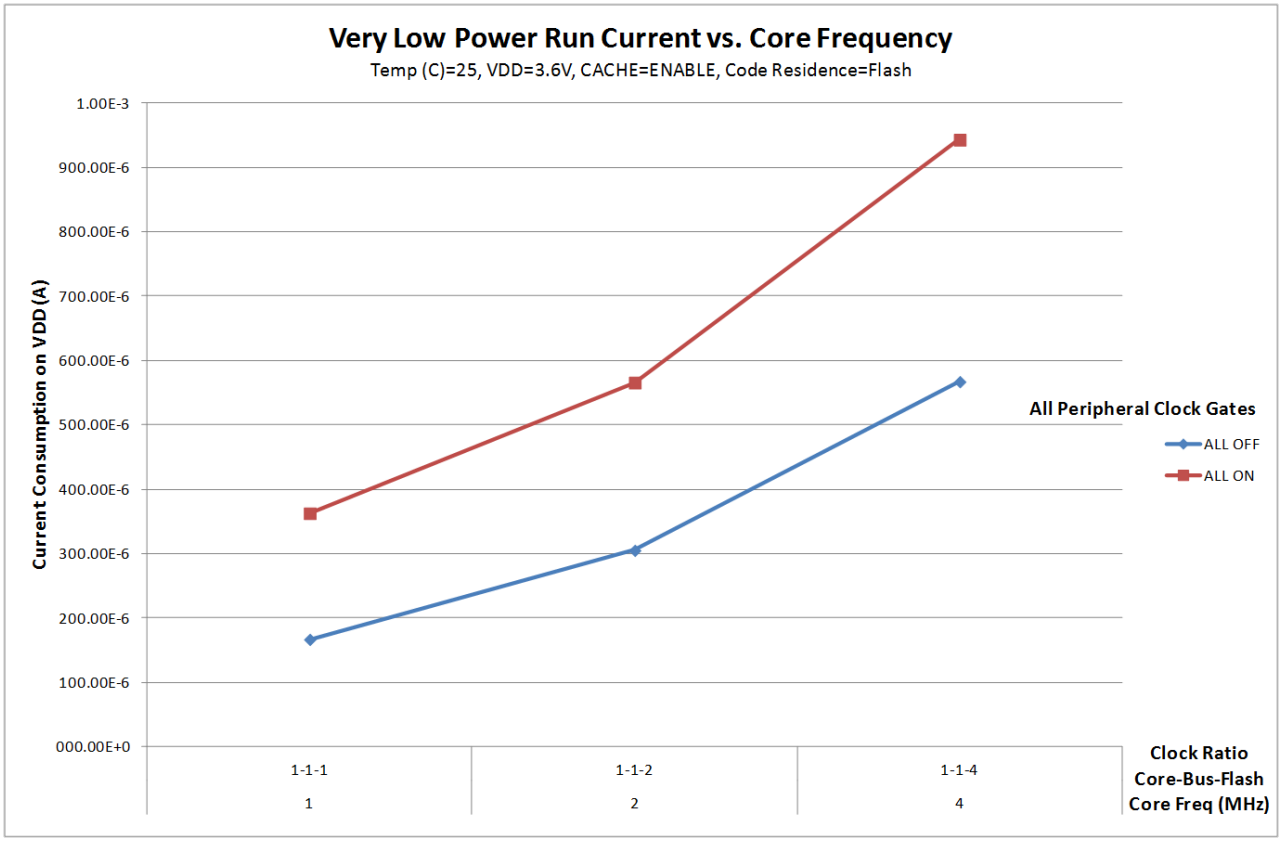



**Figure 17. VLPR mode supply current vs. core frequency**

### 5.3.2.6 EMC performance

Electromagnetic compatibility (EMC) performance is highly dependent on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components, and MCU software operation play a significant role in the EMC performance. The system designer can consult the following Freescale applications notes, available on freescale.com for advice and guidance specifically targeted at optimizing EMC performance.

- AN2321: Designing for Board Level Electromagnetic Compatibility
- AN1050: Designing for Electromagnetic Compatibility (EMC) with HCMOS Microcontrollers
- AN1263: Designing for Electromagnetic Compatibility with Single-Chip Microcontrollers

**Table 49. General switching specifications (continued)**

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| | GPIO pin interrupt pulse width (digital glitch filter disabled, passive filter disabled) — Asynchronous path | 50 | — | ns | 4 |
| | Port rise and fall time<br>• Slew disabled<br>• $1.71 \le V_{DD} \le 2.7V$<br>• $2.7 \le V_{DD} \le 3.6V$<br>• Slew enabled<br>• $1.71 \le V_{DD} \le 2.7V$<br>• $2.7 \le V_{DD} \le 3.6V$ | <br>—<br>—<br><br>—<br>—<br> | <br><br>10<br>5<br><br>30<br>16 | <br><br>ns<br>ns<br><br>ns<br>ns | 5 |

1. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In Stop, VLPS, LLS, and VLLSx modes, the synchronizer is bypassed so shorter pulses can be recognized in that case.
2. The greater of synchronous and asynchronous timing must be met.
3. These pins have a passive filter enabled on the inputs. This is the shortest pulse width that is guaranteed to be recognized.
4. These pins do not have a passive filter on the inputs. This is the shortest pulse width that is guaranteed to be recognized.
5. 25 pF load

## 5.3.4 Thermal specification

### 5.3.4.1 Thermal operating requirements

**Table 50. Thermal operating requirements**

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $T_J$ | Die junction temperature | –40 | 125 | °C | |
| $T_A$ | Ambient temperature | –40 | 105 | °C | 1 |

1. Maximum $T_A$ can be exceeded only if the user ensures that $T_J$ does not exceed maximum $T_J$. The simplest method to determine $T_J$ is: $T_J = T_A + R_{\Theta JA} \times$ chip power dissipation.

### 5.3.4.2 Thermal attributes

**Table 51. Thermal attributes**

| Board type | Symbol | Description | 100 LQFP | 64 LQFP | 48 QFN | Unit | Notes |
|---|---|---|---|---|---|---|---|
| Single-layer (1s) | $R_{\theta JA}$ | Thermal resistance, junction to ambient (natural convection) | 58 | 61 | 81 | °C/W | 1, 2, 3 |

*Table continues on the next page...*

**Table 53. JTAG limited voltage range electricals (continued)**

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| J11 | TCLK low to TDO data valid | — | 19 | ns |
| J12 | TCLK low to TDO high-Z | — | 19 | ns |
| J13 | $\overline{\text{TRST}}$ assert time | 100 | — | ns |
| J14 | $\overline{\text{TRST}}$ setup time (negation) to TCLK high | 8 | — | ns |

**Table 54. JTAG full voltage range electricals**

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| | Operating voltage | 1.71 | 3.6 | V |
| J1 | TCLK frequency of operation | | | MHz |
| | • Boundary Scan | 0 | 10 | |
| | • JTAG and CJTAG | 0 | 15 | |
| J2 | TCLK cycle period | 1/J1 | — | ns |
| J3 | TCLK clock pulse width | | | |
| | • Boundary Scan | 50 | — | ns |
| | • JTAG and CJTAG | 33 | — | ns |
| J4 | TCLK rise and fall times | — | 3 | ns |
| J5 | Boundary scan input data setup time to TCLK rise | 20 | — | ns |
| J6 | Boundary scan input data hold time after TCLK rise | 1.4 | — | ns |
| J7 | TCLK low to boundary scan output data valid | — | 27 | ns |
| J8 | TCLK low to boundary scan output high-Z | — | 27 | ns |
| J9 | TMS, TDI input data setup time to TCLK rise | 8 | — | ns |
| J10 | TMS, TDI input data hold time after TCLK rise | 1.4 | — | ns |
| J11 | TCLK low to TDO data valid | — | 26.2 | ns |
| J12 | TCLK low to TDO high-Z | — | 26.2 | ns |
| J13 | $\overline{\text{TRST}}$ assert time | 100 | — | ns |
| J14 | $\overline{\text{TRST}}$ setup time (negation) to TCLK high | 8 | — | ns |

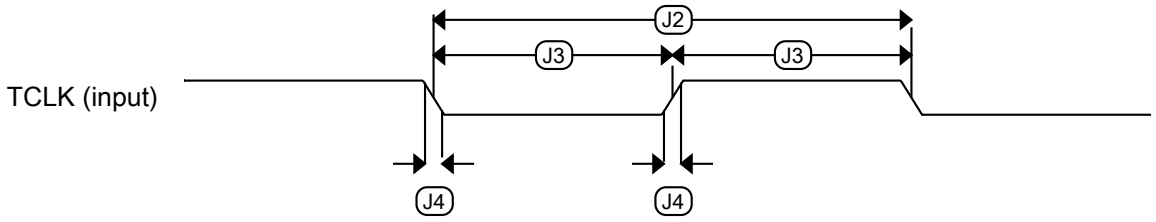



**Figure 20. Test clock input timing**

### 5.4.6.3.2 12-bit DAC operating behaviors

**Table 69. 12-bit DAC operating behaviors**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $I_{DDA\_DACLP}$ | Supply current — low-power mode | — | — | 330 | µA | |
| $I_{DDA\_DACHP}$ | Supply current — high-speed mode | — | — | 1200 | µA | |
| $t_{DACLP}$ | Full-scale settling time (0x080 to 0xF7F) — low-power mode | — | 100 | 200 | µs | 1 |
| $t_{DACHP}$ | Full-scale settling time (0x080 to 0xF7F) — high-power mode | — | 15 | 30 | µs | 1 |
| $t_{CCDACLP}$ | Code-to-code settling time (0xBF8 to 0xC08) — low-power mode and high-speed mode | — | 0.7 | 1 | µs | 1 |
| $V_{dacoutl}$ | DAC output voltage range low — high-speed mode, no load, DAC set to 0x000 | — | — | 100 | mV | |
| $V_{dacouth}$ | DAC output voltage range high — high-speed mode, no load, DAC set to 0xFFF | $V_{DACR}$ –100 | — | $V_{DACR}$ | mV | |
| INL | Integral non-linearity error — high speed mode | — | — | ±8 | LSB | 2 |
| DNL | Differential non-linearity error — $V_{DACR}$ > 2 V | — | — | ±1 | LSB | 3 |
| DNL | Differential non-linearity error — $V_{DACR}$ = VREF_OUT | — | — | ±1 | LSB | 4 |
| $V_{OFFSET}$ | Offset error | — | ±0.4 | ±0.8 | %FSR | 5 |
| $E_G$ | Gain error | — | ±0.1 | ±0.6 | %FSR | 5 |
| PSRR | Power supply rejection ratio, $V_{DDA}$ ≥ 2.4 V | 60 | — | 90 | dB | |
| $T_{CO}$ | Temperature coefficient offset voltage | — | 3.7 | — | µV/C | 6 |
| $T_{GE}$ | Temperature coefficient gain error | — | 0.000421 | — | %FSR/C | |
| Rop | Output resistance (load = 3 kΩ) | — | — | 250 | Ω | |
| SR | Slew rate -80h→ F7Fh→ 80h<br>• High power ($SP_{HP}$)<br>• Low power ($SP_{LP}$) | <br>1.2<br>0.05 | <br>1.7<br>0.12 | <br>—<br>— | V/µs | |
| BW | 3dB bandwidth<br>• High power ($SP_{HP}$)<br>• Low power ($SP_{LP}$) | <br>550<br>40 | <br>—<br>— | <br>—<br>— | kHz | |

1. Settling within ±1 LSB
2. The INL is measured for 0 + 100 mV to $V_{DACR}$ –100 mV
3. The DNL is measured for 0 + 100 mV to $V_{DACR}$ –100 mV
4. The DNL is measured for 0 + 100 mV to $V_{DACR}$ –100 mV with $V_{DDA}$ > 2.4 V
5. Calculated by a best fit curve from $V_{SS}$ + 100 mV to $V_{DACR}$ – 100 mV
6. $V_{DDA}$ = 3.0 V, reference select set for $V_{DDA}$ (DACx_CO:DACRFS = 1), high power mode (DACx_C0:LPEN = 0), DAC set to 0x800, temperature range is across the full range of the device

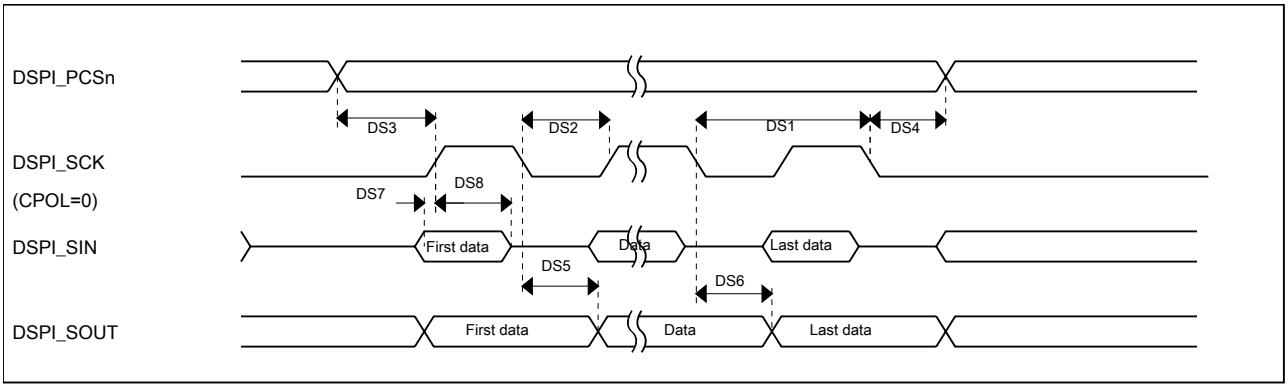



**Figure 31. DSPI classic SPI timing — master mode**

## Table 71. Slave mode DSPI timing (limited voltage range)

| Num | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| | Operating voltage | 2.7 | 3.6 | V | |
| | Frequency of operation | — | 15 | MHz | 1 |
| DS9 | DSPI_SCK input cycle time | 4 x $t_{BUS}$ | — | ns | |
| DS10 | DSPI_SCK input high/low time | ($t_{SCK}$/2) – 2 | ($t_{SCK}$/2) + 2 | ns | |
| DS11 | DSPI_SCK to DSPI_SOUT valid | — | 21.4 | ns | |
| DS12 | DSPI_SCK to DSPI_SOUT invalid | 0 | — | ns | |
| DS13 | DSPI_SIN to DSPI_SCK input setup | 2.6 | — | ns | |
| DS14 | DSPI_SCK to DSPI_SIN input hold | 7 | — | ns | |
| DS15 | $\overline{\text{DSPI\_SS}}$ active to DSPI_SOUT driven | — | 17 | ns | |
| DS16 | $\overline{\text{DSPI\_SS}}$ inactive to DSPI_SOUT not driven | — | 17 | ns | |

1. The maximum operating frequency is measured with noncontinuous CS and SCK. When DSPI is configured with continuous CS and SCK, the SPI clock must not be greater than 1/6 of the bus clock. For example, when the bus clock is 60 MHz, the SPI clock must not be greater than 10 MHz.

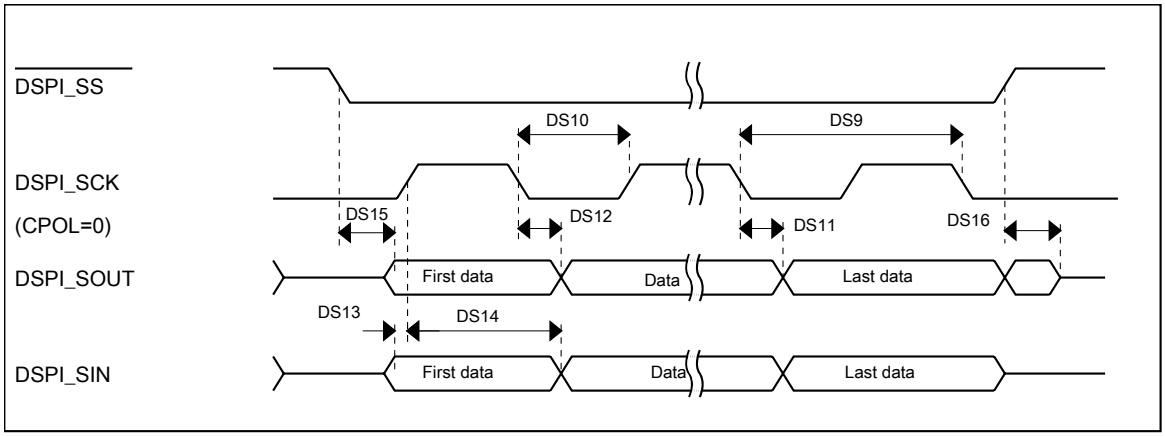



**Figure 32. DSPI classic SPI timing — slave mode**

**Table 73. Slave mode DSPI timing (full voltage range)**

| Num | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| | Operating voltage | 1.71 | 3.6 | V |
| | Frequency of operation | — | 7.5 | MHz |
| DS9 | DSPI_SCK input cycle time | 8 x $t_{BUS}$ | — | ns |
| DS10 | DSPI_SCK input high/low time | ($t_{SCK}$/2) - 4 | ($t_{SCK/2}$) + 4 | ns |
| DS11 | DSPI_SCK to DSPI_SOUT valid | — | 29.5 | ns |
| DS12 | DSPI_SCK to DSPI_SOUT invalid | 0 | — | ns |
| DS13 | DSPI_SIN to DSPI_SCK input setup | 3.2 | — | ns |
| DS14 | DSPI_SCK to DSPI_SIN input hold | 7 | — | ns |
| DS15 | $\overline{\text{DSPI\_SS}}$ active to DSPI_SOUT driven | — | 25 | ns |
| DS16 | $\overline{\text{DSPI\_SS}}$ inactive to DSPI_SOUT not driven | — | 25 | ns |

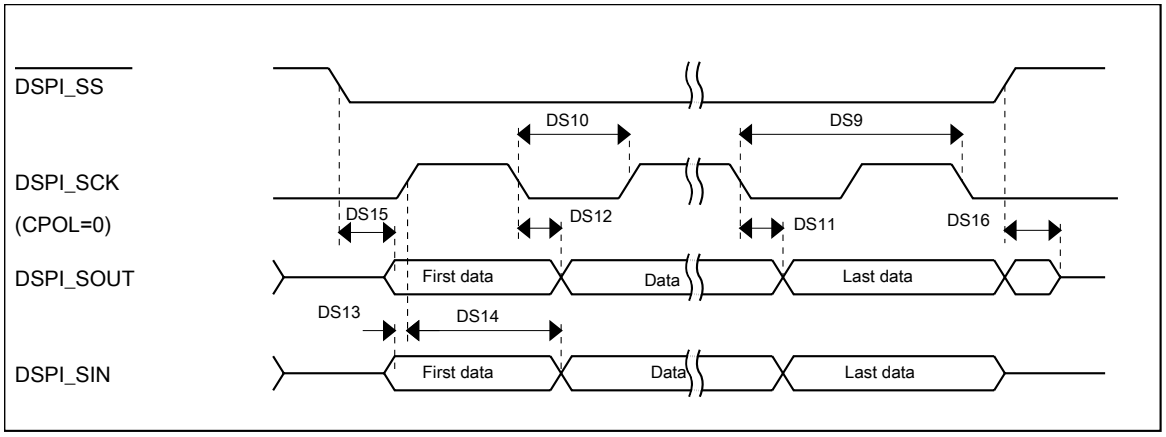



**Figure 34. DSPI classic SPI timing — slave mode**

## 5.4.8.4 LPI$^2$C

**Table 74. LPI$^2$C specifications**

| Symbol | Description | | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $f_{SCL}$ | SCL clock frequency | Standard mode (Sm) | 0 | 100 | kHz | 1 |
| | | Fast mode (Fm) | 0 | 400 | | 1, 2 |
| | | Fast mode Plus (Fm+) | 0 | 1000 | | 1, 3 |
| | | Ultra Fast mode (UFm) | 0 | 5000 | | 1, 4 |
| | | High speed mode (Hs-mode) | 0 | 3400 | | 1, 5 |

1. See General switching specifications, measured at room temperature.
2. Measured with the maximum bus loading of 400pF at 3.3V VDD with pull-up Rp = 220Ω , and at 1.8V VDD with Rp = 880Ω. For all other cases, select appropriate Rp per I2C Bus Specification and the pin drive capability.
3. Fm+ is only supported on high drive pin with high drive enabled. It is measured with the maximum bus loading of 400pF at 3.3V VDD with Rp = 220Ω. For all other cases, select appropriate Rp per I2C Bus Specification and the pin drive capability.

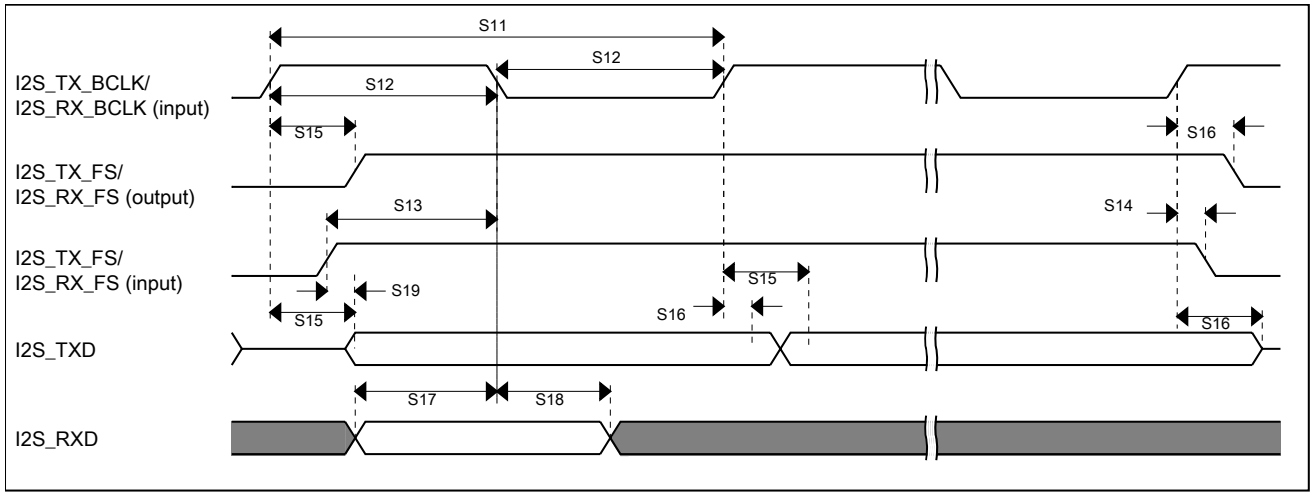



**Figure 40. I2S/SAI timing — slave modes**

# 6 Design considerations

## 6.1 Hardware design considerations

This device contains protective circuitry to guard against damage due to high static voltage or electric fields. However, take normal precautions to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit.

### 6.1.1 Printed circuit board recommendations

- Place connectors or cables on one edge of the board and do not place digital circuits between connectors.
- Drivers and filters for I/O functions must be placed as close to the connectors as possible. Connect TVS devices at the connector to a good ground. Connect filter capacitors at the connector to a good ground.
- Physically isolate analog circuits from digital circuits if possible.
- Place input filter capacitors as close to the MCU as possible.
- For best EMC performance, route signals as transmission lines; use a ground plane directly under LQFP packages; and solder the exposed pad (EP) to ground directly under QFN packages.

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Document Number KS22P100M120SF0
Revision 3, 04/2016