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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, I²C, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	40
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 1x16b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mks20fn256vlh12

The security circuitry prevents unauthorized access to RAM or flash contents from debug port.

- System register file

  This device contains a 32-byte register file that is powered in all power modes.

  Also, it retains contents during low power modes and is reset only during a power-on reset.

2.1.5 Reset and boot

The following table lists all the reset sources supported by this device.

NOTE

In the following table, Y means the specific module, except for the registers, bits or conditions mentioned in the footnote, is reset by the corresponding Reset source. N means the specific module is not reset by the corresponding Reset source.

Table 3. Reset source

Reset sources	Descriptions	Modules								
		PMC	SIM	SMC	RCM	LLWU	Reset pin is negated	RTC	LPTMR	Others
POR reset	Power-on reset (POR)	Y	Y	Y	Y	Y	Y	Y	Y	Y
System resets	Low-voltage detect (LVD)	Y[1]	Y	Y	Y	Y	Y	N	Y	Y
	Low leakage wakeup (LLWU) reset	N	Y[2]	N	Y	N	Y[3]	N	N	Y
	External pin reset ($\overline{\text{RESET}}$)	Y[1]	Y[2]	Y[4]	Y	Y	Y	N	N	Y
	Watchdog (WDOG) reset	Y[1]	Y[2]	Y[4]	Y[5]	Y	Y	N	N	Y
	Multipurpose clock generator loss of clock (LOC) reset	Y[1]	Y[2]	Y[4]	Y[5]	Y	Y	N	N	Y
	Multipurpose clock generator loss of lock (LOL) reset	Y[1]	Y[2]	Y[4]	Y[5]	Y	Y	N	N	Y
	Stop mode acknowledge error (SACKERR)	Y[1]	Y[2]	Y[4]	Y[5]	Y	Y	N	N	Y
	Software reset (SW)	Y[1]	Y[2]	Y[4]	Y[5]	Y	Y	N	N	Y
	Lockup reset (LOCKUP)	Y[1]	Y[2]	Y[4]	Y[5]	Y	Y	N	N	Y

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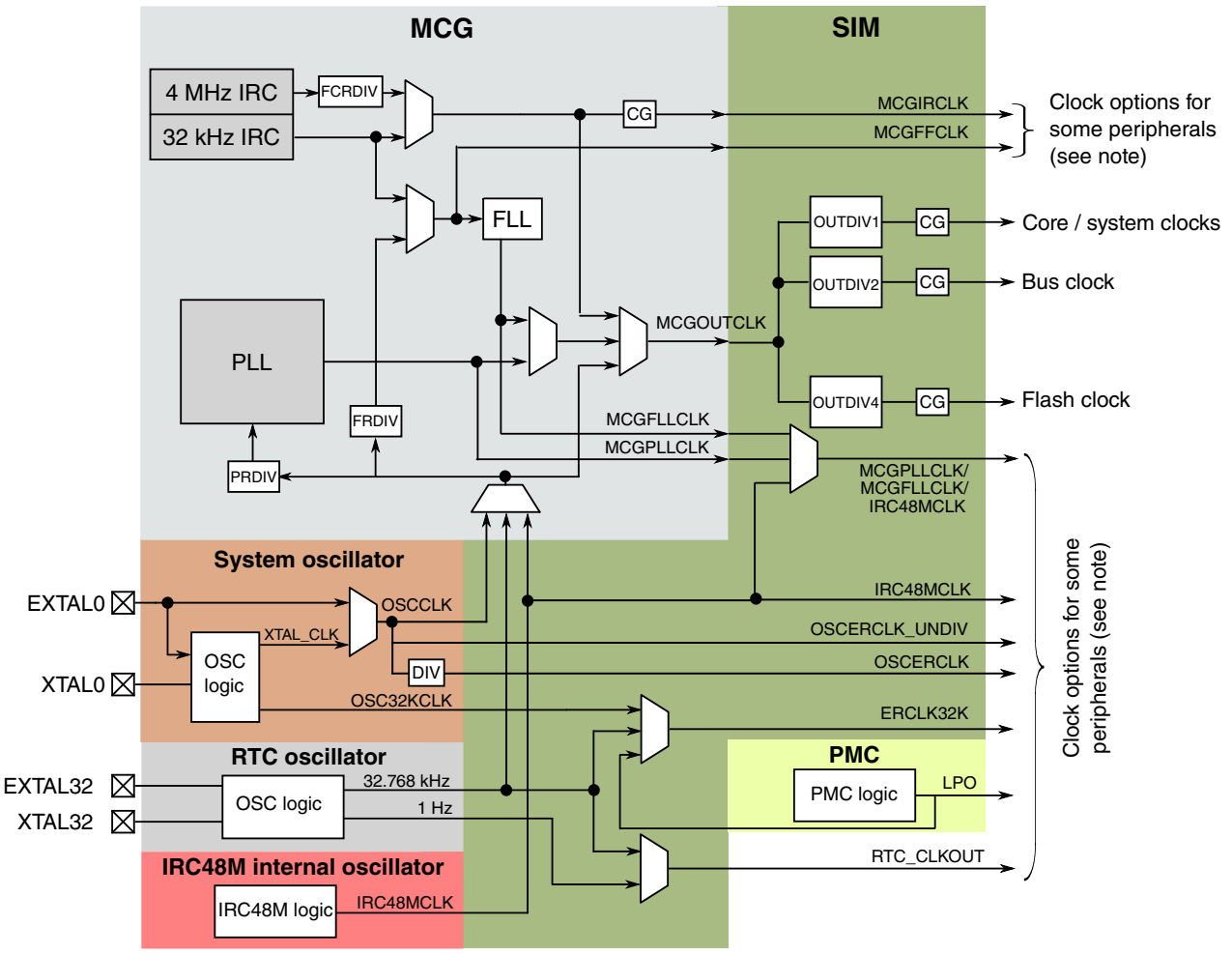


CG — Clock gate
Note: See subsequent sections for details on where these clocks are used.

Figure 3. Clock block diagram

In order to provide flexibility, many peripherals can select the clock source to use for operation. This enables the peripheral to select a clock that will always be available during operation in various operational modes.

The following table summarizes the clocks associated with each module.

Table 4. Module clocks

Module	Bus interface clock	Internal clocks	I/O interface clocks
Core modules			
ARM Cortex-M4 core	System clock	Core clock	—
NVIC	System clock	—	—
DAP	System clock	—	—

Table continues on the next page...

2.2.1 eDMA and DMAMUX

The eDMA is a highly programmable data-transfer engine optimized to minimize any required intervention from the host processor. It is intended for use in applications where the data size to be transferred is statically known and not defined within the transferred data itself. The DMA controller in this device implements 16 channels which can be routed from up to 63 DMA request sources through DMA MUX module.

Main features of eDMA are listed below:

- All data movement via dual-address transfers: read from source, write to destination
- 16-channel implementation that performs complex data transfers with minimal intervention from a host processor
- Transfer control descriptor (TCD) organized to support two-deep, nested transfer operations
- Channel activation via one of three methods
- Fixed-priority and round-robin channel arbitration
- Channel completion reported via programmable interrupt requests
- Programmable support for scatter/gather DMA processing
- Support for complex data structures

2.2.2 TPM

This device contains three low power Timer/PWM Modules (TPM), one with 6 channels and the other two with 2 channels. All TPM modules are functional in Stop/ VLPS mode if the clock source is enabled.

The TPM features are as follows:

- TPM clock mode is selectable (can increment on every edge of the asynchronous counter clock, or only on on rising edge of an external clock input synchronized to the asynchronous counter clock)
- Prescaler divide-by 1, 2, 4, 8, 16, 32, 64, or 128
- Include a 16-bit counter
- Include 6 or 2 channels (1×6ch, 2×2ch) that can be configured for input capture, output compare, edge-aligned PWM mode, or center-aligned PWM mode
- Support the generation of an interrupt and/or DMA request per channel or counter overflow

timing between ADC conversions and/or DAC updates can be achieved. The PDB can optionally provide pulse outputs (Pulse-Out's) that are used as the sample window in the CMP block.

The PIT module has the following features:

- Up to 15 trigger input sources and one software trigger source
- Up to 8 configurable PDB channels for ADC hardware trigger
- Up to 8 pulse outputs (pulse-out's)

2.2.9 LPTMR

The low-power timer (LPTMR) can be configured to operate as a time counter with optional prescaler, or as a pulse counter with optional glitch filter, across all power modes, including the low-leakage modes. It can also continue operating through most system reset events, allowing it to be used as a time of day counter.

The LPTMR module has the following features:

- 16-bit time counter or pulse counter with compare
  - Optional interrupt can generate asynchronous wakeup from any low-power mode
  - Hardware trigger output
  - Counter supports free-running mode or reset on compare
- Configurable clock source for prescaler/glitch filter
- Configurable input source for pulse counter

2.2.10 CRC

This device contains one cyclic redundancy check (CRC) module which can generate 16/32-bit CRC code for error detection.

The CRC module provides a programmable polynomial, WAS, and other parameters required to implement a 16-bit or 32-bit CRC standard.

The CRC module has the following features:

- Hardware CRC generator circuit using a 16-bit or 32-bit programmable shift register
- Programmable initial seed value and polynomial
- Option to transpose input data or output data (the CRC result) bitwise or bytewise.
- Option for inversion of final CRC result
- 32-bit CPU register programming interface

4.3.5 Timer Modules

Table 18. PDB 0 Signal Descriptions

Chip signal name	Module signal name	Description	I/O
PDB0_EXTRG	EXTRG	External Trigger Input Source If the PDB is enabled and external trigger input source is selected, a positive edge on the EXTRG signal resets and starts the counter.	I

Table 19. LPTMR 0 Signal Descriptions

Chip signal name	Module signal name	Description	I/O
LPTMR0_ALT[2:1]	LPTMR0_ALT*n*	Pulse Counter Input pin	I

Table 20. RTC Signal Descriptions

Chip signal name	Module signal name	Description	I/O
VBAT	—	Backup battery supply for RTC and VBAT register file	I
RTC_CLKOUT	RTC_CLKOUT	1 Hz square-wave output or OSCERCLK	O

Table 21. TPM 0 Signal Descriptions

Chip signal name	Module signal name	Description	I/O
TPM_CLKIN[1:0]	TPM_EXTCLK	External clock. TPM external clock can be selected to increment the TPM counter on every rising edge synchronized to the counter clock.	I
TPM0_CH[5:0]	TPM_CHn	TPM channel (n = 5 to 0). A TPM channel pin is configured as output when configured in an output compare or PWM mode and the TPM counter is enabled, otherwise the TPM channel pin is an input.	I/O

Table 22. TPM 1 Signal Descriptions

Chip signal name	Module signal name	Description	I/O
TPM_CLKIN[1:0]	TPM_EXTCLK	External clock. TPM external clock can be selected to increment the TPM counter on every rising edge synchronized to the counter clock.	I

Table continues on the next page...

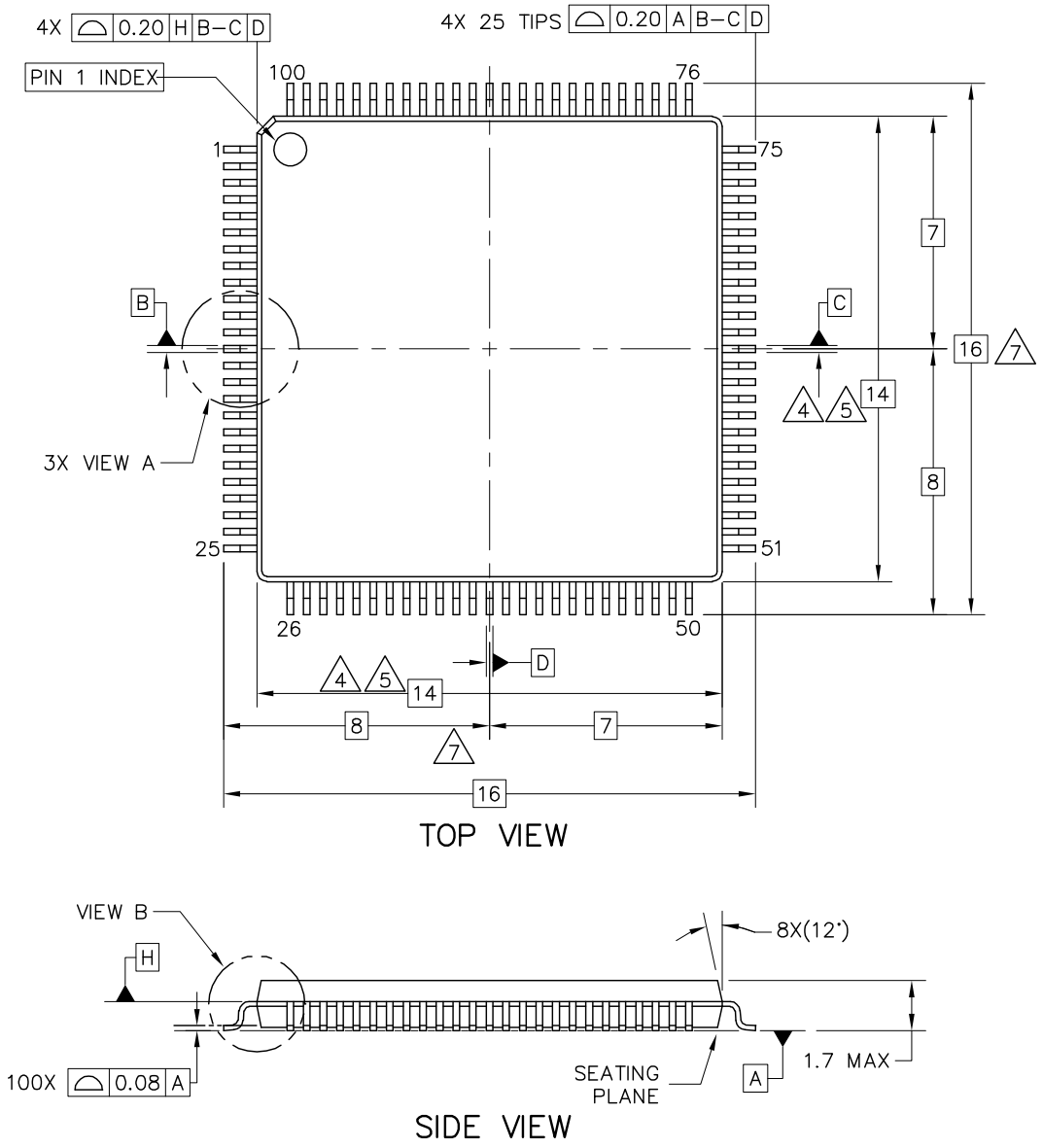
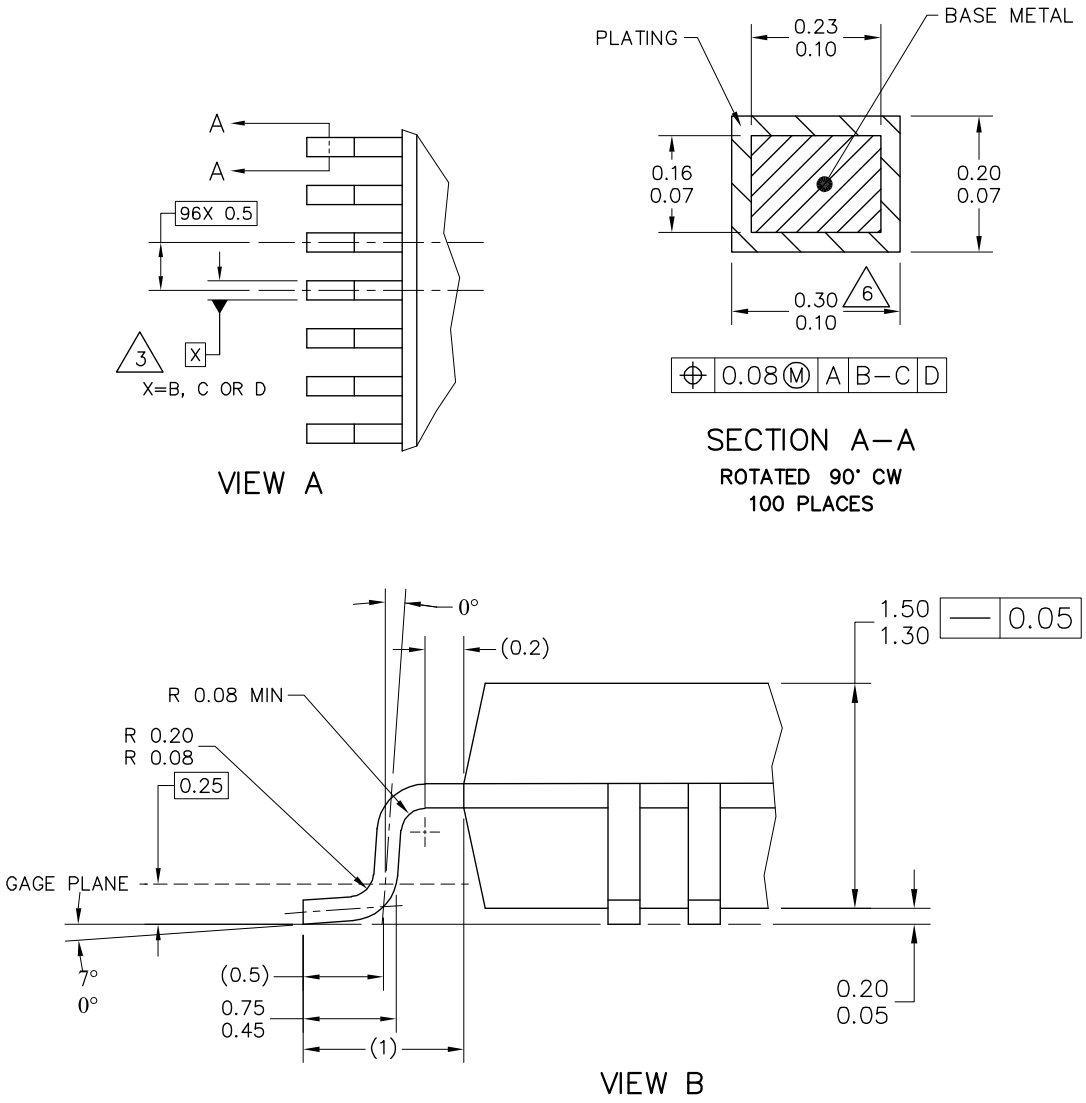


Figure 9. 100-pin LQFP package dimensions 1



NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. DATUMS B, C AND D TO BE DETERMINED AT DATUM PLANE H.
4. THE TOP PACKAGE BODY SIZE MAY BE SMALLER THAN THE BOTTOM PACKAGE SIZE BY A MAXIMUM OF 0.1 MM.
5. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSIONS. THE MAXIMUM ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. THE DIMENSIONS ARE MAXIMUM BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
6. DIMENSION DOES NOT INCLUDE DAM BAR PROTRUSION. PROTRUSIONS SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.35. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD SHALL BE 0.07 MM.
7. DIMENSIONS ARE DETERMINED AT THE SEATING PLANE, DATUM A.

Figure 10. 100-pin LQFP package dimensions 2

5.2.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

5.2.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	-2000	+2000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model	-500	+500	V	2
I_{LAT}	Latch-up current at ambient temperature of 105°C	-100	+100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

5.2.4 Voltage and current operating ratings

Table 39. Voltage and current operating ratings

Symbol	Description	Min.	Max.	Unit
V_{DD}	Digital supply voltage	–0.3	3.8	V
I_{DD}	Digital supply current	—	120	mA
V_{IO}	IO pin input voltage	–0.3	V_{DD} + 0.3	V
I_D	Instantaneous maximum current single pin limit (applies to all port pins)	–25	25	mA
V_{DDA}	Analog supply voltage	V_{DD} – 0.3	V_{DD} + 0.3	V
V_{USB_DP}	USB_DP input voltage	–0.3	3.63	V
V_{USB_DM}	USB_DM input voltage	–0.3	3.63	V
V_{BAT}	RTC battery supply voltage	–0.3	3.8	V

5.3 General

5.3.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

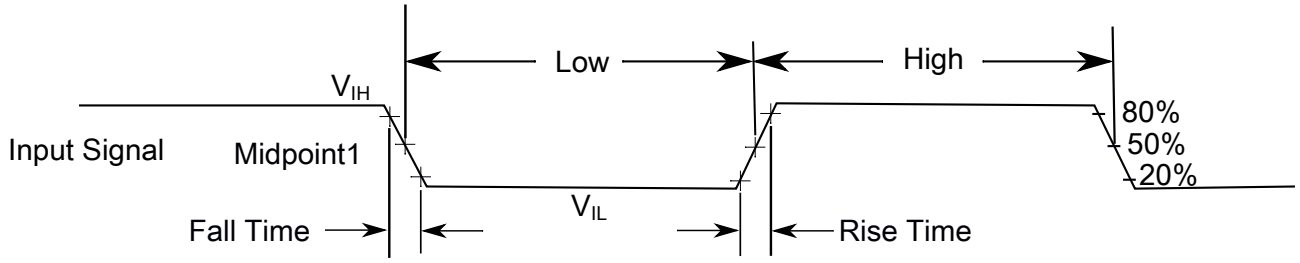


Figure 15. Input signal measurement reference

All digital I/O switching characteristics, unless otherwise specified, assume that the output pins have the following characteristics.

- C_L=30 pF loads
- Slew rate disabled
- Normal drive strength

5.3.2 Nonswitching electrical specifications

5.3.2.1 Voltage and current operating requirements

Table 40. Voltage and current operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	3.6	V	
V_{DDA}	Analog supply voltage	1.71	3.6	V	
$V_{DD} – V_{DDA}$	V_{DD}-to-V_{DDA} differential voltage	–0.1	0.1	V	
$V_{SS} – V_{SSA}$	V_{SS}-to-V_{SSA} differential voltage	–0.1	0.1	V	
V_{BAT}	RTC battery supply voltage	1.71	3.6	V	
$USBV_{DD}$	USB Transceiver supply voltage	3.0	3.6	V	1
V_{IH}	Input high voltage • 2.7 V ≤ V_{DD} ≤ 3.6 V • 1.7 V ≤ V_{DD} ≤ 2.7 V	0.7 × V_{DD} 0.75 × V_{DD}	— —	V V	

Table continues on the next page...

Table 45. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DD_VLPR}	Very-low-power run mode current in Compute operation — CoreMark benchmark code executing from flash					
	@ 1.8V	—	967.09	1031.341	µA	3, 4, 11
	@ 3.0V	—	973.06	1040.294	µA	
I_{DD_VLPR}	Very-low-power run mode current in Compute operation, code executing from flash					
	@ 1.8V	—	449.10	513.351	µA	11
	@ 3.0V	—	462.61	529.844	µA	
I_{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks disabled	—	520.34	592.022	µA	12
I_{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks enabled	—	845.46	1005.706	µA	13
I_{DD_VLPW}	Very-low-power wait mode current at 3.0 V — all peripheral clocks disabled	—	240.81	269.275	µA	14
I_{DD_STOP}	Stop mode current at 3.0 V					
	@ 25°C	—	269.63	292.223	µA	
	@ -40°C	—	253.73	280.001	µA	
	@ 70°C	—	309.98	346.335	µA	
	@ 85°C	—	347.88	401.693	µA	
	@ 105°C	—	450.05	565.013	µA	
I_{DD_VLPS}	Very-low-power stop mode current at 3.0 V					
	@ 25°C	—	3.48	6.005	µA	
	@ -40°C	—	2.47	3.740	µA	
	@ 70°C	—	15.20	30.384	µA	
	@ 85°C	—	28.62	52.396	µA	
	@ 105°C	—	65.48	115.129	µA	
I_{DD_LLS3}	Low leakage stop mode 3 current at 3.0 V					
	@ 25°C	—	2.78	3.778	µA	
	@ -40°C	—	2.14	2.881	µA	
	@ 70°C	—	7.72	12.481	µA	
	@ 85°C	—	13.30	21.607	µA	
	@ 105°C	—	29.50	47.202	µA	
I_{DD_LLS2}	Low leakage stop mode 2 current at 3.0 V					
	@ 25°C	—	2.56	3.293	µA	
	@ -40°C	—	2.10	2.802	µA	
	@ 70°C	—	6.14	8.758	µA	
	@ 85°C	—	10.34	15.242	µA	
	@ 105°C	—	22.68	33.393	µA	
I_{DD_VLLS3}	Very low-leakage stop mode 3 current at 3.0 V					
	@ 25°C	—	2.01	2.769	µA	

Table continues on the next page...

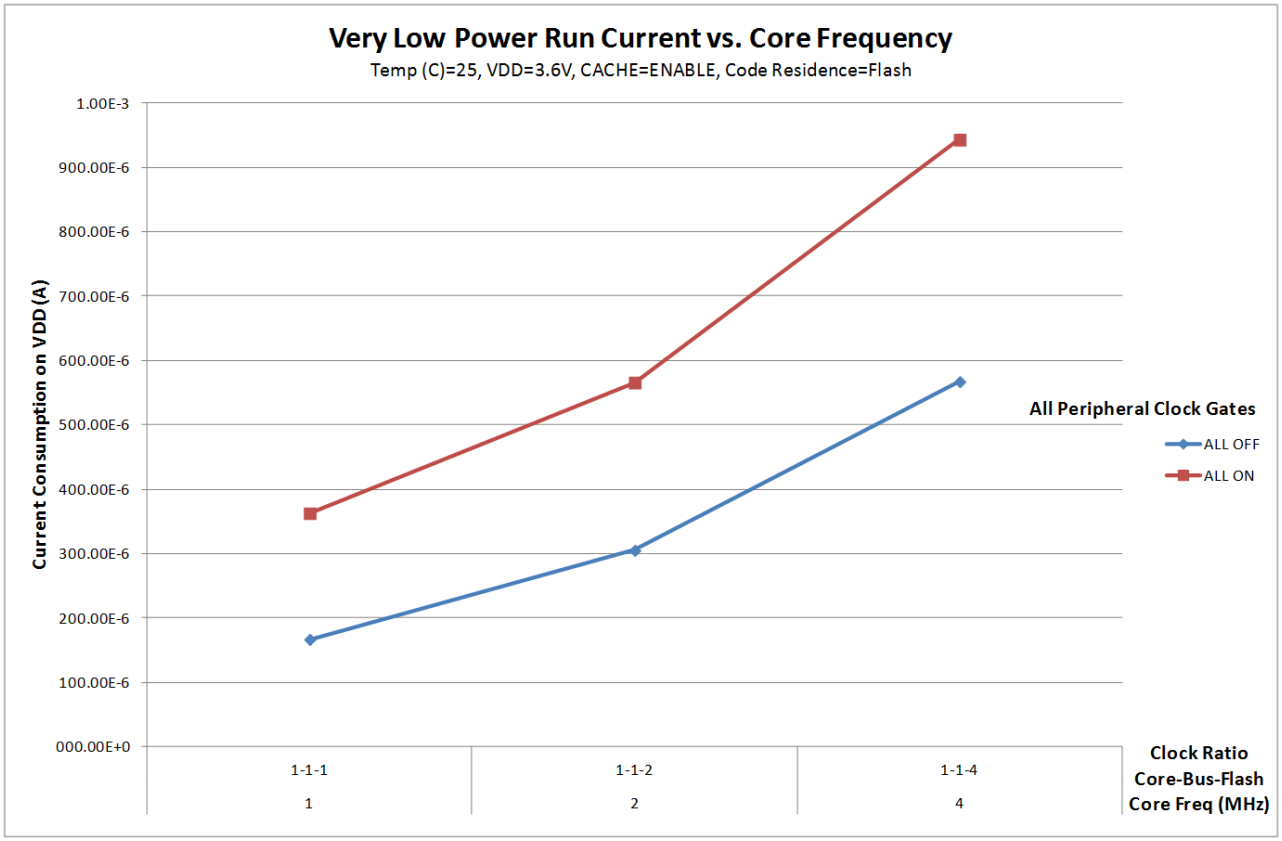


Figure 17. VLPR mode supply current vs. core frequency

5.3.2.6 EMC performance

Electromagnetic compatibility (EMC) performance is highly dependent on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components, and MCU software operation play a significant role in the EMC performance. The system designer can consult the following Freescale applications notes, available on freescale.com for advice and guidance specifically targeted at optimizing EMC performance.

- AN2321: Designing for Board Level Electromagnetic Compatibility
- AN1050: Designing for Electromagnetic Compatibility (EMC) with HCMOS Microcontrollers
- AN1263: Designing for Electromagnetic Compatibility with Single-Chip Microcontrollers

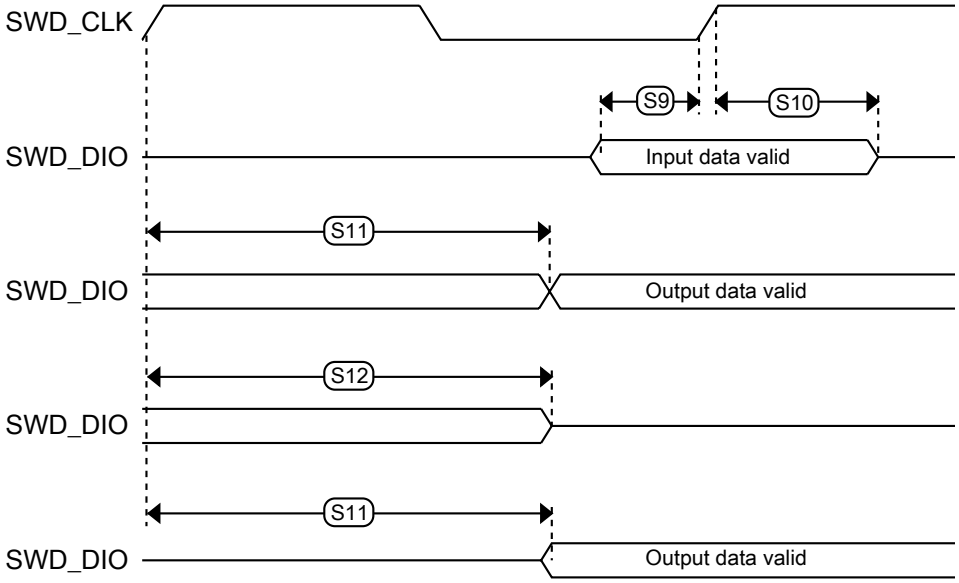


Figure 19. Serial wire data timing

5.4.1.2 JTAG electricals

Table 53. JTAG limited voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
J1	TCLK frequency of operation			MHz
	• Boundary Scan	0	10	
	• JTAG and CJTAG	0	20	
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width			
	• Boundary Scan	50	—	ns
	• JTAG and CJTAG	25	—	ns
J4	TCLK rise and fall times	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	1	—	ns
J7	TCLK low to boundary scan output data valid	—	25	ns
J8	TCLK low to boundary scan output high-Z	—	25	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	1	—	ns

Table continues on the next page...

Table 55. MCG specifications (continued)

Symbol	Description		Min.	Typ.	Max.	Unit	Notes
f_{loc_high}	Loss of external clock minimum frequency — RANGE = 01, 10, or 11		(16/5) x f_{ints_t}	—	—	kHz	
FLL							
f_{fll_ref}	FLL reference frequency range		31.25	—	39.0625	kHz	
f_{dco}	DCO output frequency range	Low range (DRS=00) 640 × f_{fll_ref}	20	20.97	25	MHz	3, 4
		Mid range (DRS=01) 1280 × f_{fll_ref}	40	41.94	50	MHz	
		Mid-high range (DRS=10) 1920 × f_{fll_ref}	60	62.91	75	MHz	
		High range (DRS=11) 2560 × f_{fll_ref}	80	83.89	100	MHz	
$f_{dco\_t\_DMX32}$	DCO output frequency	Low range (DRS=00) 732 × f_{fll_ref}	—	23.99	—	MHz	5, 6
		Mid range (DRS=01) 1464 × f_{fll_ref}	—	47.97	—	MHz	
		Mid-high range (DRS=10) 2197 × f_{fll_ref}	—	71.99	—	MHz	
		High range (DRS=11) 2929 × f_{fll_ref}	—	95.98	—	MHz	
J_{cyc_fll}	FLL period jitter • f_{VCO} = 48 MHz • f_{VCO} = 98 MHz		— —	— 180 150	— —	ps	
$t_{fll\_acquire}$	FLL target frequency acquisition time		—	—	1	ms	7
PLL							
f_{vco}	VCO operating frequency		48.0	—	120	MHz	
I_{pll}	PLL operating current • PLL @ 96 MHz ($f_{osc\_hi\_1}$ = 8 MHz, f_{pll_ref} = 2 MHz, VDIV multiplier = 48)		—	1060	—	µA	8
I_{pll}	PLL operating current • PLL @ 48 MHz ($f_{osc\_hi\_1}$ = 8 MHz, f_{pll_ref} = 2 MHz, VDIV multiplier = 24)		—	600	—	µA	8
f_{pll_ref}	PLL reference frequency range		2.0	—	4.0	MHz	
J_{cyc_pll}	PLL period jitter (RMS) • f_{vco} = 48 MHz • f_{vco} = 100 MHz		— —	120 75	— —	ps ps	9
J_{acc_pll}	PLL accumulated jitter over 1µs (RMS)		— —	1350 600	— —	ps ps	9

Table continues on the next page...

5.4.6 Analog

5.4.6.1 ADC electrical specifications

The 16-bit accuracy specifications listed in Table 65 and Table 66 are achievable on the differential pins ADCx_DPx, ADCx_DMx.

All other ADC channels meet the 13-bit differential/12-bit single-ended accuracy specifications.

5.4.6.1.1 16-bit ADC operating conditions

Table 65. 16-bit ADC operating conditions

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
V_{DDA}	Supply voltage	Absolute	1.71	—	3.6	V	
ΔV_{DDA}	Supply voltage	Delta to V_{DD} (V_{DD} – V_{DDA})	-100	0	+100	mV	2
ΔV_{SSA}	Ground voltage	Delta to V_{SS} (V_{SS} – V_{SSA})	-100	0	+100	mV	2
V_{REFH}	ADC reference voltage high		1.13	V_{DDA}	V_{DDA}	V	
V_{REFL}	ADC reference voltage low		V_{SSA}	V_{SSA}	V_{SSA}	V	
V_{ADIN}	Input voltage	• 16-bit differential mode • All other modes	VREFL VREFL	— —	31/32 * VREFH VREFH	V	
C_{ADIN}	Input capacitance	• 16-bit mode • 8-bit / 10-bit / 12-bit modes	— —	8 4	10 5	pF	
R_{ADIN}	Input series resistance		—	2	5	kΩ	
R_{AS}	Analog source resistance (external)	13-bit / 12-bit modes f_{ADCK} < 4 MHz	—	—	5	kΩ	3
f_{ADCK}	ADC conversion clock frequency	≤ 13-bit mode	1.0	—	24.0	MHz	4
f_{ADCK}	ADC conversion clock frequency	16-bit mode	2.0	—	12.0	MHz	4
C_{rate}	ADC conversion rate	≤ 13-bit modes No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	20	—	1200	Ksps	5
C_{rate}	ADC conversion rate	16-bit mode No ADC hardware averaging	37	—	461	Ksps	5

Table 66. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

Symbol	Description	Conditions[1]	Min.	Typ.[2]	Max.	Unit	Notes
E_{IL}	Input leakage error		$I_{In} \times R_{AS}$			mV	I_{In} = leakage current (refer to the MCU's voltage and current operating ratings)
	Temp sensor slope	Across the full temperature range of the device	1.55	1.62	1.69	mV/°C	8
V_{TEMP25}	Temp sensor voltage	25 °C	706	716	726	mV	8

1. All accuracy numbers assume the ADC is calibrated with $V_{REFH} = V_{DDA}$
2. Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 2.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
3. The ADC supply current depends on the ADC conversion clock speed, conversion rate and ADC_CFG1[ADLPC] (low power). For lowest power operation, ADC_CFG1[ADLPC] must be set, the ADC_CFG2[ADHSC] bit must be clear with 1 MHz ADC conversion clock speed.
4. 1 LSB = $(V_{REFH} - V_{REFL})/2^N$
5. ADC conversion clock < 16 MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
6. Input data is 100 Hz sine wave. ADC conversion clock < 12 MHz.
7. Input data is 1 kHz sine wave. ADC conversion clock < 12 MHz.
8. ADC conversion clock < 3 MHz

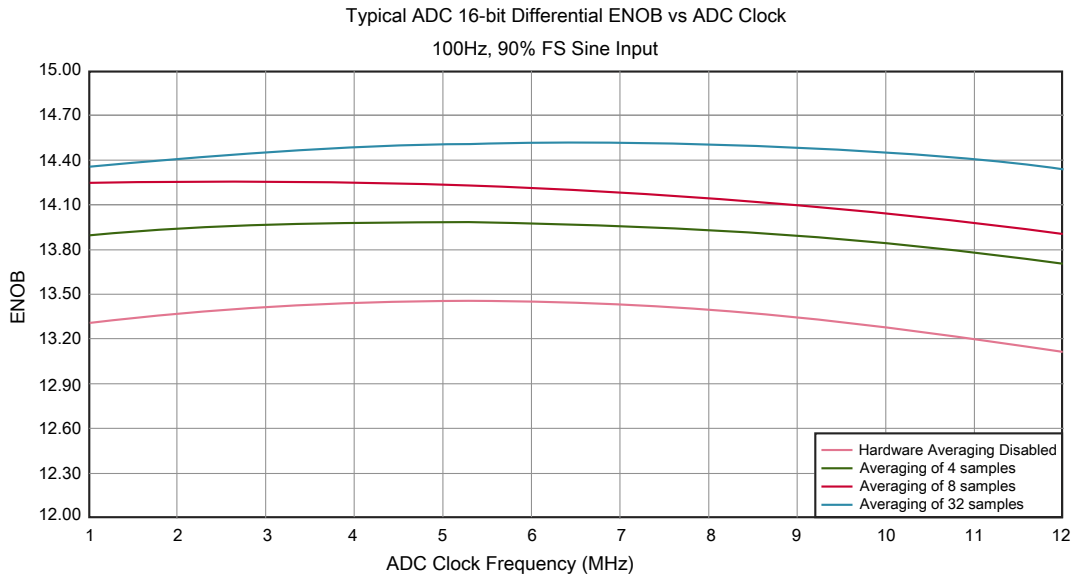


Figure 25. Typical ENOB vs. ADC_CLK for 16-bit differential mode

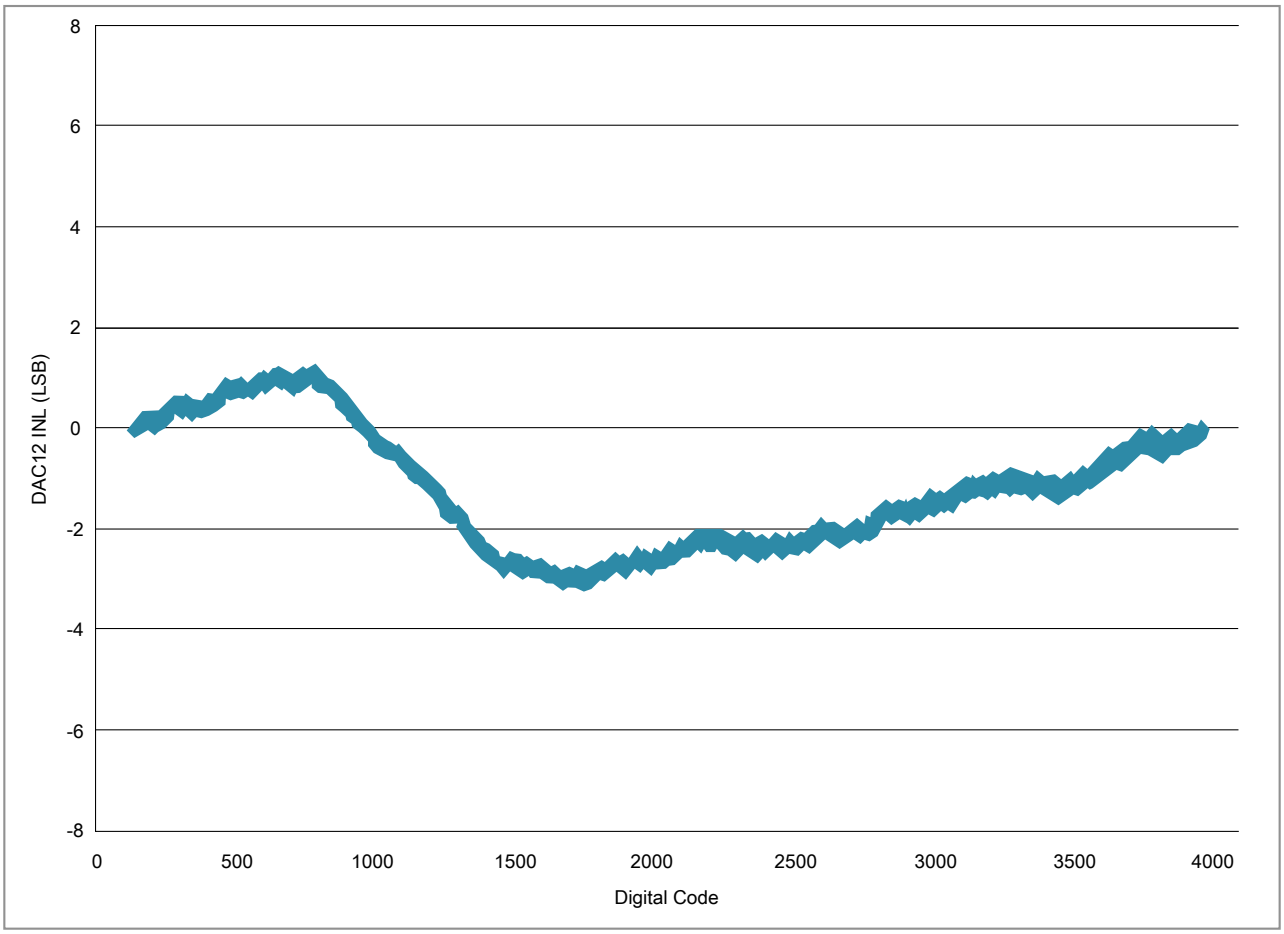


Figure 29. Typical INL error vs. digital code

Table 73. Slave mode DSPI timing (full voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
	Frequency of operation	—	7.5	MHz
DS9	DSPI_SCK input cycle time	8 x t_{BUS}	—	ns
DS10	DSPI_SCK input high/low time	(t_{SCK}/2) - 4	($t_{SCK/2}$) + 4	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	29.5	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	3.2	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns
DS15	$\overline{\text{DSPI\_SS}}$ active to DSPI_SOUT driven	—	25	ns
DS16	$\overline{\text{DSPI\_SS}}$ inactive to DSPI_SOUT not driven	—	25	ns

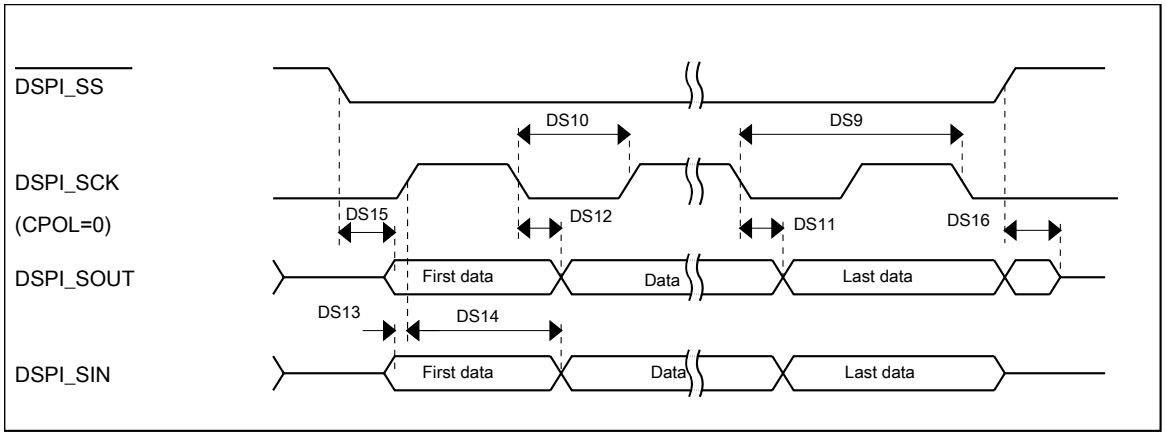


Figure 34. DSPI classic SPI timing — slave mode

5.4.8.4 LPI^{2}C

Table 74. LPI^{2}C specifications

Symbol	Description		Min.	Max.	Unit	Notes
f_{SCL}	SCL clock frequency	Standard mode (Sm)	0	100	kHz	1
		Fast mode (Fm)	0	400		1, 2
		Fast mode Plus (Fm+)	0	1000		1, 3
		Ultra Fast mode (UFm)	0	5000		1, 4
		High speed mode (Hs-mode)	0	3400		1, 5

1. See General switching specifications, measured at room temperature.
2. Measured with the maximum bus loading of 400pF at 3.3V VDD with pull-up Rp = 220Ω , and at 1.8V VDD with Rp = 880Ω. For all other cases, select appropriate Rp per I2C Bus Specification and the pin drive capability.
3. Fm+ is only supported on high drive pin with high drive enabled. It is measured with the maximum bus loading of 400pF at 3.3V VDD with Rp = 220Ω. For all other cases, select appropriate Rp per I2C Bus Specification and the pin drive capability.

4. UFm is only supported on high drive pin with high drive enabled and push-pull output only mode. It is measured at 3.3V VDD with the maximum bus loading of 400pF. For 1.8V VDD, the maximum speed is 4Mbps.
5. Hs-mode is only supported in slave mode and on the high drive pins with high drive enabled.

5.4.8.5 UART switching specifications

See General switching specifications.

5.4.8.6 I2S/SAI switching specifications

This section provides the AC timing for the I2S/SAI module in master mode (clocks are driven) and slave mode (clocks are input). All timing is given for noninverted serial clock polarity (TCR2[BCP] is 0, RCR2[BCP] is 0) and a noninverted frame sync (TCR4[FSP] is 0, RCR4[FSP] is 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the bit clock signal (BCLK) and/or the frame sync (FS) signal shown in the following figures.

5.4.8.6.1 Normal Run, Wait and Stop mode performance over a limited operating voltage range

This section provides the operating performance over a limited operating voltage for the device in Normal Run, Wait and Stop modes.

Table 75. I2S/SAI master mode timing in Normal Run, Wait and Stop modes (limited voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
S1	I2S_MCLK cycle time	40	—	ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	80	—	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid	—	15	ns
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid	0	—	ns
S7	I2S_TX_BCLK to I2S_TXD valid	—	15	ns
S8	I2S_TX_BCLK to I2S_TXD invalid	0	—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	18	—	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns

This MCU uses the standard ARM SWD interface protocol as shown in the following figure. While pull-up or pull-down resistors are not required (SWD_DIO has an internal pull-up and SWD_CLK has an internal pull-down), external 10 kΩ pull resistors are recommended for system robustness. The RESET_b pin recommendations mentioned above must also be considered.

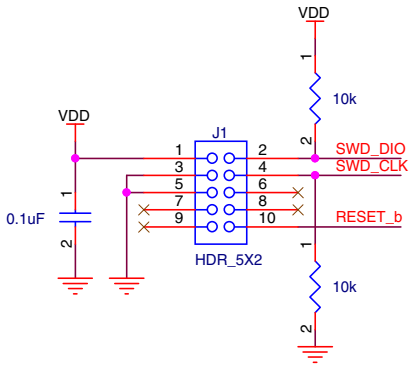


Figure 46. SWD debug interface

- Low leakage stop mode wakeup

  Select low leakage wakeup pins (LLWU_Px) to wake the MCU from one of the low leakage stop modes (LLS/VLLSx). See the pinout table for pin selection.

- Unused pin

  Unused GPIO pins must be left floating (no electrical connections) with the MUX field of the pin's PORTx_PCRn register equal to 0:0:0. This disables the digital input path to the MCU.

  If the USB module is not used, leave the USB data pins (USB0_DP, USB0_DM) floating. Connect USB_VDD to ground through a 10 kΩ resistor if the USB module is not used.

6.1.5 Crystal oscillator

When using an external crystal or ceramic resonator as the frequency reference for the MCU clock system, refer to the following table and diagrams.

The feedback resistor, RF, is incorporated internally with the low power oscillators. An external feedback is required when using high gain (HGO=1) mode.

7.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

7.2 Format

Part numbers for this device have the following format:

Q KS## A FFF R T PP CC N

7.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Table 82. Part number fields description

Field	Description	Values
Q	Qualification status	• M = Fully qualified, general market flow • P = Prequalification
KS##	Kinetis family	• KS20 • KS22
A	Key attribute	• F = Cortex-M4 with DSP and FPU
FFF	Program flash memory size	• 128 = 128 KB • 256 = 256 KB
R	Silicon revision	• (Blank) = Main • A = Revision after main
T	Temperature range (°C)	• V = –40 to 105
PP	Package identifier	• FT = 48 QFN (7 mm x 7 mm) • LH = 64 LQFP (10 mm x 10 mm) • LL = 100 LQFP (14 mm x 14 mm)
CC	Maximum CPU frequency (MHz)	• 12 = 120 MHz
N	Packaging type	• R = Tape and reel • (Blank) = Trays

7.4 Example

This is an example part number:

MKS22FN256VLL12