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Product Status	Active
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Program Memory Type	-
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RAM Size	-
Voltage - Supply (Vcc/Vdd)	-
Data Converters	-
Oscillator Type	-
Operating Temperature	-
Mounting Type	-
Package / Case	-
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mks20fn256vll12

1 Ordering information

The following chips are available for ordering.

Table 1. Ordering information

Product		Memory		Package		IO and ADC channel			Communication
Part number	Marking (Line1/Line2)	Flash (KB)	SRAM (KB)	Pin count	Package	GPIOs	GPIOs (INT/HD) [1]	ADC channels (SE/DP) [2]	FlexCAN
MKS22FN256VLL12	MKS22FN256 / VLL12	256	64	100	LQFP	66	66/8	17/4	2
MKS22FN256VLH12	MKS22FN256 / VLH12	256	64	64	LQFP	40	40/8	14/2 [3]	2
MKS22FN256VFT12	MKS22FN256 / VFT12	256	64	48	QFN	35	35/8	13/—	2
MKS22FN128VLL12	MKS22FN128 / VLL12	128	64	100	LQFP	66	66/8	17/4	2
MKS22FN128VLH12	MKS22FN128 / VLH12	128	64	64	LQFP	40	40/8	14/2 [3]	2
MKS22FN128VFT12	MKS22FN128 / VFT12	128	64	48	QFN	35	35/8	13/—	2
MKS20FN256VLL12	MKS20FN256 / VLL12	256	64	100	LQFP	66	66/8	17/4	1
MKS20FN256VLH12	MKS20FN256 / VLH12	256	64	64	LQFP	40	40/8	14/2 [3]	1
MKS20FN256VFT12	MKS20FN256 / VFT12	256	64	48	QFN	35	35/8	13/—	1
MKS20FN128VLL12	MKS20FN128 / VLL12	128	64	100	LQFP	66	66/8	17/4	1
MKS20FN128VLH12	MKS20FN128 / VLH12	128	64	64	LQFP	40	40/8	14/2 [3]	1
MKS20FN128VFT12	MKS20FN128 / VFT12	128	64	48	QFN	35	35/8	13/—	1

Wake-up sources for this SoC are listed as below:

Table 2. AWIC Partial Stop, Stop and VLPS Wake-up Sources

Wake-up source	Description
Available system resets	$\overline{\text{RESET}}$ pin and WDOG when LPO is its clock source, and JTAG
Low voltage detect	Power Mode Controller
Low voltage warning	Power Mode Controller
High voltage detect	Power Mode Controller
Pin interrupts	Port Control Module - Any enabled pin interrupt is capable of waking the system
ADC	The ADC is functional when using internal clock source
CMP	Since no system clocks are available, functionality is limited, trigger mode provides wakeup functionality with periodic sampling
LPI^{2}C	Functional when using clock source which is active in Stop and VLPS modes
FlexIO	Functional when using clock source which is active in Stop and VLPS modes
TPM	Functional when using clock source which is active in Stop and VLPS modes
UART	Active edge on RXD
LPUART	Functional when using clock source which is active in Stop and VLPS modes
USB FS/LS Controller	Wakeup
LPTMR	Functional when using clock source which is active in Stop and VLPS modes
RTC	Functional in Stop/VLPS modes
I2S (SAI)	Functional when using an external bit clock or external master clock
TPM	Functional when using clock source which is active in Stop and VLPS modes
CAN	Wakeup on edge (CANx_RX)
NMI	Non-maskable interrupt

2.1.4 Memory

This device has the following features:

- 64 KB of embedded RAM accessible (read/write) at CPU clock speed with 0 wait states.
- The non-volatile memory is divided into
  - 128/256 KB of embedded program memory

  The program flash memory contains a 16-byte flash configuration field that stores default protection settings and security information. The page size of program flash is 2 KB.

  The protection setting can protect 32 regions of the program flash memory from unintended erase or program operations.

- Support selectable trigger input to optionally reset or cause the counter to start or stop incrementing
- Support the generation of hardware triggers when the counter overflows and per channel

2.2.3 ADC

This device contains one ADC module. This ADC module supports hardware triggers from TPM, LPTMR, PIT, RTC, external trigger pin and CMP output. It supports wakeup of MCU in low power mode when using internal clock source or external crystal clock.

ADC module has the following features:

- Linear successive approximation algorithm with up to 16-bit resolution
- Up to four pairs of differential and 17 single-ended external analog inputs
- Support selectable 16-bit, 13-bit, 11-bit, and 9-bit differential output mode, or 16-bit, 12-bit, 10-bit, and 8-bit single-ended output modes
- Single or continuous conversion
- Configurable sample time and conversion speed/power
- Selectable clock source up to three
- Operation in low-power modes for lower noise
- Asynchronous clock source for lower noise operation with option to output the clock
- Selectable hardware conversion trigger
- Automatic compare with interrupt for less-than, greater-than or equal-to, within range, or out-of-range, programmable value
- Temperature sensor
- Hardware average function up to 32×
- Voltage reference: from external
- Self-calibration mode

2.2.3.1 Temperature sensor

This device contains one temperature sensor internally connected to the input channel of AD26, see Table 66 for details of the linearity factor.

The sensor must be calibrated to gain good accuracy, so as to provide good linearity, see also AN3031.

2.2.4 DAC

The 12-bit digital-to-analog converter (DAC) is a low-power, general-purpose DAC. The output of the DAC can be placed on an external pin or set as one of the inputs to the analog comparator, or ADC.

DAC module has the following features:

- On-chip programmable reference generator output. The voltage output range is from 1⁄4096 V_{in} to V_{in}, and the step is 1⁄4096 V_{in}, where V_{in} is the input voltage.
- V_{in} can be selected from the reference source V_{DDA}
- Static operation in Normal Stop mode
- 16-word data buffer supported with multiple operation modes
- DMA support

2.2.5 CMP

The device contains one high-speed comparator and two 8-input multiplexers for both the inverting and non-inverting inputs of the comparator. Each CMP input channel connects to both muxes.

The CMP includes one 6-bit DAC, which provides a selectable voltage reference for various user application cases. Besides, the CMP also has several module-to-module interconnects in order to facilitate ADC triggering, TPM triggering, and interfaces.

The CMP has the following features:

- Inputs may range from rail to rail
- Programmable hysteresis control
- Selectable interrupt on rising-edge, falling-edge, or both rising or falling edges of the comparator output
- Selectable inversion on comparator output
- Capability to produce a wide range of outputs such as sampled, digitally filtered
- External hysteresis can be used at the same time that the output filter is used for internal functions
- Two software selectable performance levels: shorter propagation delay at the expense of higher power and Low power with longer propagation delay
- DMA transfer support
- Functional in all modes of operation except in VLLS0 mode
- The filter functions are not available in Stop, VLPS, LLS, or VLLSx modes
- Integrated 6-bit DAC with selectable supply reference source and can be power down to conserve power
- Two 8-to-1 channel mux

100 LQFP	64 LQFP	48 QFN	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
21	12	—	ADC0_DM3	ADC0_DM3	ADC0_DM3							
22	13	12	VDDA	VDDA	VDDA							
23	14	12	VREFH	VREFH	VREFH							
24	15	13	VREFL	VREFL	VREFL							
25	16	13	VSSA	VSSA	VSSA							
26	17	—	CMP0_IN5	CMP0_IN5	CMP0_IN5							
27	18	—	DAC0_OUT/ ADC0_SE23	DAC0_OUT/ ADC0_SE23	DAC0_OUT/ ADC0_SE23							
28	19	14	XTAL32	XTAL32	XTAL32							
29	20	15	EXTAL32	EXTAL32	EXTAL32							
30	21	16	VBAT	VBAT	VBAT							
31	—	—	PTE24	ADC0_SE17	ADC0_SE17	PTE24	CAN1_TX	TPM0_CH0	I2S1_TX_FS	LPI2C0_SCL	EWM_OUT_b	
32	—	—	PTE25	ADC0_SE18	ADC0_SE18	PTE25	CAN1_RX	TPM0_CH1	I2S1_TX_ BCLK	LPI2C0_SDA	EWM_IN	
33	—	—	PTE26/ CLKOUT32K	DISABLED		PTE26/ CLKOUT32K			I2S1_TXD0		RTC_ CLKOUT	USB_CLKIN
34	22	17	PTA0	JTAG_TCLK/ SWD_CLK		PTA0	UART0_ CTS_b	TPM0_CH5		EWM_IN		JTAG_TCLK/ SWD_CLK
35	23	18	PTA1	JTAG_TDI		PTA1	UART0_RX		CMP0_OUT	LPI2C1_ HREQ	TPM1_CH1	JTAG_TDI
36	24	19	PTA2	JTAG_TDO/ TRACE_ SWO		PTA2	UART0_TX				TPM1_CH0	JTAG_TDO/ TRACE_ SWO
37	25	20	PTA3	JTAG_TMS/ SWD_DIO		PTA3	UART0_ RTS_b	TPM0_CH0		EWM_OUT_b		JTAG_TMS/ SWD_DIO
38	26	21	PTA4/ LLWU_P3	NMI_b		PTA4/ LLWU_P3		TPM0_CH1			I2S0_MCLK	NMI_b
39	27	—	PTA5	DISABLED		PTA5	USB_CLKIN	TPM0_CH2			I2S0_TX_ BCLK	JTAG_TRST_ b
40	—	—	VDD	VDD	VDD							
41	—	—	VSS	VSS	VSS							
42	28	—	PTA12	DISABLED		PTA12	CAN0_TX	TPM1_CH0			I2S0_TXD0	
43	29	—	PTA13/ LLWU_P4	DISABLED		PTA13/ LLWU_P4	CAN0_RX	TPM1_CH1			I2S0_TX_FS	
44	—	—	PTA14	DISABLED		PTA14	SPI0_PCS0	UART0_TX			I2S0_RX_ BCLK	
45	—	—	PTA15	DISABLED		PTA15	SPI0_SCK	UART0_RX			I2S0_RXD0	
46	—	—	PTA16	DISABLED		PTA16	SPI0_SOUT	UART0_ CTS_b			I2S0_RX_FS	
47	—	—	PTA17	DISABLED		PTA17	SPI0_SIN	UART0_ RTS_b			I2S0_MCLK	
48	30	22	VDD	VDD	VDD							
49	31	23	VSS	VSS	VSS							
50	32	24	PTA18	EXTAL0	EXTAL0	PTA18			TPM_CLKIN0			

4.2 Pin properties

The following table lists the pin properties.

100LQFP	64LQFP	48QFN	Pin Name	Driver Strength	Default Status after POR	Pull-up/ pull-down Setting after POR	Slew Rate after POR	Passive Pin Filter after POR	Open Drain	Pin Interrupt
1	1	1	PTE0/ CLKOUT 32K	ND	Hi-Z	-	FS	N	N	Y
2	2	2	PTE1/ LLWU_P0	ND	Hi-Z	-	FS	N	N	Y
3		3	PTE2/ LLWU_P1	ND	Hi-Z	-	FS	N	N	Y
4		4	PTE3	ND	Hi-Z	-	FS	N	N	Y
5		5	PTE4/ LLWU_P2	ND	Hi-Z	-	FS	N	N	Y
6		6	PTE5	ND	Hi-Z	-	FS	N	N	Y
7			PTE6	ND	Hi-Z	-	FS	N	N	Y
8	3	7	VDD	-	-	-	-	-	-	-
9	4	8	VSS	-	-	-	-	-	-	-
9	4	9	VSS	-	-	-	-	-	-	-
10	5	10	USB0_DP	-	Hi-Z	-	-	-	-	-
11	6	11	USB0_DM	-	Hi-Z	-	-	-	-	-
12	7		USBVDD	-	-	-	-	-	-	-
13			NC	-	-	-	-	-	-	-
14	8		ADC0_DP1	-	Hi-Z	-	-	-	-	-
15			ADC0_DM1	-	Hi-Z	-	-	-	-	-
16			ADC0_DP2	-	Hi-Z	-	-	-	-	-
17			ADC0_DM2	-	Hi-Z	-	-	-	-	-
18	9		ADC0_DP0	-	Hi-Z	-	-	-	-	-
19	10		ADC0_DM0	-	Hi-Z	-	-	-	-	-

Table continues on the next page...

Table 9. JTAG Signal Descriptions (continued)

Chip signal name	Module signal name	Description	I/O
JTAG_TCLK	JTAG_TCLK/ SWD_CLK	JTAG Test Clock	I
JTAG_TDI	JTAG_TDI	JTAG Test Data Input	I
JTAG_TDO	JTAG_TDO/ TRACE_SWO	JTAG Test Data Output	O
JTAG_TRST	JTAG_TRST_b	JTAG Reset	I

Table 10. SWD Signal Descriptions

Chip signal name	Module signal name	Description	I/O
SWD_DIO	JTAG_TMS/ SWD_DIO	Serial Wire Data	I
SWD_CLK	JTAG_TCLK/ SWD_CLK	Serial Wire Clock	I

Table 11. TPIU Signal Descriptions

Chip signal name	Module signal name	Description	I/O
TRACE_SWO	JTAG_TDO/ TRACE_SWO	Trace output data from the ARM CoreSight debug block over a single pin	O

4.3.2 System Modules

Table 12. EWM Signal Descriptions

Chip signal name	Module signal name	Description	I/O
EWM_IN	EWM_in	EWM input for safety status of external safety circuits. The polarity of EWM_in is programmable using the EWM_CTRL[ASSIN] bit. The default polarity is active-low.	I
$\overline{\text{EWM\_OUT}}$	$\overline{\text{EWM\_out}}$	EWM reset out signal	O

Table 26. CAN 1 (for KS22 only) Signal Descriptions

Chip signal name	Module signal name	Description	I/O
CAN1_RX	CAN Rx	CAN Receive Pin	Input
CAN1_TX	CAN Tx	CAN Transmit Pin	Output

Table 27. SPI 0 Signal Descriptions

Chip signal name	Module signal name	Description	I/O
SPI0_PCS0	PCS0/$\overline{SS}$	Peripheral Chip Select 0 (O)	I/O
SPI0_PCS[3:1]	PCS[1:3]	Peripheral Chip Selects 1–3	O
SPI0_PCS4	PCS4	Peripheral Chip Select 4	O
SPI0_PCS5	PCS5/ $\overline{PCSS}$	Peripheral Chip Select 5 /Peripheral Chip Select Strobe	O
SPI0_SIN	SIN	Serial Data In	I
SPI0_SOUT	SOUT	Serial Data Out	O
SPI0_SCK	SCK	Serial Clock (O)	I/O

Table 28. SPI 1 Signal Descriptions

Chip signal name	Module signal name	Description	I/O
SPI1_PCS0	PCS0/$\overline{SS}$	Peripheral Chip Select 0 (O)	I/O
SPI1_PCS[3:1]	PCS[1:3]	Peripheral Chip Selects 1–3	O
SPI1_SIN	SIN	Serial Data In	I
SPI1_SOUT	SOUT	Serial Data Out	O
SPI1_SCK	SCK	Serial Clock (O)	I/O

Table 29. LPI^{2}C 0 Signal Descriptions

Chip signal name	Module signal name	Description	I/O
LPI2C0_SCL	SCL	LPI2C clock line.	I/O
LPI2C0_SDA	SDA	LPI2C data line.	I/O
LPI2C0_HREQ	HREQ	Host request, can initiate an LPI2C master transfer if asserted and the I2C bus is idle.	I
LPI2C0_SCLS	SCLS	Secondary I2C clock line. If LPI2C master/slave are configured to use separate pins, this the LPI2C slave SCL pin.	I/O
LPI2C0_SDAS	SDAS	Secondary I2C data line. If LPI2C master/slave are configured to use separate pins, this the LPI2C slave SDA pin.	I/O

Table 44. Power mode transition operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• LLS2 → RUN	—	—	6	µs	
	• LLS3 → RUN	—	—	6	µs	
	• VLPS → RUN	—	—	5.7	µs	
	• STOP → RUN	—	—	5.7	µs	

1. Normal boot (FTFA_FOPT[LPBOOT]=1)

5.3.2.5 Power consumption operating behaviors

The maximum values stated in the following table represent the characterized results equivalent to the mean plus three times the standard deviation (mean + 3 sigma).

NOTE

The while(1) test is executed with flash cache enabled.

Table 45. Power consumption operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA}	Analog supply current	—	—	See note	mA	1
I_{DD_HSRUN}	High Speed Run mode current - all peripheral clocks disabled, CoreMark benchmark code executing from flash					
	@ 1.8V	—	24.17	26.215	mA	2, 3, 4
	@ 3.0V	—	24.20	26.292	mA	
I_{DD_HSRUN}	High Speed Run mode current - all peripheral clocks disabled, code executing from flash					
	@ 1.8V	—	20.97	23.015	mA	2
	@ 3.0V	—	20.97	23.062	mA	
I_{DD_HSRUN}	High Speed Run mode current — all peripheral clocks enabled, code executing from flash					
	@ 1.8V	—	27.77	30.028	mA	5
	@ 3.0V	—	27.79	30.083	mA	
I_{DD_RUN}	Run mode current in Compute operation — CoreMark benchmark code executing from flash					
	@ 1.8V	—	15.58	16.790	mA	3, 4, 6
	@ 3.0V	—	16.19	17.457	mA	

Table continues on the next page...

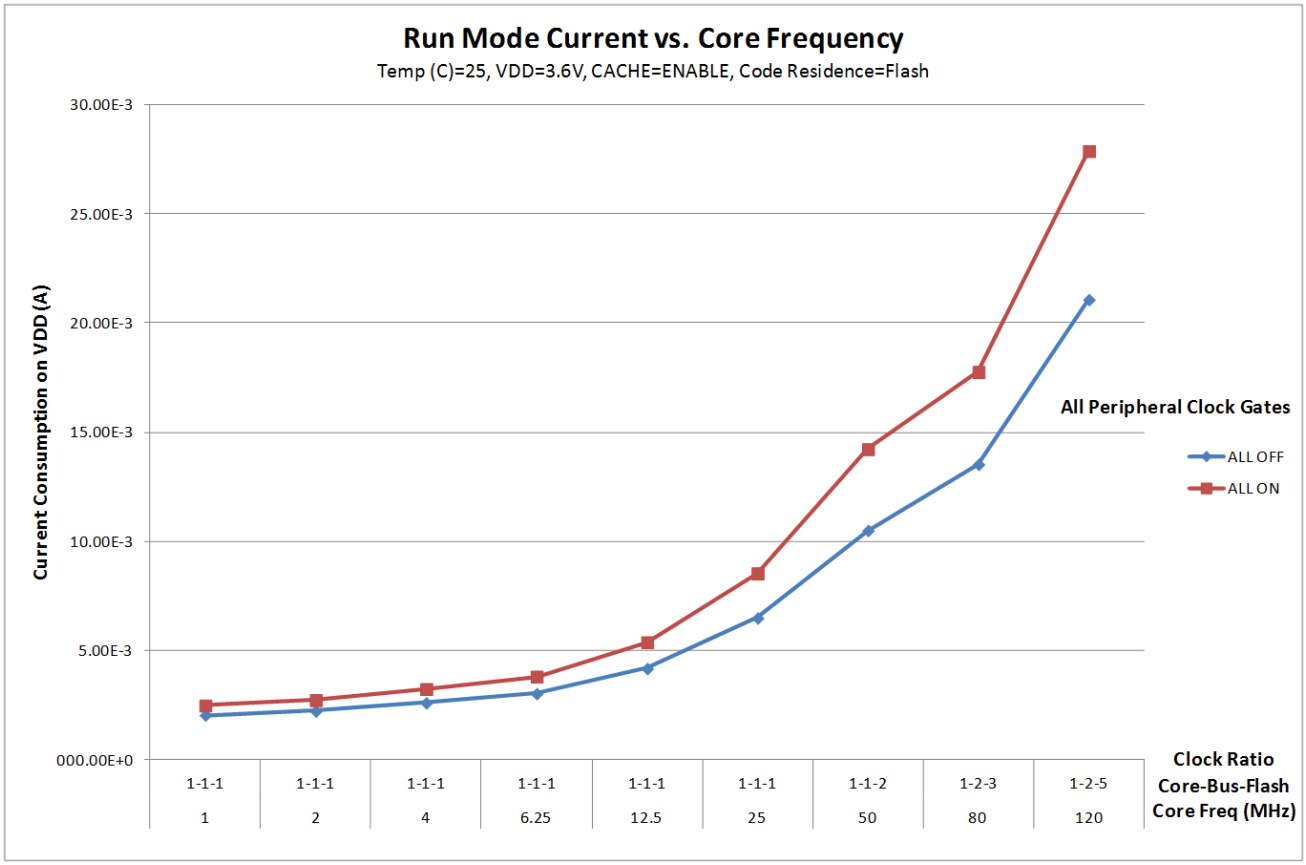

Figure 16. Run mode supply current vs. core frequency

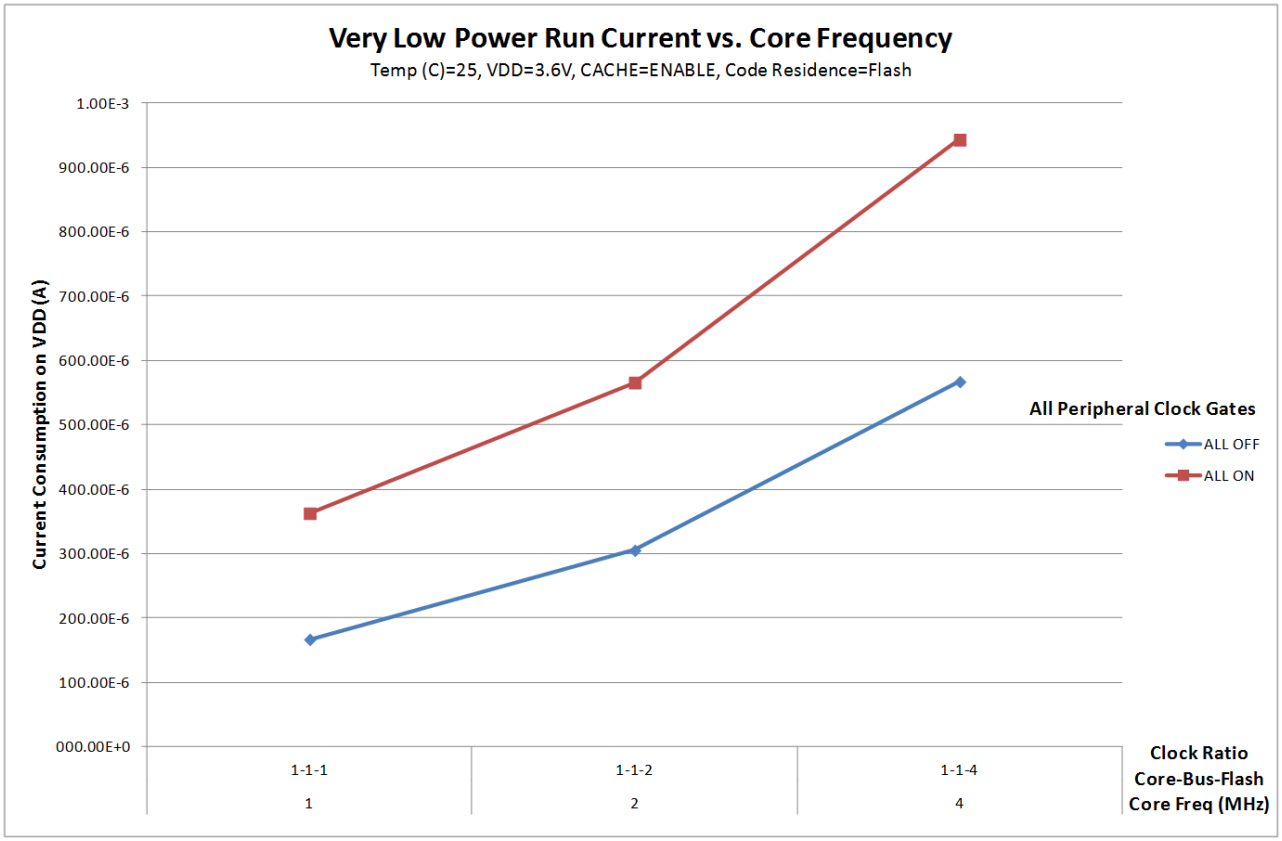

Figure 17. VLPR mode supply current vs. core frequency

5.3.2.6 EMC performance

Electromagnetic compatibility (EMC) performance is highly dependent on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components, and MCU software operation play a significant role in the EMC performance. The system designer can consult the following Freescale applications notes, available on freescale.com for advice and guidance specifically targeted at optimizing EMC performance.

- AN2321: Designing for Board Level Electromagnetic Compatibility
- AN1050: Designing for Electromagnetic Compatibility (EMC) with HCMOS Microcontrollers
- AN1263: Designing for Electromagnetic Compatibility with Single-Chip Microcontrollers

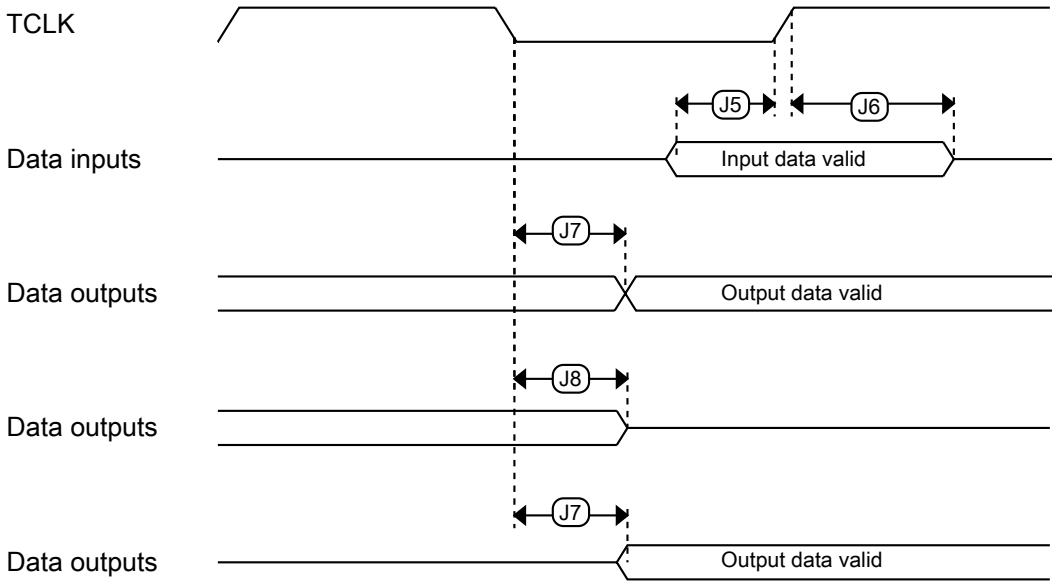

Figure 21. Boundary scan (JTAG) timing

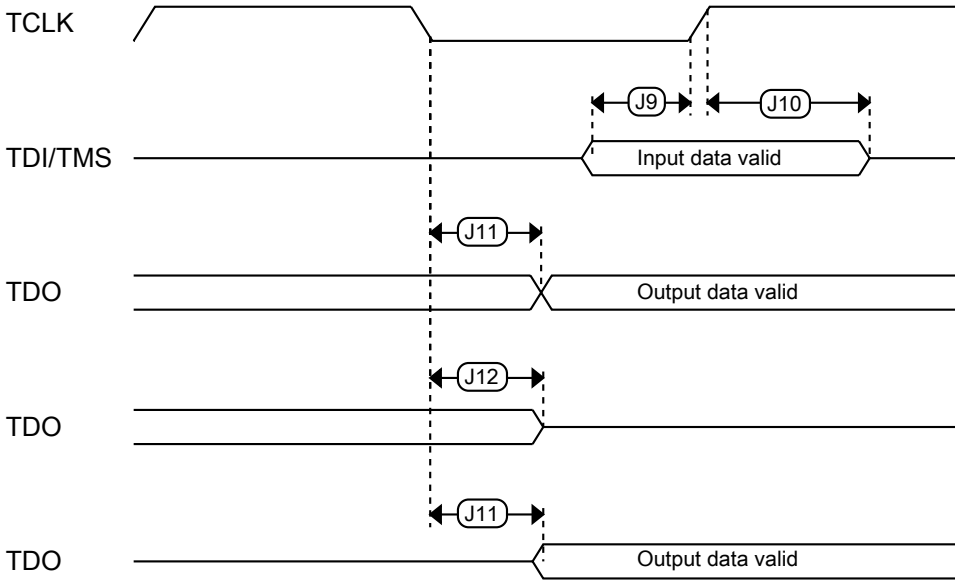

Figure 22. Test Access Port timing

Table 55. MCG specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• f_{vco} = 48 MHz • f_{vco} = 100 MHz					
D_{lock}	Lock entry frequency tolerance	± 1.49	—	± 2.98	%	
D_{unl}	Lock exit frequency tolerance	± 4.47	—	± 5.97	%	
t_{pll_lock}	Lock detector detection time	—	—	$150 \times 10^{-6} + 1075(1/f_{pll\_ref})$	s	10

1. This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
2. 2.0 V <= VDD <= 3.6 V.
3. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=0.
4. The resulting system clock frequencies should not exceed their maximum specified values. The DCO frequency deviation (Δf_{dco_t}) over voltage and temperature should be considered.
5. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=1.
6. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.
7. This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
8. Excludes any oscillator currents that are also consuming power while PLL is in operation.
9. This specification was obtained using a NXP developed PCB. PLL jitter is dependent on the noise characteristics of each PCB and results will vary.
10. This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

5.4.3.2 IRC48M specifications

Table 56. IRC48M specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	—	3.6	V	
I_{DD48M}	Supply current	—	400	500	µA	
f_{irc48m}	Internal reference frequency	—	48	—	MHz	
$\Delta f_{irc48m\_ol\_hv}$	Open loop total deviation of IRC48M frequency at high voltage (VDD=1.89V-3.6V) over 0°C to 70°C	—				
	Regulator enable (USB_CLK_RECOVER_IRC_EN[REG_EN]=1)	—	± 0.2	± 0.5	$\%f_{irc48m}$	1
$\Delta f_{irc48m\_ol\_hv}$	Open loop total deviation of IRC48M frequency at high voltage (VDD=1.89V-3.6V) over full temperature					
	Regulator enable (USB_CLK_RECOVER_IRC_EN[REG_EN]=1)	—	± 0.4	± 1.0	$\%f_{irc48m}$	1
$\Delta f_{irc48m\_ol\_lv}$	Open loop total deviation of IRC48M frequency at low voltage (VDD=1.71V-1.89V) over full temperature					1
	Regulator disable (USB_CLK_RECOVER_IRC_EN[REG_EN]=0)	—	± 0.4	± 1.0	$\%f_{irc48m}$	

Table continues on the next page...

Table 57. Oscillator DC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• 24 MHz • 32 MHz	—	4	—	mA	
C_x	EXTAL load capacitance	—	—	—		2, 3
C_y	XTAL load capacitance	—	—	—		2, 3
R_F	Feedback resistor — low-frequency, low-power mode (HGO=0)	—	—	—	MΩ	2, 4
	Feedback resistor — low-frequency, high-gain mode (HGO=1)	—	10	—	MΩ	
	Feedback resistor — high-frequency, low-power mode (HGO=0)	—	—	—	MΩ	
	Feedback resistor — high-frequency, high-gain mode (HGO=1)	—	1	—	MΩ	
R_S	Series resistor — low-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — low-frequency, high-gain mode (HGO=1)	—	200	—	kΩ	
	Series resistor — high-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — high-frequency, high-gain mode (HGO=1)	—	0	—	kΩ	
V_{pp}[5]	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1)	—	V_{DD}	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1)	—	V_{DD}	—	V	

1. V_{DD}=3.3 V, Temperature =25 °C
2. See crystal or resonator manufacturer's recommendation
3. C_x and C_y can be provided by using either integrated capacitors or external components.
4. When low-power mode is selected, R_F is integrated and must not be attached externally.
5. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other device.

Table 65. 16-bit ADC operating conditions

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
		Continuous conversions enabled, subsequent conversion time					

1. Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz, unless otherwise stated. Typical values are for reference only, and are not tested in production.
2. DC potential difference.
3. This resistance is external to MCU. To achieve the best results, the analog source resistance must be kept as low as possible. The results in this data sheet were derived from a system that had < 8 Ω analog source resistance. The R_{AS}/C_{AS} time constant should be kept to < 1 ns.
4. To use the maximum ADC conversion clock frequency, CFG2[ADHSC] must be set and CFG1[ADLPC] must be clear.
5. For guidelines and examples of conversion rate calculation, download the ADC calculator tool.

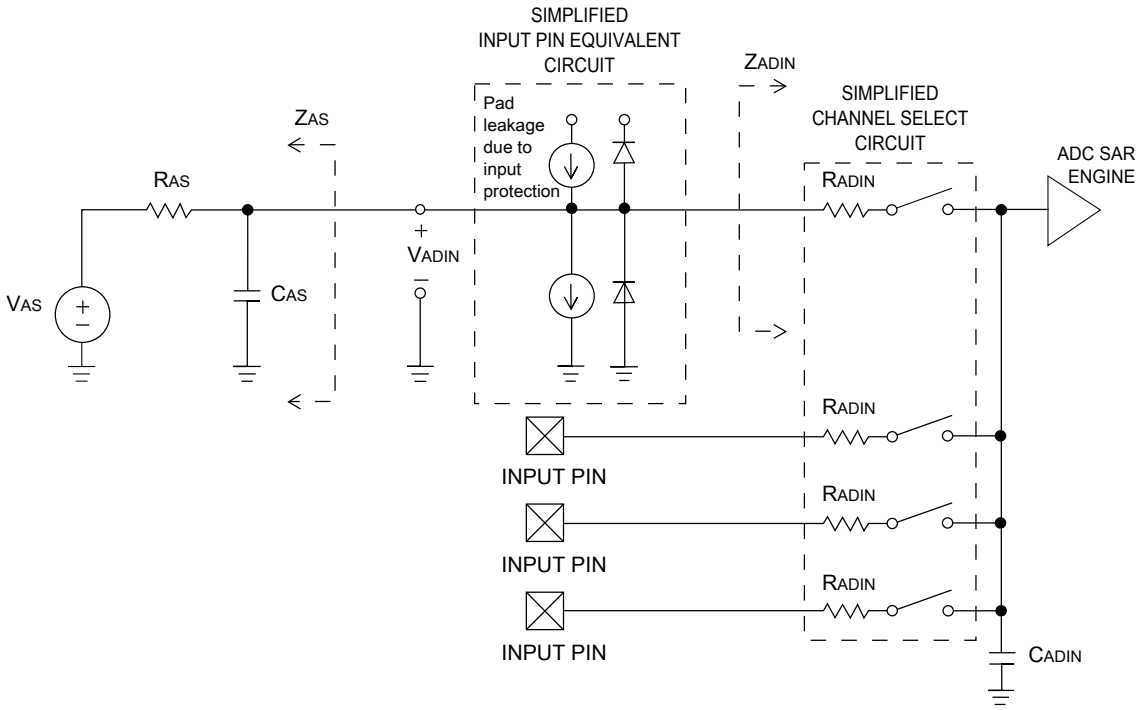

Figure 24. ADC input impedance equivalency diagram

5.4.6.1.2 16-bit ADC electrical characteristics

Table 66. 16-bit ADC characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA})

Symbol	Description	Conditions[1]	Min.	Typ.[2]	Max.	Unit	Notes
I_{DDA_ADC}	Supply current		0.215	—	1.7	mA	3
f_{ADACK}	ADC asynchronous clock source	• ADLPC = 1, ADHSC = 0	1.2	2.4	3.9	MHz	t_{ADACK} = 1/ f_{ADACK}

Table continues on the next page...

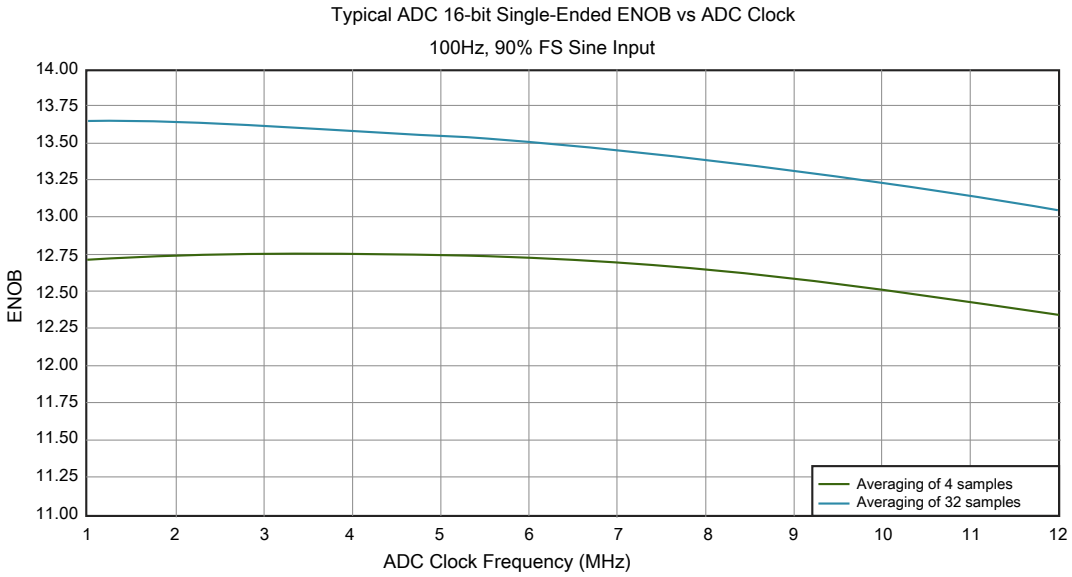

Figure 26. Typical ENOB vs. ADC_CLK for 16-bit single-ended mode

5.4.6.2 CMP and 6-bit DAC electrical specifications

Table 67. Comparator and 6-bit DAC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage	1.71	—	3.6	V
I_{DDHS}	Supply current, High-speed mode (EN=1, PMODE=1)	—	—	200	µA
I_{DDLS}	Supply current, low-speed mode (EN=1, PMODE=0)	—	—	20	µA
V_{AIN}	Analog input voltage	V_{SS} – 0.3	—	V_{DD}	V
V_{AIO}	Analog input offset voltage	—	—	20	mV
V_H	Analog comparator hysteresis[1]				
	• CR0[HYSTCTR] = 00	—	5	—	mV
	• CR0[HYSTCTR] = 01	—	10	—	mV
	• CR0[HYSTCTR] = 10	—	20	—	mV
	• CR0[HYSTCTR] = 11	—	30	—	mV
V_{CMPOh}	Output high	V_{DD} – 0.5	—	—	V
V_{CMPOl}	Output low	—	—	0.5	V
t_{DHS}	Propagation delay, high-speed mode (EN=1, PMODE=1)	20	50	200	ns
t_{DLS}	Propagation delay, low-speed mode (EN=1, PMODE=0)	80	250	600	ns
	Analog comparator initialization delay[2]	—	—	40	µs
I_{DAC6b}	6-bit DAC current adder (enabled)	—	7	—	µA
INL	6-bit DAC integral non-linearity	–0.5	—	0.5	LSB[3]
DNL	6-bit DAC differential non-linearity	–0.3	—	0.3	LSB

1. Typical hysteresis is measured with input voltage range limited to 0.6 to V_{DD}–0.6 V.

5.4.6.3.2 12-bit DAC operating behaviors

Table 69. 12-bit DAC operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA_DACLP}	Supply current — low-power mode	—	—	330	µA	
I_{DDA_DACHP}	Supply current — high-speed mode	—	—	1200	µA	
t_{DACLP}	Full-scale settling time (0x080 to 0xF7F) — low-power mode	—	100	200	µs	1
t_{DACHP}	Full-scale settling time (0x080 to 0xF7F) — high-power mode	—	15	30	µs	1
$t_{CCDACLP}$	Code-to-code settling time (0xBF8 to 0xC08) — low-power mode and high-speed mode	—	0.7	1	µs	1
$V_{dacoutl}$	DAC output voltage range low — high-speed mode, no load, DAC set to 0x000	—	—	100	mV	
$V_{dacouth}$	DAC output voltage range high — high-speed mode, no load, DAC set to 0xFFF	V_{DACR} –100	—	V_{DACR}	mV	
INL	Integral non-linearity error — high speed mode	—	—	±8	LSB	2
DNL	Differential non-linearity error — V_{DACR} > 2 V	—	—	±1	LSB	3
DNL	Differential non-linearity error — V_{DACR} = VREF_OUT	—	—	±1	LSB	4
V_{OFFSET}	Offset error	—	±0.4	±0.8	%FSR	5
E_G	Gain error	—	±0.1	±0.6	%FSR	5
PSRR	Power supply rejection ratio, V_{DDA} ≥ 2.4 V	60	—	90	dB	
T_{CO}	Temperature coefficient offset voltage	—	3.7	—	µV/C	6
T_{GE}	Temperature coefficient gain error	—	0.000421	—	%FSR/C	
Rop	Output resistance (load = 3 kΩ)	—	—	250	Ω	
SR	Slew rate -80h→ F7Fh→ 80h • High power (SP_{HP}) • Low power (SP_{LP})	 1.2 0.05	 1.7 0.12	 — —	V/µs	
BW	3dB bandwidth • High power (SP_{HP}) • Low power (SP_{LP})	 550 40	 — —	 — —	kHz	

1. Settling within ±1 LSB
2. The INL is measured for 0 + 100 mV to V_{DACR} –100 mV
3. The DNL is measured for 0 + 100 mV to V_{DACR} –100 mV
4. The DNL is measured for 0 + 100 mV to V_{DACR} –100 mV with V_{DDA} > 2.4 V
5. Calculated by a best fit curve from V_{SS} + 100 mV to V_{DACR} – 100 mV
6. V_{DDA} = 3.0 V, reference select set for V_{DDA} (DACx_CO:DACRFS = 1), high power mode (DACx_C0:LPEN = 0), DAC set to 0x800, temperature range is across the full range of the device

Table 73. Slave mode DSPI timing (full voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
	Frequency of operation	—	7.5	MHz
DS9	DSPI_SCK input cycle time	8 x t_{BUS}	—	ns
DS10	DSPI_SCK input high/low time	(t_{SCK}/2) - 4	($t_{SCK/2}$) + 4	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	29.5	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	3.2	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns
DS15	$\overline{\text{DSPI\_SS}}$ active to DSPI_SOUT driven	—	25	ns
DS16	$\overline{\text{DSPI\_SS}}$ inactive to DSPI_SOUT not driven	—	25	ns

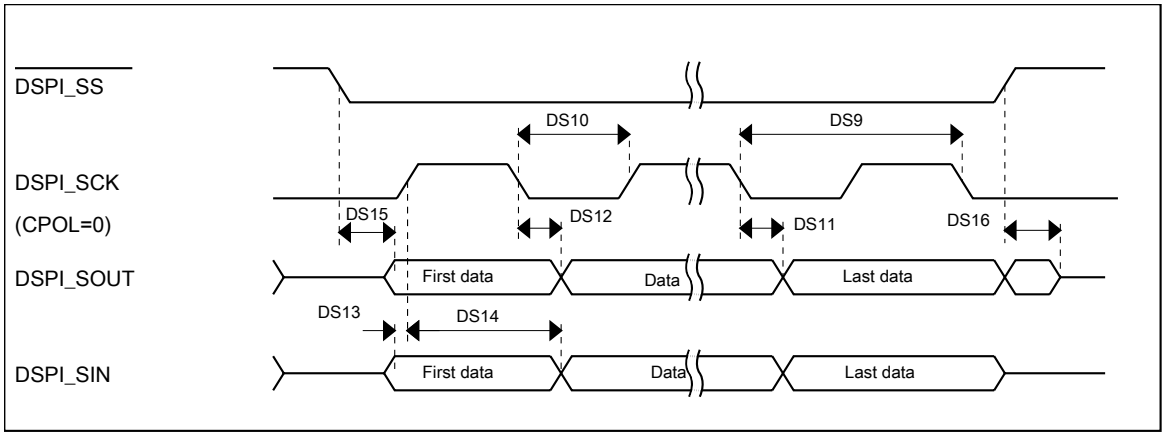

Figure 34. DSPI classic SPI timing — slave mode

5.4.8.4 LPI^{2}C

Table 74. LPI^{2}C specifications

Symbol	Description		Min.	Max.	Unit	Notes
f_{SCL}	SCL clock frequency	Standard mode (Sm)	0	100	kHz	1
		Fast mode (Fm)	0	400		1, 2
		Fast mode Plus (Fm+)	0	1000		1, 3
		Ultra Fast mode (UFm)	0	5000		1, 4
		High speed mode (Hs-mode)	0	3400		1, 5

1. See General switching specifications, measured at room temperature.
2. Measured with the maximum bus loading of 400pF at 3.3V VDD with pull-up Rp = 220Ω , and at 1.8V VDD with Rp = 880Ω. For all other cases, select appropriate Rp per I2C Bus Specification and the pin drive capability.
3. Fm+ is only supported on high drive pin with high drive enabled. It is measured with the maximum bus loading of 400pF at 3.3V VDD with Rp = 220Ω. For all other cases, select appropriate Rp per I2C Bus Specification and the pin drive capability.

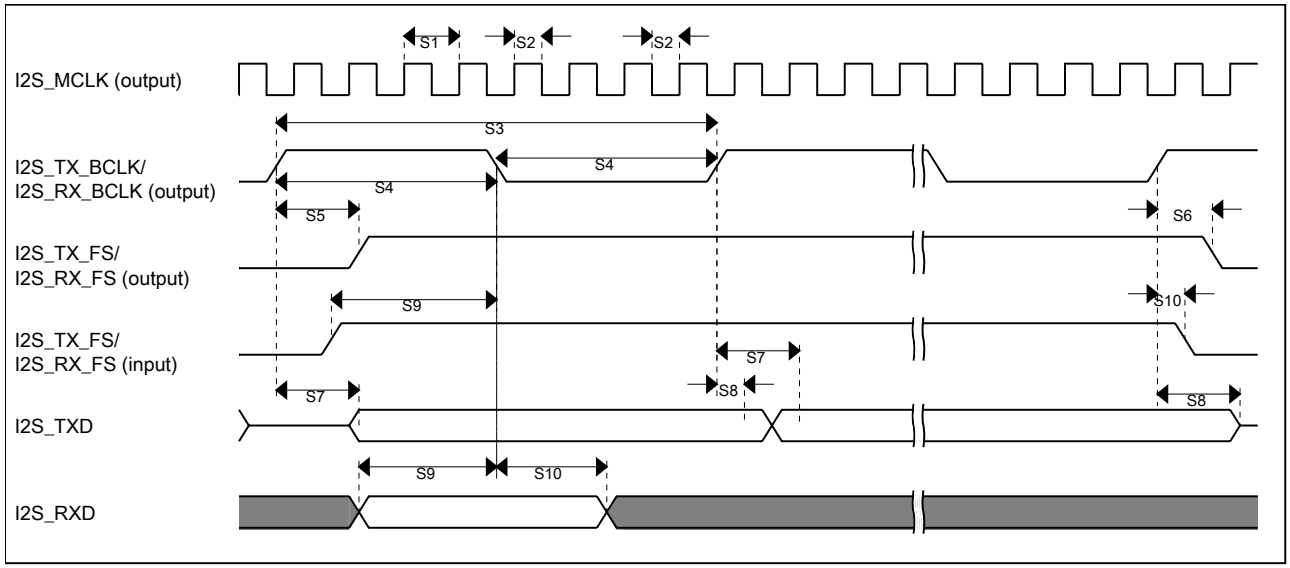

Figure 39. I2S/SAI timing — master modes

Table 80. I2S/SAI slave mode timing in VLPR, VLPW, and VLPS modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	250	—	ns
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	30	—	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	7	—	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid	—		ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	30	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK	4	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid[1]	—	72	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

Internal load capacitors (Cx, Cy) are provided in the low frequency (32.786 kHz) mode. Use the SCxP bits in the OSC0_CR register to adjust the load capacitance for the crystal. Typically, values of 10pf to 16 pF are sufficient for 32.768 kHz crystals that have a 12.5 pF CL specification. The internal load capacitor selection must not be used for high frequency crystals and resonators.

Table 81. External crystal/resonator connections

Oscillator mode	Oscillator mode
Low frequency (32.768 kHz), low power	Diagram 1
Low frequency (32.768 kHz), high gain	Diagram 2, Diagram 4
High frequency (3-32 MHz), low power	Diagram 3
High frequency (3-32 MHz), high gain	Diagram 4

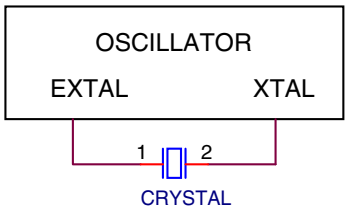

Figure 47. Crystal connection – Diagram 1

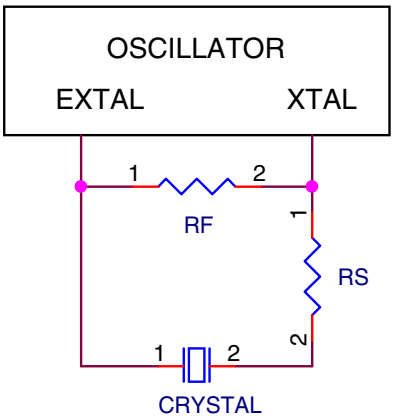

Figure 48. Crystal connection – Diagram 2

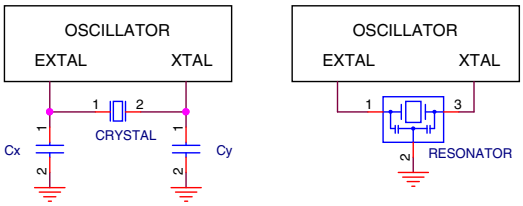

Figure 49. Crystal connection – Diagram 3