Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, I²C, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	40
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 1x16b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mks22fn128vlh12

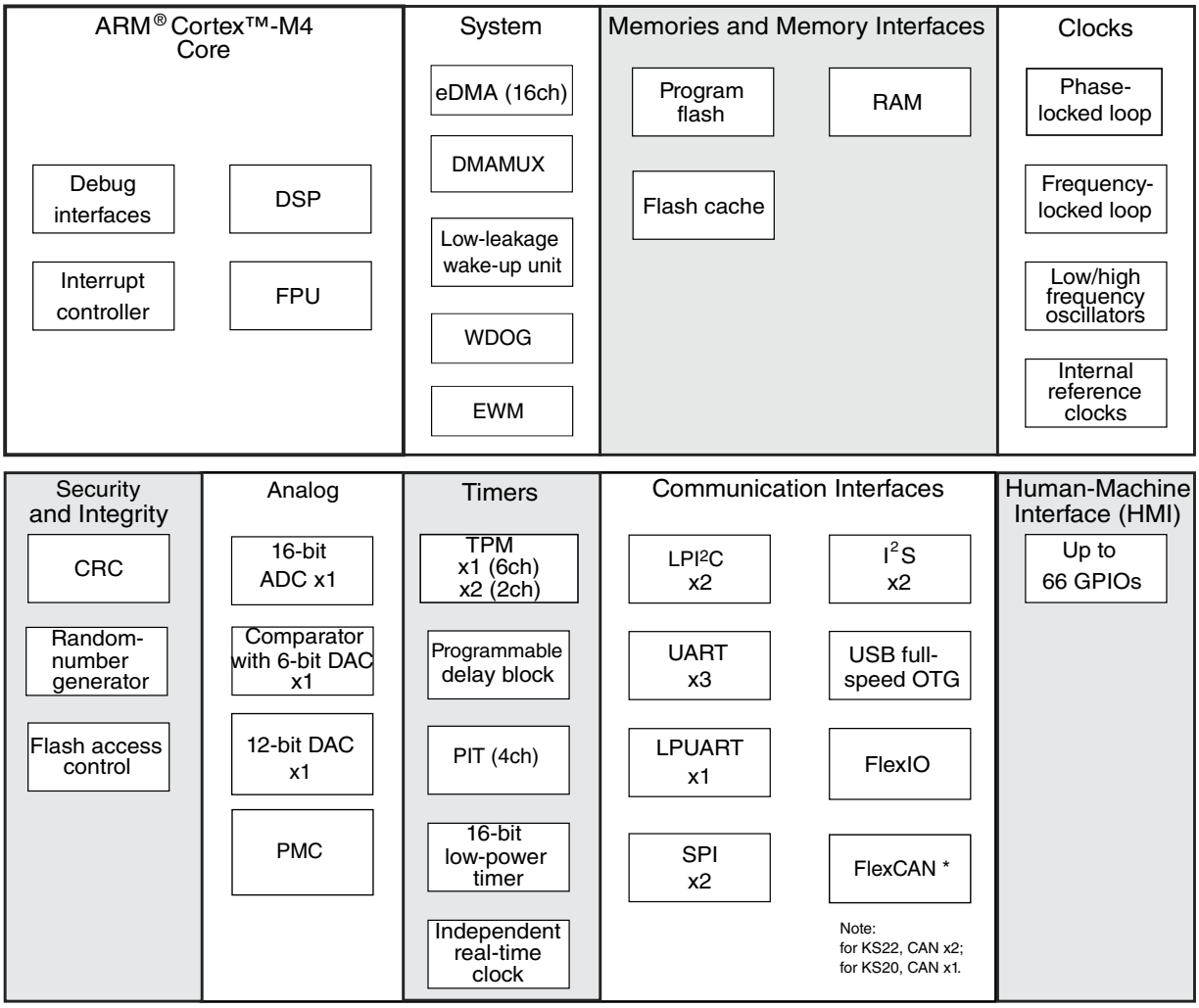

Figure 1. Functional block diagram

NOTE

DAC0 and I^2S1 are NOT supported in the 48-QFN package. For more details, see the "Signal Multiplexing and Pin Assignments" section.

1. INT: interrupt pin numbers; HD: high drive pin numbers
2. SE: single-ended; DP: differential pair
3. ADC0_DP1 is for single-ended (SE) mode only in 64-LQFP.

2 Overview

The following figure shows the system diagram of this device.

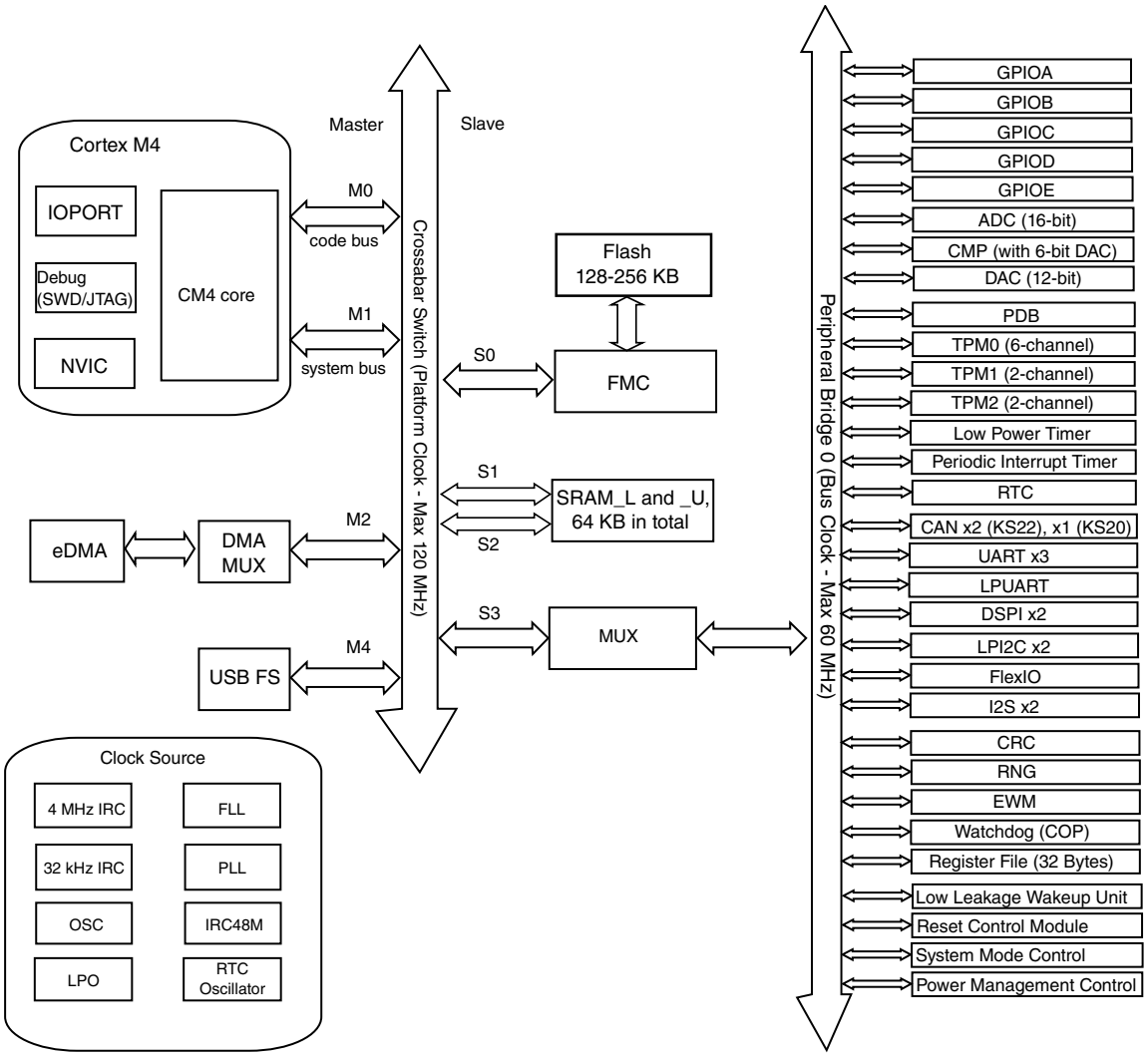

Figure 2. System diagram

The crossbar switch connects bus masters and slaves using a crossbar switch structure. This structure allows up to four bus masters to access different bus slaves simultaneously, while providing arbitration among the bus masters when they access the same slave.

2.1 System features

The following sections describe the high-level system features.

2.1.1 ARM Cortex-M4 core

The ARM Cortex-M4 is the member of the Cortex M Series of processors targeting microcontroller cores focused on very cost sensitive, deterministic, interrupt driven environments. The Cortex M4 processor is based on the ARMv7 Architecture and Thumb®-2 ISA and is upward compatible with the Cortex M3, Cortex M1, and Cortex M0 architectures. Cortex M4 improvements include an ARMv7 Thumb-2 DSP (ported from the ARMv7-A/R profile architectures) providing 32-bit instructions with SIMD (single instruction multiple data) DSP style multiply-accumulates and saturating arithmetic.

2.1.2 NVIC

The Nested Vectored Interrupt Controller supports nested interrupts and 16 priority levels for interrupts. In the NVIC, each source in the IPR registers contains 4 bits. It also differs in number of interrupt sources and supports 240 interrupt vectors.

The Cortex-M family uses a number of methods to improve interrupt latency . It also can be used to wake the MCU core from Wait and VLPW modes.

2.1.3 AWIC

The asynchronous wake-up interrupt controller (AWIC) is used to detect asynchronous wake-up events in Stop mode and signal to clock control logic to resume system clocking. After clock restarts, the NVIC observes the pending interrupt and performs the normal interrupt or event processing. The AWIC can be used to wake MCU core from Partial Stop, Stop and VLPS modes.

4 Pinouts

4.1 Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

NOTE

For KS20, only CAN0 exists. For KS22, there are two instances of CAN module (CAN0 and CAN1).

100 LQFP	64 LQFP	48 QFN	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
1	1	1	PTE0/ CLKOUT32K	ADC0_SE4a	ADC0_SE4a	PTE0/ CLKOUT32K	SPI1_PCS1	UART1_TX			LPI2C1_SDA	RTC_ CLKOUT
2	2	2	PTE1/ LLWU_P0	ADC0_SE5a	ADC0_SE5a	PTE1/ LLWU_P0	SPI1_SOUT	UART1_RX			LPI2C1_SCL	SPI1_SIN
3	—	3	PTE2/ LLWU_P1	ADC0_SE6a	ADC0_SE6a	PTE2/ LLWU_P1	SPI1_SCK	UART1_ CTS_b				
4	—	4	PTE3	ADC0_SE7a	ADC0_SE7a	PTE3	SPI1_SIN	UART1_ RTS_b				SPI1_SOUT
5	—	5	PTE4/ LLWU_P2	DISABLED		PTE4/ LLWU_P2	SPI1_PCS0	LPUART0_ TX				LPI2C1_SDA
6	—	6	PTE5	DISABLED		PTE5	SPI1_PCS2	LPUART0_ RX				LPI2C1_SCL
7	—	—	PTE6	DISABLED		PTE6	SPI1_PCS3	LPUART0_ CTS_b	I2S0_MCLK			USB_SOF_ OUT
8	3	7	VDD	VDD	VDD							
9	4	8	VSS	VSS	VSS							
10	5	9	USB0_DP	USB0_DP	USB0_DP							
11	6	10	USB0_DM	USB0_DM	USB0_DM							
12	7	11	USBVDD	USBVDD	USBVDD							
13	—	—	NC	NC	NC							
14	8	—	ADC0_DP1	ADC0_DP1	ADC0_DP1							
15	—	—	ADC0_DM1	ADC0_DM1	ADC0_DM1							
16	—	—	ADC0_DP2	ADC0_DP2	ADC0_DP2							
17	—	—	ADC0_DM2	ADC0_DM2	ADC0_DM2							
18	9	—	ADC0_DP0	ADC0_DP0	ADC0_DP0							
19	10	—	ADC0_DM0	ADC0_DM0	ADC0_DM0							
20	11	—	ADC0_DP3	ADC0_DP3	ADC0_DP3							

100 LQFP	64 LQFP	48 QFN	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
21	12	—	ADC0_DM3	ADC0_DM3	ADC0_DM3							
22	13	12	VDDA	VDDA	VDDA							
23	14	12	VREFH	VREFH	VREFH							
24	15	13	VREFL	VREFL	VREFL							
25	16	13	VSSA	VSSA	VSSA							
26	17	—	CMP0_IN5	CMP0_IN5	CMP0_IN5							
27	18	—	DAC0_OUT/ ADC0_SE23	DAC0_OUT/ ADC0_SE23	DAC0_OUT/ ADC0_SE23							
28	19	14	XTAL32	XTAL32	XTAL32							
29	20	15	EXTAL32	EXTAL32	EXTAL32							
30	21	16	VBAT	VBAT	VBAT							
31	—	—	PTE24	ADC0_SE17	ADC0_SE17	PTE24	CAN1_TX	TPM0_CH0	I2S1_TX_FS	LPI2C0_SCL	EWM_OUT_b	
32	—	—	PTE25	ADC0_SE18	ADC0_SE18	PTE25	CAN1_RX	TPM0_CH1	I2S1_TX_ BCLK	LPI2C0_SDA	EWM_IN	
33	—	—	PTE26/ CLKOUT32K	DISABLED		PTE26/ CLKOUT32K			I2S1_TXD0		RTC_ CLKOUT	USB_CLKIN
34	22	17	PTA0	JTAG_TCLK/ SWD_CLK		PTA0	UART0_ CTS_b	TPM0_CH5		EWM_IN		JTAG_TCLK/ SWD_CLK
35	23	18	PTA1	JTAG_TDI		PTA1	UART0_RX		CMP0_OUT	LPI2C1_ HREQ	TPM1_CH1	JTAG_TDI
36	24	19	PTA2	JTAG_TDO/ TRACE_ SWO		PTA2	UART0_TX				TPM1_CH0	JTAG_TDO/ TRACE_ SWO
37	25	20	PTA3	JTAG_TMS/ SWD_DIO		PTA3	UART0_ RTS_b	TPM0_CH0		EWM_OUT_b		JTAG_TMS/ SWD_DIO
38	26	21	PTA4/ LLWU_P3	NMI_b		PTA4/ LLWU_P3		TPM0_CH1			I2S0_MCLK	NMI_b
39	27	—	PTA5	DISABLED		PTA5	USB_CLKIN	TPM0_CH2			I2S0_TX_ BCLK	JTAG_TRST_ b
40	—	—	VDD	VDD	VDD							
41	—	—	VSS	VSS	VSS							
42	28	—	PTA12	DISABLED		PTA12	CAN0_TX	TPM1_CH0			I2S0_TXD0	
43	29	—	PTA13/ LLWU_P4	DISABLED		PTA13/ LLWU_P4	CAN0_RX	TPM1_CH1			I2S0_TX_FS	
44	—	—	PTA14	DISABLED		PTA14	SPI0_PCS0	UART0_TX			I2S0_RX_ BCLK	
45	—	—	PTA15	DISABLED		PTA15	SPI0_SCK	UART0_RX			I2S0_RXD0	
46	—	—	PTA16	DISABLED		PTA16	SPI0_SOUT	UART0_ CTS_b			I2S0_RX_FS	
47	—	—	PTA17	DISABLED		PTA17	SPI0_SIN	UART0_ RTS_b			I2S0_MCLK	
48	30	22	VDD	VDD	VDD							
49	31	23	VSS	VSS	VSS							
50	32	24	PTA18	EXTAL0	EXTAL0	PTA18			TPM_CLKIN0			

4.2 Pin properties

The following table lists the pin properties.

100LQFP	64LQFP	48QFN	Pin Name	Driver Strength	Default Status after POR	Pull-up/ pull-down Setting after POR	Slew Rate after POR	Passive Pin Filter after POR	Open Drain	Pin Interrupt
1	1	1	PTE0/ CLKOUT 32K	ND	Hi-Z	-	FS	N	N	Y
2	2	2	PTE1/ LLWU_P0	ND	Hi-Z	-	FS	N	N	Y
3		3	PTE2/ LLWU_P1	ND	Hi-Z	-	FS	N	N	Y
4		4	PTE3	ND	Hi-Z	-	FS	N	N	Y
5		5	PTE4/ LLWU_P2	ND	Hi-Z	-	FS	N	N	Y
6		6	PTE5	ND	Hi-Z	-	FS	N	N	Y
7			PTE6	ND	Hi-Z	-	FS	N	N	Y
8	3	7	VDD	-	-	-	-	-	-	-
9	4	8	VSS	-	-	-	-	-	-	-
9	4	9	VSS	-	-	-	-	-	-	-
10	5	10	USB0_DP	-	Hi-Z	-	-	-	-	-
11	6	11	USB0_DM	-	Hi-Z	-	-	-	-	-
12	7		USBVDD	-	-	-	-	-	-	-
13			NC	-	-	-	-	-	-	-
14	8		ADC0_DP1	-	Hi-Z	-	-	-	-	-
15			ADC0_DM1	-	Hi-Z	-	-	-	-	-
16			ADC0_DP2	-	Hi-Z	-	-	-	-	-
17			ADC0_DM2	-	Hi-Z	-	-	-	-	-
18	9		ADC0_DP0	-	Hi-Z	-	-	-	-	-
19	10		ADC0_DM0	-	Hi-Z	-	-	-	-	-

Table continues on the next page...

100LQFP	64LQFP	48QFN	Pin Name	Driver Strength	Default Status after POR	Pull-up/ pull-down Setting after POR	Slew Rate after POR	Passive Pin Filter after POR	Open Drain	Pin Interrupt
47			PTA17	ND	Hi-Z	-	FS	N	N	Y
48	30	22	VDD	-	-	-	-	-	-	-
49	31	23	VSS	-	-	-	-	-	-	-
50	32	24	PTA18	ND	Hi-Z	-	FS	N	N	Y
51	33	25	PTA19	ND	Hi-Z	-	FS	N	N	Y
52	34	26	RESET_b	-	H	PU	-	Y	N	-
53	35	27	PTB0/ LLWU_P5	HD	Hi-Z	-	FS	N	N	Y
54	36	28	PTB1	HD	Hi-Z	-	FS	N	N	Y
55	37	29	PTB2	ND	Hi-Z	-	FS	N	N	Y
56	38	30	PTB3	ND	Hi-Z	-	FS	N	N	Y
57			PTB9	ND	Hi-Z	-	FS	N	N	Y
58			PTB10	ND	Hi-Z	-	FS	N	N	Y
59			PTB11	ND	Hi-Z	-	FS	N	N	Y
60			VSS	-	-	-	-	-	-	-
61			VDD	-	-	-	-	-	-	-
62	39	31	PTB16	ND	Hi-Z	-	FS	N	N	Y
63	40		PTB17	ND	Hi-Z	-	FS	N	N	Y
64	41	32	PTB18	ND	Hi-Z	-	FS	N	N	Y
65	42	33	PTB19	ND	Hi-Z	-	FS	N	N	Y
66			PTB20	ND	Hi-Z	-	FS	N	N	Y
67			PTB21	ND	Hi-Z	-	FS	N	N	Y
68			PTB22	ND	Hi-Z	-	FS	N	N	Y
69			PTB23	ND	Hi-Z	-	FS	N	N	Y
70	43		PTC0	ND	Hi-Z	-	FS	N	N	Y
71	44	34	PTC1/ LLWU_P6	ND	Hi-Z	-	FS	N	N	Y
72	45	35	PTC2	ND	Hi-Z	-	FS	N	N	Y
73	46	36	PTC3/ LLWU_P7	HD	Hi-Z	-	FS	N	N	Y
74	47		VSS	-	-	-	-	-	-	-
75	48		VDD	-	-	-	-	-	-	-

Table continues on the next page...

100LQFP	64LQFP	48QFN	Pin Name	Driver Strength	Default Status after POR	Pull-up/ pull-down Setting after POR	Slew Rate after POR	Passive Pin Filter after POR	Open Drain	Pin Interrupt
100	64	48	PTD7	HD	Hi-Z	-	FS	N	N	Y

Properties	Abbreviation	Descriptions
Driver strength	ND	Normal drive
	HD	High drive
Default status after POR	Hi-Z	High impendence
	H	High level
	L	Low level
Pull-up/pull-down setting after POR	PU	Pull-up
	PD	Pull-down
Slew rate after POR	FS	Fast slew rate
	SS	Slow slew rate
Passive Pin Filter after POR	N	Disabled
	Y	Enabled
Open drain	N	Disabled[1]
	Y	Enabled
Pin interrupt	Y	Yes

1. When UART or LPUART module is enabled and a pin is functional for UART or LPUART, this pin is (pseudo-) open drain configurable.

4.3 Module Signal Description Tables

The following sections correlate the chip-level signal name with the signal name used in the module's chapter. They also briefly describe the signal function and direction.

4.3.1 Core Modules

Table 9. JTAG Signal Descriptions

Chip signal name	Module signal name	Description	I/O
JTAG_TMS	JTAG_TMS/ SWD_DIO	JTAG Test Mode Selection	I

Table continues on the next page...

Table 26. CAN 1 (for KS22 only) Signal Descriptions

Chip signal name	Module signal name	Description	I/O
CAN1_RX	CAN Rx	CAN Receive Pin	Input
CAN1_TX	CAN Tx	CAN Transmit Pin	Output

Table 27. SPI 0 Signal Descriptions

Chip signal name	Module signal name	Description	I/O
SPI0_PCS0	PCS0/$\overline{SS}$	Peripheral Chip Select 0 (O)	I/O
SPI0_PCS[3:1]	PCS[1:3]	Peripheral Chip Selects 1–3	O
SPI0_PCS4	PCS4	Peripheral Chip Select 4	O
SPI0_PCS5	PCS5/ $\overline{PCSS}$	Peripheral Chip Select 5 /Peripheral Chip Select Strobe	O
SPI0_SIN	SIN	Serial Data In	I
SPI0_SOUT	SOUT	Serial Data Out	O
SPI0_SCK	SCK	Serial Clock (O)	I/O

Table 28. SPI 1 Signal Descriptions

Chip signal name	Module signal name	Description	I/O
SPI1_PCS0	PCS0/$\overline{SS}$	Peripheral Chip Select 0 (O)	I/O
SPI1_PCS[3:1]	PCS[1:3]	Peripheral Chip Selects 1–3	O
SPI1_SIN	SIN	Serial Data In	I
SPI1_SOUT	SOUT	Serial Data Out	O
SPI1_SCK	SCK	Serial Clock (O)	I/O

Table 29. LPI^{2}C 0 Signal Descriptions

Chip signal name	Module signal name	Description	I/O
LPI2C0_SCL	SCL	LPI2C clock line.	I/O
LPI2C0_SDA	SDA	LPI2C data line.	I/O
LPI2C0_HREQ	HREQ	Host request, can initiate an LPI2C master transfer if asserted and the I2C bus is idle.	I
LPI2C0_SCLS	SCLS	Secondary I2C clock line. If LPI2C master/slave are configured to use separate pins, this the LPI2C slave SCL pin.	I/O
LPI2C0_SDAS	SDAS	Secondary I2C data line. If LPI2C master/slave are configured to use separate pins, this the LPI2C slave SDA pin.	I/O

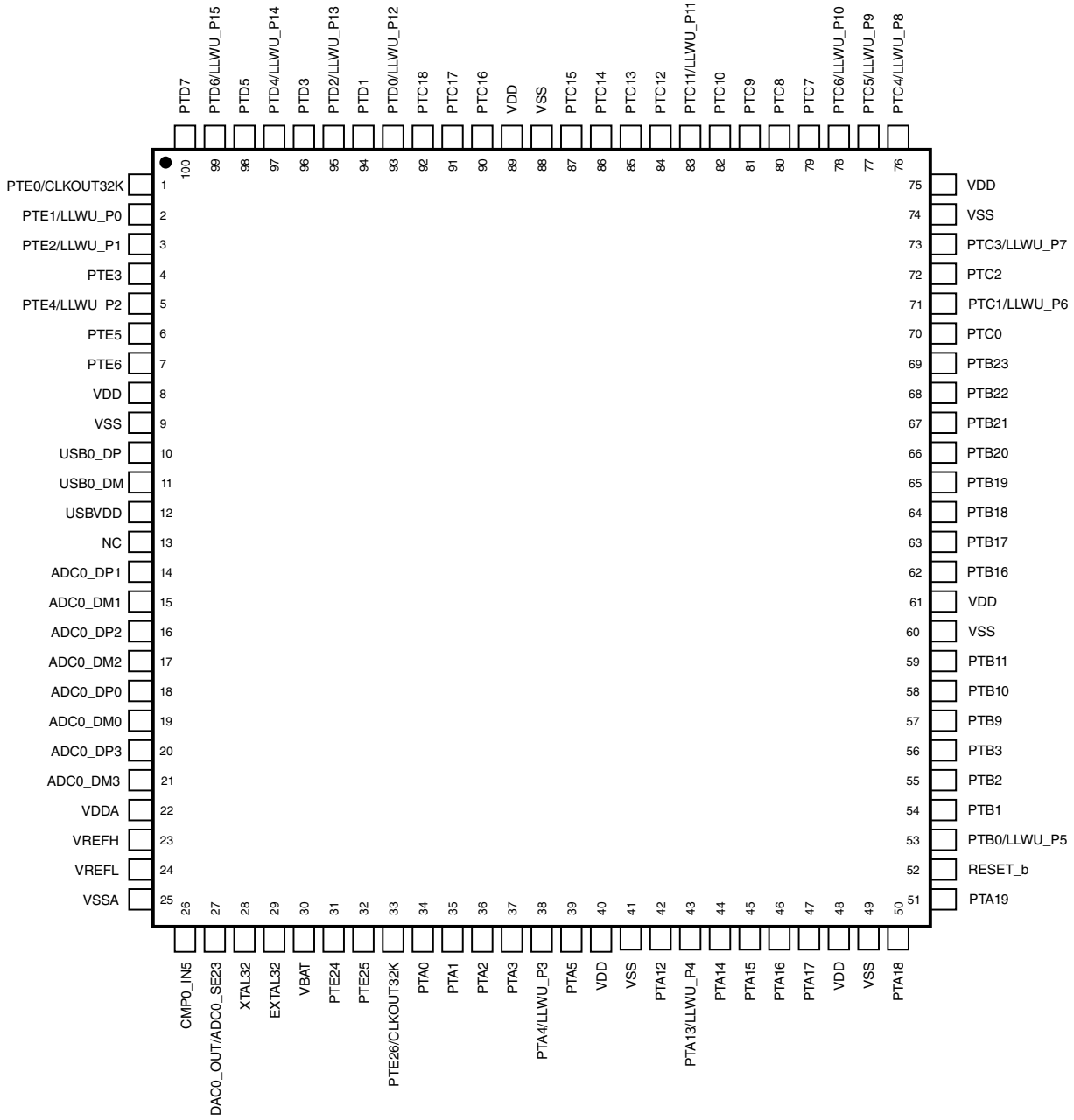

Figure 6. 100 LQFP Pinout Diagram

5.2.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

5.2.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	-2000	+2000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model	-500	+500	V	2
I_{LAT}	Latch-up current at ambient temperature of 105°C	-100	+100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

5.2.4 Voltage and current operating ratings

Table 39. Voltage and current operating ratings

Symbol	Description	Min.	Max.	Unit
V_{DD}	Digital supply voltage	–0.3	3.8	V
I_{DD}	Digital supply current	—	120	mA
V_{IO}	IO pin input voltage	–0.3	V_{DD} + 0.3	V
I_D	Instantaneous maximum current single pin limit (applies to all port pins)	–25	25	mA
V_{DDA}	Analog supply voltage	V_{DD} – 0.3	V_{DD} + 0.3	V
V_{USB_DP}	USB_DP input voltage	–0.3	3.63	V
V_{USB_DM}	USB_DM input voltage	–0.3	3.63	V
V_{BAT}	RTC battery supply voltage	–0.3	3.8	V

5.3 General

5.3.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

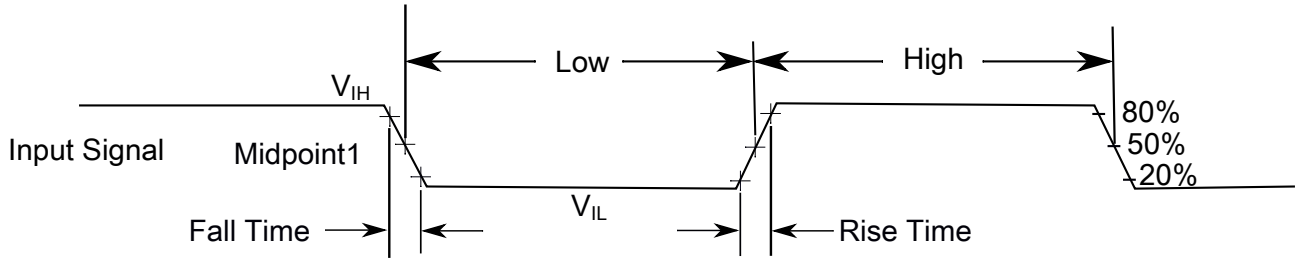

Figure 15. Input signal measurement reference

All digital I/O switching characteristics, unless otherwise specified, assume that the output pins have the following characteristics.

- C_L=30 pF loads
- Slew rate disabled
- Normal drive strength

5.3.2 Nonswitching electrical specifications

5.3.2.1 Voltage and current operating requirements

Table 40. Voltage and current operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	3.6	V	
V_{DDA}	Analog supply voltage	1.71	3.6	V	
$V_{DD} – V_{DDA}$	V_{DD}-to-V_{DDA} differential voltage	–0.1	0.1	V	
$V_{SS} – V_{SSA}$	V_{SS}-to-V_{SSA} differential voltage	–0.1	0.1	V	
V_{BAT}	RTC battery supply voltage	1.71	3.6	V	
$USBV_{DD}$	USB Transceiver supply voltage	3.0	3.6	V	1
V_{IH}	Input high voltage • 2.7 V ≤ V_{DD} ≤ 3.6 V • 1.7 V ≤ V_{DD} ≤ 2.7 V	0.7 × V_{DD} 0.75 × V_{DD}	— —	V V	

Table continues on the next page...

Table 53. JTAG limited voltage range electricals (continued)

Symbol	Description	Min.	Max.	Unit
J11	TCLK low to TDO data valid	—	19	ns
J12	TCLK low to TDO high-Z	—	19	ns
J13	$\overline{\text{TRST}}$ assert time	100	—	ns
J14	$\overline{\text{TRST}}$ setup time (negation) to TCLK high	8	—	ns

Table 54. JTAG full voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
J1	TCLK frequency of operation			MHz
	• Boundary Scan	0	10	
	• JTAG and CJTAG	0	15	
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width			
	• Boundary Scan	50	—	ns
	• JTAG and CJTAG	33	—	ns
J4	TCLK rise and fall times	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	1.4	—	ns
J7	TCLK low to boundary scan output data valid	—	27	ns
J8	TCLK low to boundary scan output high-Z	—	27	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	1.4	—	ns
J11	TCLK low to TDO data valid	—	26.2	ns
J12	TCLK low to TDO high-Z	—	26.2	ns
J13	$\overline{\text{TRST}}$ assert time	100	—	ns
J14	$\overline{\text{TRST}}$ setup time (negation) to TCLK high	8	—	ns

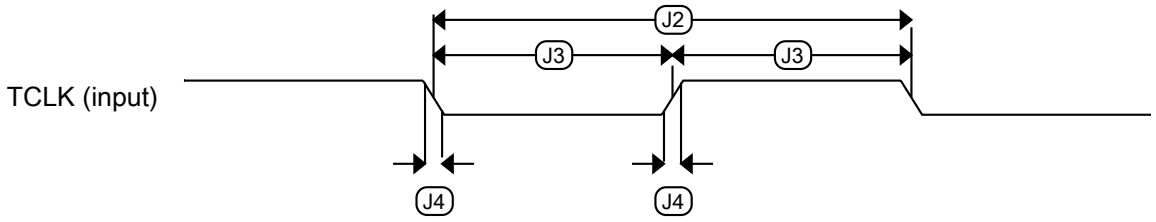

Figure 20. Test clock input timing

5.4.6 Analog

5.4.6.1 ADC electrical specifications

The 16-bit accuracy specifications listed in Table 65 and Table 66 are achievable on the differential pins ADCx_DPx, ADCx_DMx.

All other ADC channels meet the 13-bit differential/12-bit single-ended accuracy specifications.

5.4.6.1.1 16-bit ADC operating conditions

Table 65. 16-bit ADC operating conditions

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
V_{DDA}	Supply voltage	Absolute	1.71	—	3.6	V	
ΔV_{DDA}	Supply voltage	Delta to V_{DD} (V_{DD} – V_{DDA})	-100	0	+100	mV	2
ΔV_{SSA}	Ground voltage	Delta to V_{SS} (V_{SS} – V_{SSA})	-100	0	+100	mV	2
V_{REFH}	ADC reference voltage high		1.13	V_{DDA}	V_{DDA}	V	
V_{REFL}	ADC reference voltage low		V_{SSA}	V_{SSA}	V_{SSA}	V	
V_{ADIN}	Input voltage	• 16-bit differential mode • All other modes	VREFL VREFL	— —	31/32 * VREFH VREFH	V	
C_{ADIN}	Input capacitance	• 16-bit mode • 8-bit / 10-bit / 12-bit modes	— —	8 4	10 5	pF	
R_{ADIN}	Input series resistance		—	2	5	kΩ	
R_{AS}	Analog source resistance (external)	13-bit / 12-bit modes f_{ADCK} < 4 MHz	—	—	5	kΩ	3
f_{ADCK}	ADC conversion clock frequency	≤ 13-bit mode	1.0	—	24.0	MHz	4
f_{ADCK}	ADC conversion clock frequency	16-bit mode	2.0	—	12.0	MHz	4
C_{rate}	ADC conversion rate	≤ 13-bit modes No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	20	—	1200	Ksps	5
C_{rate}	ADC conversion rate	16-bit mode No ADC hardware averaging	37	—	461	Ksps	5

Table 66. 16-bit ADC characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA}) (continued)

Symbol	Description	Conditions[1]	Min.	Typ.[2]	Max.	Unit	Notes
		• ADLPC = 1, ADHSC = 1 • ADLPC = 0, ADHSC = 0 • ADLPC = 0, ADHSC = 1	2.4 3.0 4.4	4.0 5.2 6.2	6.1 7.3 9.5	MHz MHz MHz	
	Sample Time	See Reference Manual chapter for sample times					
TUE	Total unadjusted error	• 12-bit modes • <12-bit modes	— —	±4 ±1.4	±6.8 ±2.1	LSB[4]	5
DNL	Differential non-linearity	• 12-bit modes • <12-bit modes	— —	±0.7 ±0.2	–1.1 to +1.9 –0.3 to 0.5	LSB[4]	5
INL	Integral non-linearity	• 12-bit modes • <12-bit modes	— —	±1.0 ±0.5	–2.7 to +1.9 –0.7 to +0.5	LSB[4]	5
E_{FS}	Full-scale error	• 12-bit modes • <12-bit modes	— —	–4 –1.4	–5.4 –1.8	LSB[4]	V_{ADIN} = V_{DDA}[5]
E_Q	Quantization error	• 16-bit modes • ≤13-bit modes	— —	–1 to 0 —	— ±0.5	LSB[4]	
ENOB	Effective number of bits	16-bit differential mode • Avg = 32 • Avg = 4 16-bit single-ended mode • Avg = 32 • Avg = 4	 12.8 11.9 12.2 11.4	 14.5 13.8 13.9 13.1	 — — — —	 bits bits bits bits	6
SINAD	Signal-to-noise plus distortion	See ENOB	6.02 × ENOB + 1.76			dB	
THD	Total harmonic distortion	16-bit differential mode • Avg = 32 16-bit single-ended mode • Avg = 32	 — —	 -94 -85	 — —	dB dB 	7
SFDR	Spurious free dynamic range	16-bit differential mode • Avg = 32 16-bit single-ended mode • Avg = 32	 82 78	 95 90	 — — 	 dB dB 	7

Table continues on the next page...

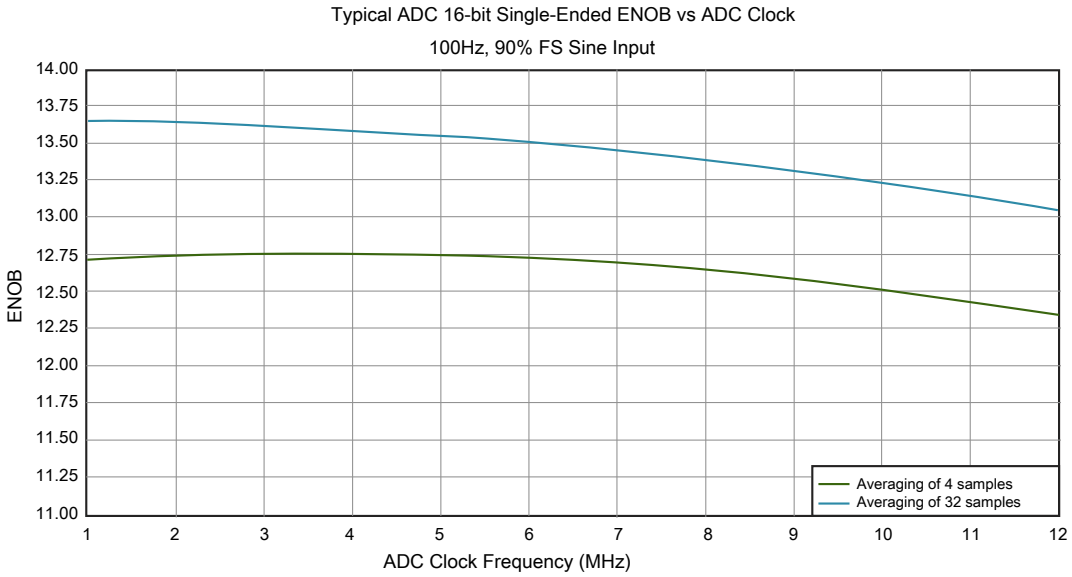

Figure 26. Typical ENOB vs. ADC_CLK for 16-bit single-ended mode

5.4.6.2 CMP and 6-bit DAC electrical specifications

Table 67. Comparator and 6-bit DAC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage	1.71	—	3.6	V
I_{DDHS}	Supply current, High-speed mode (EN=1, PMODE=1)	—	—	200	µA
I_{DDLS}	Supply current, low-speed mode (EN=1, PMODE=0)	—	—	20	µA
V_{AIN}	Analog input voltage	V_{SS} – 0.3	—	V_{DD}	V
V_{AIO}	Analog input offset voltage	—	—	20	mV
V_H	Analog comparator hysteresis[1]				
	• CR0[HYSTCTR] = 00	—	5	—	mV
	• CR0[HYSTCTR] = 01	—	10	—	mV
	• CR0[HYSTCTR] = 10	—	20	—	mV
	• CR0[HYSTCTR] = 11	—	30	—	mV
V_{CMPOh}	Output high	V_{DD} – 0.5	—	—	V
V_{CMPOl}	Output low	—	—	0.5	V
t_{DHS}	Propagation delay, high-speed mode (EN=1, PMODE=1)	20	50	200	ns
t_{DLS}	Propagation delay, low-speed mode (EN=1, PMODE=0)	80	250	600	ns
	Analog comparator initialization delay[2]	—	—	40	µs
I_{DAC6b}	6-bit DAC current adder (enabled)	—	7	—	µA
INL	6-bit DAC integral non-linearity	–0.5	—	0.5	LSB[3]
DNL	6-bit DAC differential non-linearity	–0.3	—	0.3	LSB

1. Typical hysteresis is measured with input voltage range limited to 0.6 to V_{DD}–0.6 V.

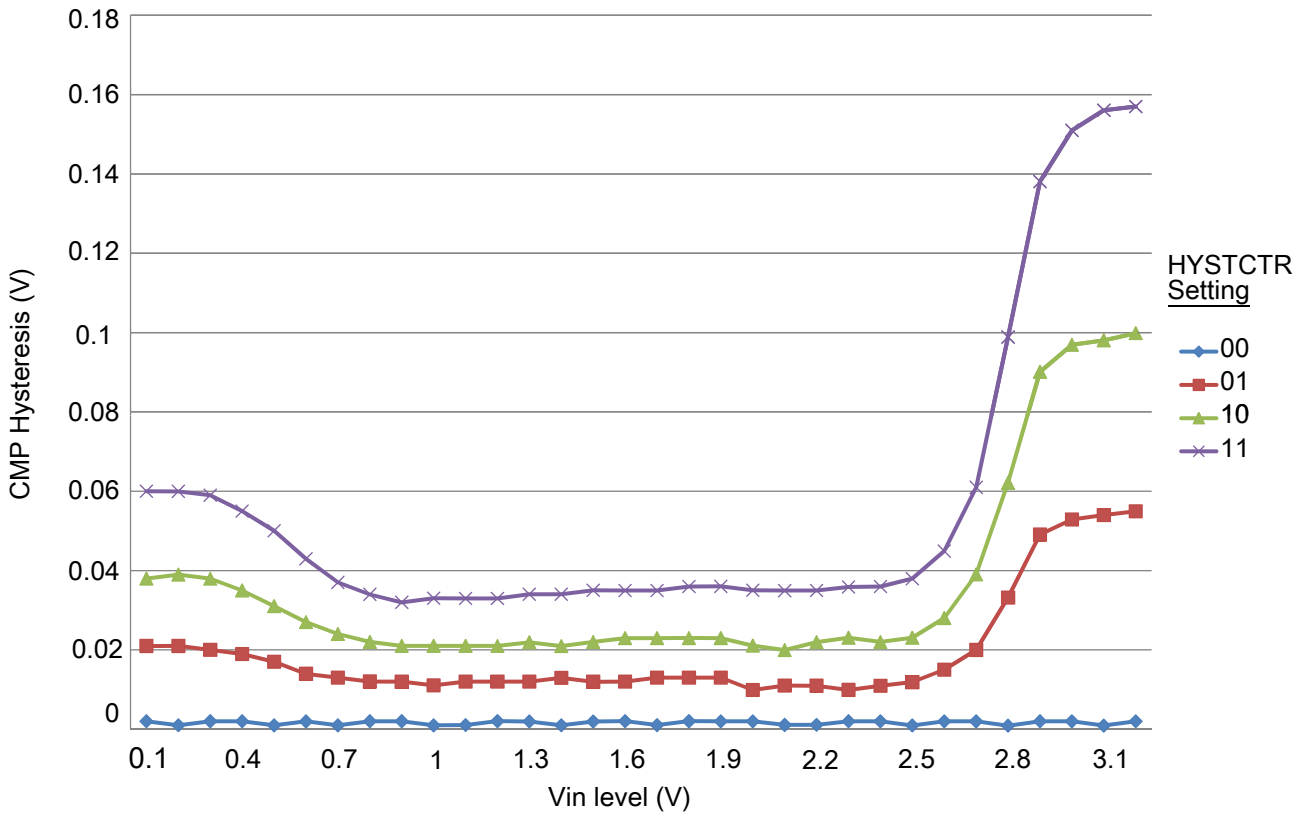

Figure 28. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 1)

5.4.6.3 12-bit DAC electrical characteristics

5.4.6.3.1 12-bit DAC operating requirements

Table 68. 12-bit DAC operating requirements

Symbol	Desciption	Min.	Max.	Unit	Notes
V_{DDA}	Supply voltage	1.71	3.6	V	
V_{DACR}	Reference voltage	1.13	3.6	V	1
C_L	Output load capacitance	—	100	pF	2
I_L	Output load current	—	1	mA	

1. The DAC reference can be selected to be V_{DDA} or VREFH.
2. A small load capacitance (47 pF) can improve the bandwidth performance of the DAC

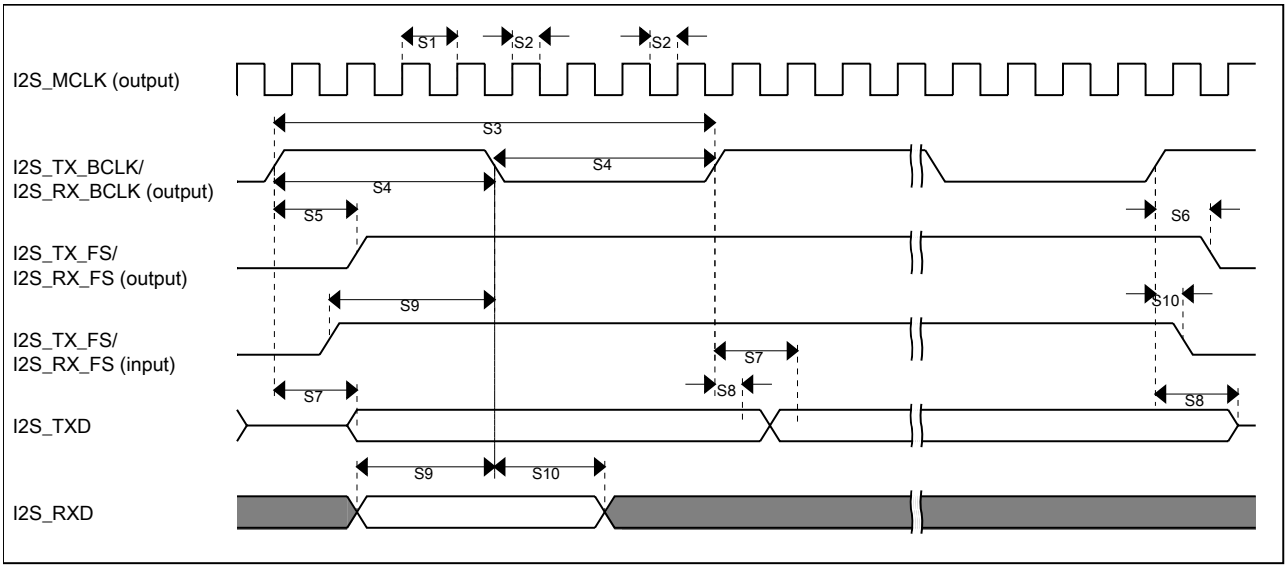

Figure 35. I2S/SAI timing — master modes

Table 76. I2S/SAI slave mode timing in Normal Run, Wait and Stop modes (limited voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	80	—	ns
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	4.5	—	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	2	—	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid	—	20	ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	4.5	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK	2	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid[1]	—	25	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

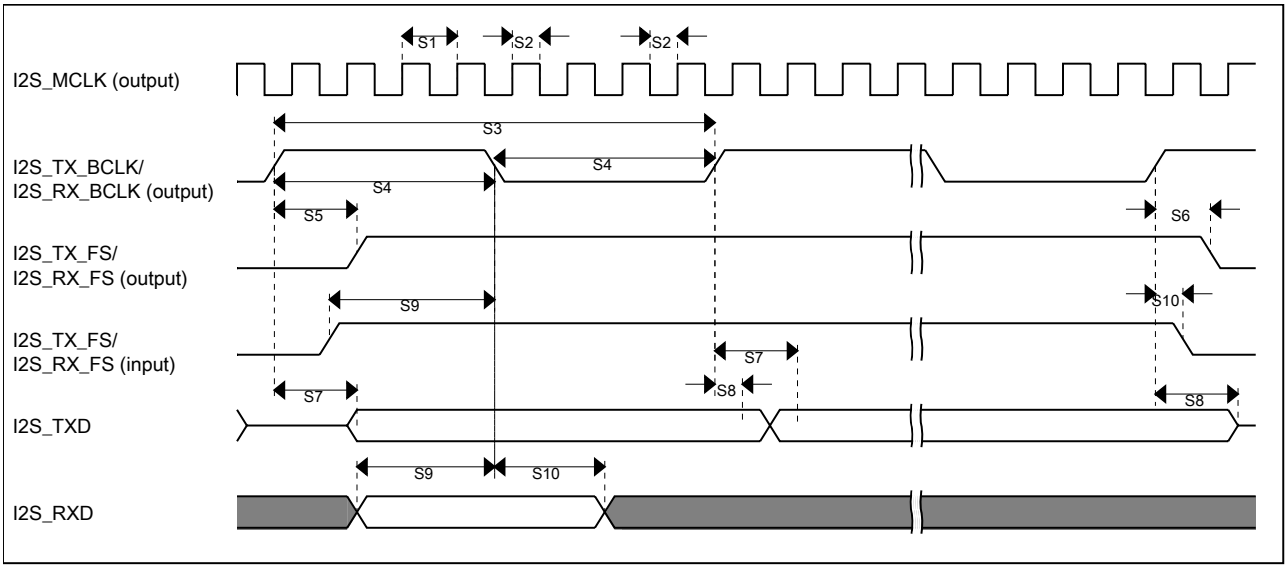

Figure 37. I2S/SAI timing — master modes

Table 78. I2S/SAI slave mode timing in Normal Run, Wait and Stop modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	80	—	ns
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	5.8	—	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	2	—	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid	—	28.5	ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	5.8	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK	2	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid[1]	—	26.3	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

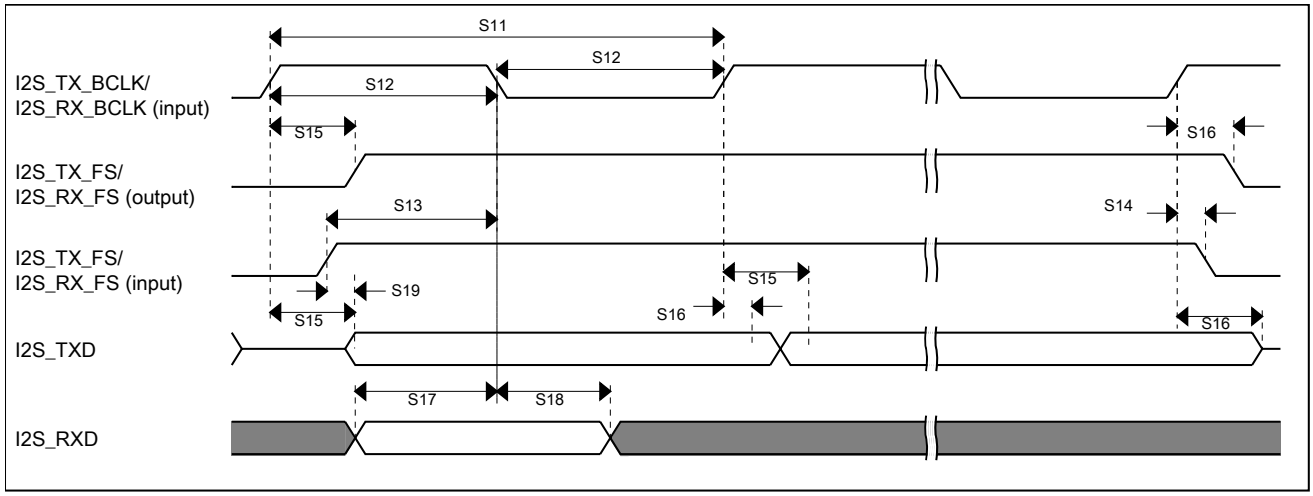

Figure 38. I2S/SAI timing — slave modes

5.4.8.6.3 VLPR, VLPW, and VLPS mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in VLPR, VLPW, and VLPS modes.

Table 79. I2S/SAI master mode timing in VLPR, VLPW, and VLPS modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	I2S_MCLK cycle time	62.5	—	ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	250	—	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid	—	45	ns
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid	-1	—	ns
S7	I2S_TX_BCLK to I2S_TXD valid	—	45	ns
S8	I2S_TX_BCLK to I2S_TXD invalid		—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK		—	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns