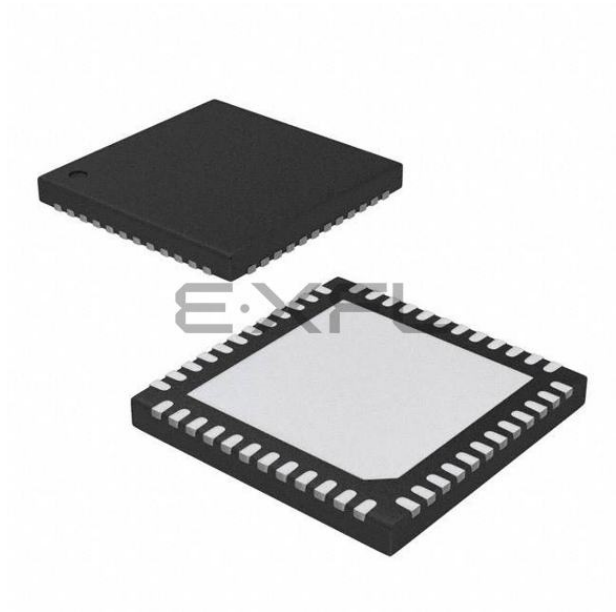

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	10MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	POR, PWM, Temp Sensor, WDT
Number of I/O	14
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 32
Voltage - Supply (Vcc/Vdd)	2.375V ~ 2.625V
Data Converters	A/D 5x24b, 8x24b; D/A 1x14b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad, CSP
Supplier Device Package	48-LFCSP-VQ (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/aduc7060bcpz32-rl

4/2009—Revision 0: Initial Version

Table 6. SPI Slave Mode Timing (Phase Mode = 0)

Parameter	Description	Min	Typ	Max	Unit
$t_{\overline{CS}}$	$\overline{CS}$ to SCLOCK edge[1]	$(2 \times t_{HCLK}) + (2 \times t_{UCLK})$			ns
t_{SL}	SCLOCK low pulse width	$2 \times t_{UCLK}$			ns
t_{SH}	SCLOCK high pulse width	$2 \times t_{UCLK}$			ns
t_{DAV}	Data output valid after SCLOCK edge			40	ns
t_{DSU}	Data input setup time before SCLOCK edge[1]	$1 \times t_{UCLK}$			ns
t_{DHD}	Data input hold time after SCLOCK edge[1]	$2 \times t_{UCLK}$			ns
t_{DF}	Data output fall time		30	40	ns
t_{DR}	Data output rise time		30	40	ns
t_{SR}	SCLOCK rise time	1			ns
t_{SF}	SCLOCK fall time	1			ns
t_{DOCS}	Data output valid after $\overline{CS}$ edge			10	ns
t_{SFS}	$\overline{CS}$ high after SCLOCK edge	0			ns

[1] t_{UCLK} = 97.6 ns. It corresponds to the 10.24 MHz internal clock from the PLL.

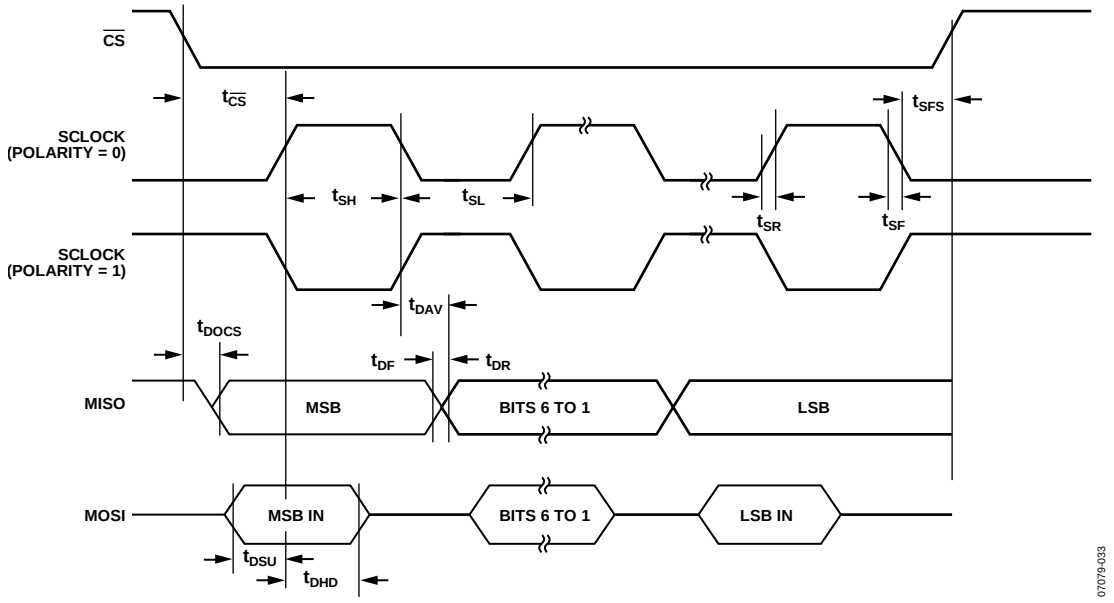

Figure 6. SPI Slave Mode Timing (Phase Mode = 0)

ABSOLUTE MAXIMUM RATINGS

T_A = −40°C to +125°C, unless otherwise noted.

Table 7.

Parameter	Rating
AGND to DGND to AVDD to DVDD	−0.3 V to +0.3 V
Digital I/O Voltage to DGND	−0.3 V to +3.6 V
VREF± to AGND	−0.3 V to AVDD + 0.3 V
ADC Inputs to AGND	−0.3 V to AVDD + 0.3 V
ESD (Human Body Model) Rating	
All Pins	±2 kV
Storage Temperature	125°C
Junction Temperature	
Transient	150°C
Continuous	130°C
Lead Temperature	
Soldering Reflow (15 sec)	260°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

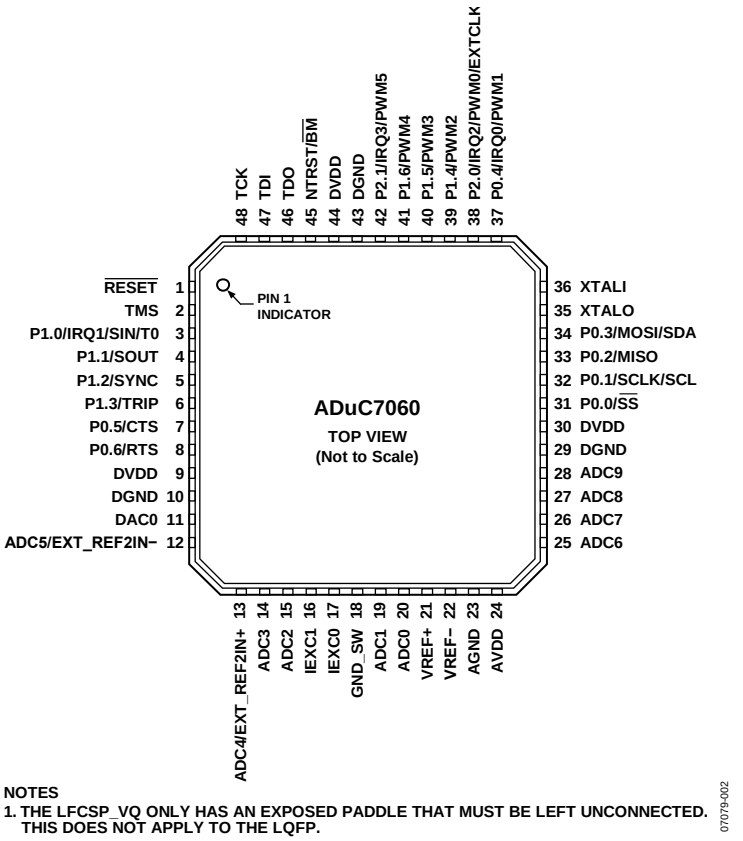

Figure 7. 48-Lead LQFP and 48-Lead LFCSP_VQ Pin Configuration

Table 8. ADuC7060 Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
0	EP		Exposed Paddle. The LFCSP_VQ only has an exposed paddle that must be left unconnected. This does not apply to the LQFP.
1	$\overline{\text{RESET}}$	I	Reset. Input pin, active low. An external 1 kΩ pull-up resistor is recommended with this pin.
2	TMS	I	JTAG Test Mode Select. Input pin used for debug and download. An external pull-up resistor (~100 kΩ) should be added to this pin.
3	P1.0/IRQ1/SIN/T0	I/O	General-Purpose Input and General Purpose Output P1.0/External Interrupt Request 1/Serial Input/Timer0 Input. This is a multifunction input/output pin offering four functions.
4	P1.1/SOUT	I/O	General-Purpose Input and General-Purpose Output P1.1/Serial Output. This is a dual function input/output pin.
5	P1.2/SYNC	I/O	General-Purpose Input and General-Purpose Output P1.2/PWM External Sync Input. This is a dual function input/output pin.
6	P1.3/TRIP	I/O	General-Purpose Input and General-Purpose Output P1.3/PWM External Trip Input. This is a dual function input/output pin.
7	P0.5/CTS	I/O	General-Purpose Input and General-Purpose Output P0.5/Clear-to-Send Signal in UART Mode.
8	P0.6/RTS	I/O	General-Purpose Input and General-Purpose Output P0.6/Request-to-Send Signal in UART Mode.
9	DVDD	S	Digital Supply Pin.
10	DGND	S	Digital Ground.
11	DAC0	O	DAC Output. Analog output pin.

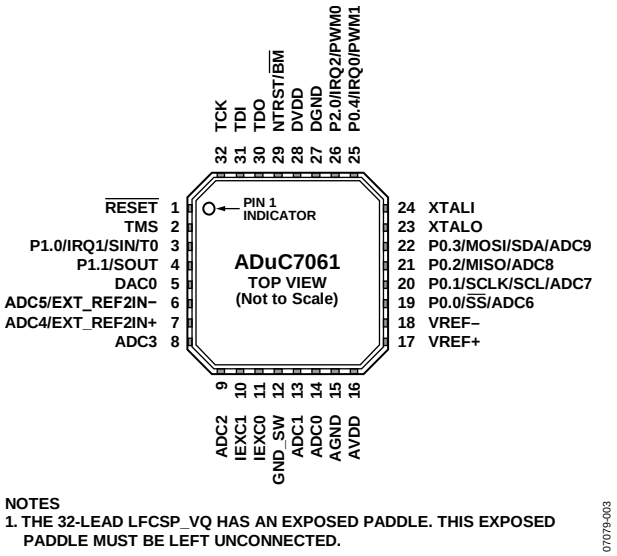

Figure 8. 32-Lead LFCSP Pin Configuration

Table 9. ADuC7061 Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
0	EP		Exposed Paddle. The 32-lead LFCSP_VQ has an exposed paddle that must be left unconnected.
1	$\overline{\text{RESET}}$	I	Reset Pin. Input pin, active low. An external 1 kΩ pull-up resistor is recommended with this pin.
2	TMS	I	JTAG Test Mode Select. Input pin used for debug and download. An external pull-up resistor (~100 kΩ) should be added to this pin.
3	P1.0/IRQ1/SIN/T0	I/O	General-Purpose Input and General-Purpose Output P1.0/External Interrupt Request 1/Serial Input/Timer0 Input. This is a multifunction input/output pin offering four functions.
4	P1.1/SOUT	I/O	General-Purpose Input and General-Purpose Output P1.1/Serial Output. This is a dual function input/output pin.
5	DAC0	O	DAC Output. Analog output pin.
6	ADC5/EXT_REF2IN–	I	Single-Ended or Differential Analog Input 5/External Reference Negative Input. This is a dual function analog input pin. The ADC5 serves as the analog input for the auxiliary ADC. The EXT_REF2IN– serves as the external reference negative input by ADC for the auxiliary channel.
7	ADC4/EXT_REF2IN+	I	Multifunction Analog Input Pin. This pin can be used for the single-ended or differential Analog Input 4, which is the analog input for the auxiliary ADC, or it can be used for the external reference positive input for the auxiliary channel.
8	ADC3	I	Single-Ended or Differential Analog Input 3. Analog input for primary and auxiliary ADCs.
9	ADC2	I	Single-Ended or Differential Analog Input 2. Analog input for primary and auxiliary ADCs.
10	IEXC1	O	Programmable Current Source. Analog output pin.
11	IEXC0	O	Programmable Current Source. Analog output pin.
12	GND_SW	I	Switch to Internal Analog Ground Reference. When this input pin is not used, connect it directly to the AGND system ground.
13	ADC1	I	Single-Ended or Differential Analog Input 1. Analog input for the primary ADC. Negative differential input for primary ADC.
14	ADC0	I	Single-Ended or Differential Analog Input 0. Analog input for the primary ADC. Positive differential input for primary ADC.
15	AGND	S	Analog Ground.
16	AVDD	S	Analog Supply Pin.
17	VREF+	I	External Reference Positive Input for the Primary Channel. Analog input pin.
18	VREF–	I	External Reference Negative Input for the Primary Channel. Analog input pin.
19	P0.0/$\overline{\text{SS}}$/ADC6	I/O	General-Purpose Input and General-Purpose Output P0.0/SPI Slave Select (Active Low)/Input to Auxiliary ADC6. This is a multifunction input/output pin. Single-ended or differential Analog Input 6. Analog input for the auxiliary ADC.
20	P0.1/SCLK/SCL/ADC7	I/O	General-Purpose Input and General-Purpose Output P0.1/SPI Clock/I^2C Clock/Input to Auxiliary ADC7. This is a multifunction input/output pin. Single-ended or differential Analog Input 7. Analog input for the auxiliary ADC.

Permanent Protection

Permanent protection can be set via FEEPRO, similar to how keyed permanent protection is set, with the only difference being that the software key used is 0xDEADDEAD. When the FEEPRO write sequence is saved, only a mass erase sets the software protection key back to 0xFFFFFFFF. This also erases the entire user code space.

Sequence to Write the Software Protection Key and Set Permanent Protection

1. Write in FEEPRO corresponding to the pages to be protected.
2. Write the new (user-defined) 32-bit software protection key in FEEADR (Bits[31:16]) and FEEDAT (Bits[15:0]).
3. Write 10 in FEEMOD (Bits[6:5]) and set FEEMOD (Bit 3).
4. Run the protect command (Code 0x0C) in FEECON.

To remove or modify the protection, the same sequence can be used with a modified value of FEEPRO.

The previous sequence for writing the key and setting permanent protection is illustrated in the following example, this protects writing Page 4 and Page 5 of the Flash/EE:

```
Int a = FEESTA;           // Ensure FEESTA
is cleared
FEEPRO = 0xFFFFFFFB;      // Protect Page 4
and Page 5
FEEADR = 0x66BB;          // 32-bit key
value (Bits[31:16])
FEEDAT = 0xAA55;          // 32-bit key
value (Bits[15:0])
FEEMOD = 0x0048           // Lock security
sequence
FEECON = 0x0C;            // Write key
command
while (FEESTA & 0x04){}   // Wait for
command to finish
```

Command Sequence for Executing a Mass Erase

```
FEEDAT = 0x3CFF;
FEEADR = 0xFFC3;
FEEMOD = FEEMOD|0x8;   //Erase key enable
FEECON = 0x06;         //Mass erase command
```

MEMORY MAPPED REGISTERS

The memory mapped register (MMR) space is mapped into the upper two pages of the memory array and is accessed by indirect addressing through the ARM7 banked registers.

The MMR space provides an interface between the CPU and all on-chip peripherals. All registers, except the core registers, reside in the MMR area. All shaded locations shown in Figure 12 are unoccupied or reserved locations and should not be accessed by user software. Figure 12 shows the full MMR memory map.

The access time for reading from or writing to an MMR depends on the advanced microcontroller bus architecture (AMBA) bus used to access the peripheral. The processor has two AMBA buses: the advanced high performance bus (AHB) used for system modules and the advanced peripheral bus (APB) used for a lower performance peripheral. Access to the AHB is one cycle, and access to the APB is two cycles. All peripherals on the ADuC7060/ADuC7061 are on the APB except for the Flash/EE memory, the GPIOs, and the PWM.

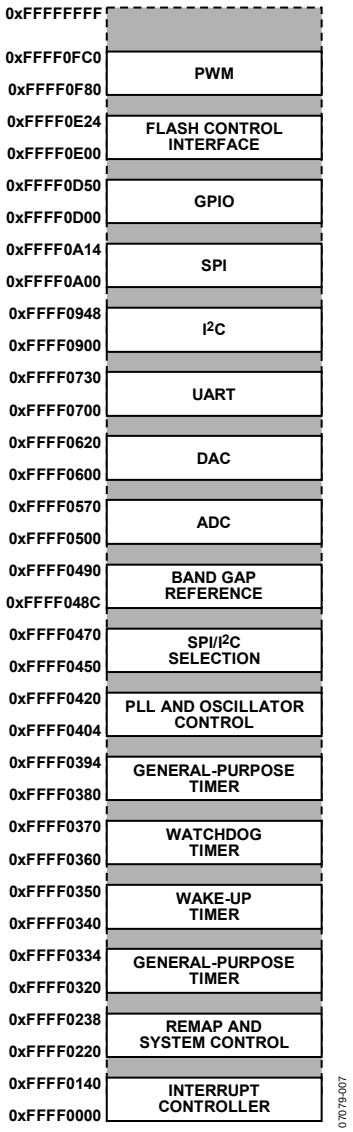

Figure 12. Memory Mapped Registers

Table 19. Timer Address Base = 0xFFFF0300

Address	Name	Bytes	Access Type	Default Value	Description
0x0320	T0LD	4	R/W	0x00000000	Timer0 load register.
0x0324	T0VAL	4	R	0xFFFFFFFF	Timer0 value register.
0x0328	T0CON	4	R/W	0x01000000	Timer0 control MMR.
0x032C	T0CLRI	1	W	N/A	Timer0 interrupt clear register.
0x0330	T0CAP	4	R	0x00000000	Timer0 capture register.
0x0340	T1LD	4	R/W	0x00000000	Timer1 load register.
0x0344	T1VAL	4	R	0xFFFFFFFF	Timer1 value register.
0x0348	T1CON	2	R/W	0x0000	Timer1 control MMR.
0x034C	T1CLRI	1	W	N/A	Timer1 interrupt clear register.
0x0360	T2LD	2	R/W	0x3BF8	Timer2 load register.
0x0364	T2VAL	2	R	0x3BF8	Timer2 value register.
0x0368	T2CON	2	R/W	0x0000	Timer2 control MMR.
0x036C	T2CLRI	1	W	N/A	Timer2 interrupt clear register.
0x0380	T3LD	2	R/W	0x0000	Timer3 load register.
0x0384	T3VAL	2	R	0xFFFF	Timer3 value register.
0x0388	T3CON	4	R/W	0x00000000	Timer3 control MMR.
0x038C	T3CLRI	1	W	N/A	Timer3 interrupt clear register.
0x0390	T3CAP	2	R	0x0000	Timer3 capture register.

Table 20. PLL Base Address = 0xFFFF0400

Address	Name	Bytes	Access Type	Default Value	Description
0x0404	POWKEY1	2	W	0xXXXX	POWCON0 prewrite key.
0x0408	POWCON0	1	R/W	0x7B	Power control and core speed control register.
0x040C	POWKEY2	2	W	0xXXXX	POWCON0 postwrite key.
0x0410	PLLKEY1	2	W	0xXXXX	PLLCON prewrite key.
0x0414	PLLCON	1	R/W	0x00	PLL clock source selection MMR.
0x0418	PLLKEY2	2	W	0xXXXX	PLLCON postwrite key.
0x0434	POWKEY3	2	W	0xXXXX	POWCON1 prewrite key.
0x0438	POWCON1	2	R/W	0x124	Power control register.
0x043C	POWKEY4	2	W	0xXXXX	POWCON1 postwrite key.
0x0464	GP0KEY1	2	W	0xXXXX	GP0CON1 prewrite key.
0x0468	GP0CON1	1	R/W	0x00	Configures P0.0, P0.1, P0.2, and P0.3 as analog inputs or digital I/Os. Also enables SPI or I^2C mode.
0x046C	GP0KEY2	2	W	0xXXXX	GP0CON1 postwrite key.

Table 21. ADC Address Base = 0xFFFF0500

Address	Name	Bytes	Access Type	Default Value	Description
0x0500	ADCSTA	2	R	0x0000	ADC status MMR.
0x0504	ADCMSKI	2	R/W	0x0000	ADC interrupt source enable MMR.
0x0508	ADCMDE	1	R/W	0x03	ADC mode register.
0x050C	ADC0CON	2	R/W	0x8000	Primary ADC control MMR.
0x0510	ADC1CON	2	R/W	0x0000	Auxiliary ADC control MMR.
0x0514	ADCFLT	2	R/W	0x0007	ADC filter control MMR.
0x0518	ADCCFG	1	R/W	0x00	ADC configuration MMR.
0x051C	ADC0DAT	4	R	0x00000000	Primary ADC result MMR.
0x0520	ADC1DAT	4	R	0x00000000	Auxiliary ADC result MMR
0x0524	ADC0OF[1]	2	R/W	0x0000, part specific, factory programmed	Primary ADC offset calibration setting.
0x0528	ADC1OF[1]	2	R/W	0x0000, part specific, factory programmed	Auxiliary ADC offset MMR.
0x052C	ADC0GN[1]	2	R/W	0x5555	Primary ADC offset MMR.
0x0530	ADC1GN[1]	2	R/W	0x5555	Auxiliary ADC offset MMR. See the ADC operation mode configuration bit (ADCLPMCFG[1:0]) in Table 42.
0x0534	ADC0RCR	2	R/W	0x0001	Primary ADC result counter/reload MMR.
0x0538	ADC0RCV	2	R	0x0000	Primary ADC result counter MMR.
0x053C	ADC0TH	2	R/W	0x0000	Primary ADC 16-bit comparator threshold MMR.
0x0540	ADC0THC	2	R/W	0x0001	Primary ADC 16-bit comparator threshold counter limit.
0x0544	ADC0THV	2	R	0x0000	ADC0 8-bit threshold exceeded counter register
0x0548	ADC0ACC	4	R	0x00000000	Primary ADC accumulator.
0x054C	ADC0ATH	4	R/W	0x00000000	Primary ADC 32-bit comparator threshold MMR.
0x0570	IEXCON	1	R/W	0x00	Excitation current sources control register.

[1] Updated by the kernel to part specific calibration value.

Table 22. DAC Control Address Base = 0xFFFF0600

Address	Name	Bytes	Access Type	Default Value	Description
0x0600	DAC0CON	2	R/W	0x0200	DAC control register.
0x0604	DAC0DAT	4	R/W	0x00000000	DAC output data register.

Table 23. UART Base Address = 0xFFFF0700

Address	Name	Bytes	Access Type	Default Value	Description
0x0700	COMTX	1	W	N/A	UART transmit register.
0x0700	COMRX	1	R	0x00	UART receive register.
0x0700	COMDIV0	1	R/W	0x00	UART Standard Baud Rate Generator Divisor Value 0.
0x0704	COMIEN0	1	R/W	0x00	UART Interrupt Enable MMR 0.
0x0704	COMDIV1	1	R/W	0x00	UART Standard Baud Rate Generator Divisor Value 1.
0x0708	COMIID0	1	R	0x01	UART Interrupt Identification 0.
0x070C	COMCON0	1	R/W	0x00	UART Control Register 0.
0x0710	COMCON1	1	R/W	0x00	UART Control Register 1.
0x0714	COMSTA0	1	R	0x60	UART Status Register 0.
0x0718	COMSTA1	1	R	0x00	UART Status Register 1.
0X072C	COMDIV2	2	R/W	0x0000	UART fractional divider MMR.

Table 27. Flash/EE Base Address = 0xFFFF0E00

Address	Name	Bytes	Access Type	Default Value	Description
0x0E00	FEESTA	2	R	0x20	Flash/EE status MMR.
0x0E04	FEEMOD	2	R/W	0x0000	Flash/EE control MMR.
0x0E08	FEECON	1	R/W	0x07	Flash/EE control MMR.
0x0E0C	FEEDAT	2	R/W	0xXXXX	Flash/EE data MMR.
0x0E10	FEEADR	2	R/W	0x0000	Flash/EE address MMR.
0x0E18	FEESIG	3	R	0xFFFFFF	Flash/EE LFSR MMR.
0x0E1C	FEEPRO	4	R/W	0x00000000	Flash/EE protection MMR.
0x0E20	FEEHID	4	R/W	0xFFFFFFFF	Flash/EE protection MMR.

Table 28. PWM Base Address = 0xFFFF0F80

Address	Name	Bytes	Access Type	Default Value	Description
0x0F80	PWMCON	2	R/W	0x0012	PWM control register. See the Pulse-Width Modulator section for full details.
0x0F84	PWM0COM0	2	R/W	0x0000	Compare Register 0 for PWM Output 0 and PWM Output 1.
0x0F88	PWM0COM1	2	R/W	0x0000	Compare Register 1 for PWM Output 0 and PWM Output 1.
0x0F8C	PWM0COM2	2	R/W	0x0000	Compare Register 2 for PWM Output 0 and PWM Output 1.
0x0F90	PWM0LEN	2	R/W	0x0000	Frequency control for PWM Output 0 and PWM Output 1.
0x0F94	PWM1COM0	2	R/W	0x0000	Compare Register 0 for PWM Output 2 and PWM Output 3.
0x0F98	PWM1COM1	2	R/W	0x0000	Compare Register 1 for PWM Output 2 and PWM Output 3.
0x0F9C	PWM1COM2	2	R/W	0x0000	Compare Register 2 for PWM Output 2 and PWM Output 3.
0x0FA0	PWM1LEN	2	R/W	0x0000	Frequency control for PWM Output 2 and PWM Output 3.
0x0FA4	PWM2COM0	2	R/W	0x0000	Compare Register 0 for PWM Output 4 and PWM Output 5.
0x0FA8	PWM2COM1	2	R/W	0x0000	Compare Register 1 for PWM Output 4 and PWM Output 5.
0x0FAC	PWM2COM2	2	R/W	0x0000	Compare Register 2 for PWM Output 4 and PWM Output 5.
0x0FB0	PWM2LEN	2	R/W	0x0000	Frequency control for PWM Output 4 and PWM Output 5.
0x0FB8	PWMCLRI	2	W	0x0000	PWM interrupt clear register. Writing any value to this register clears a PWM interrupt source.

Bit	Name	Description
4:3	ADCLPMCFG[1:0]	ADC power mode configuration. [00] = ADC normal mode. If enabled, the ADC operates with normal current consumption yielding optimum electrical performance. [01] = ADC low power mode. [10] = ADC normal mode, same as [00]. [11] = ADC low power plus mode (low power mode and PGA off).
2:0	ADCMD[2:0]	ADC operation mode configuration. [000] = ADC power-down mode. All ADC circuits and the input amplifier are powered down. [001] = ADC continuous conversion mode. In this mode, any enabled ADC continuously converts at a frequency equal to f_{ADC}. ADCxRDY must be cleared to enable new data to be written to ADC0DAT/ADC1DAT. [010] = ADC single conversion mode. In this mode, any enabled ADC performs a single conversion. The ADC enters idle mode when the single shot conversion is complete. A single conversion takes two to three ADC clock cycles, depending on the chop mode. [011] = ADC idle mode. In this mode, the ADC is fully powered on but is held in reset. The part enters this mode after calibration. [100] = ADC self-offset calibration. In this mode, an offset calibration is performed on any enabled ADC using an internally generated 0 V. The calibration is carried out at the user-programmed ADC settings; therefore, as with a normal single ADC conversion, it takes two to three ADC conversion cycles before a fully settled calibration result is ready. The calibration result is automatically written to the ADCxOF MMR of the respective ADC. The ADC returns to idle mode, and the calibration and conversion ready status bits are set at the end of an offset calibration cycle. Note: Always use ADC0 for single-ended self-calibration cycles on the primary ADC. Always use ADC0/ADC1 when self-calibrating for a differential input to the primary ADC. [101] = ADC self-gain calibration. In this mode, a gain calibration against an internal reference voltage is performed on all enabled ADCs. A gain calibration is a two-stage process and takes twice the time of an offset calibration. The calibration result is automatically written to the ADCxGN MMR of the respective ADC. The ADC returns to idle mode and the calibration and conversion ready status bits are set at the end of a gain calibration cycle. An ADC self-gain calibration should only be carried out on the primary channel ADC. Note that self-gain calibration works only when the gain = 1; do not use it when the gain > 1. [110] = ADC system zero-scale calibration. In this mode, a zero-scale calibration is performed on enabled ADC channels against an external zero-scale voltage driven at the ADC input pins. To do this, short the channel externally. [111] = ADC system full-scale calibration. In this mode, a full-scale calibration is performed on enabled ADC channels against an external full-scale voltage driven at the ADC input pins. The ADCxGN register is updated after a full-scale calibration sequence.

Primary ADC Control Register

Name: ADC0CON

Address: 0xFFFF050C

Default value: 0x8000

Access: Read and write

Function: The primary channel ADC control MMR is a 16-bit register. If the primary ADC is reconfigured via ADC0CON, the auxiliary ADC is also reset.

Bit	Name	Description
7	NOTCH2	Sinc3 modify. Set by user to modify the standard sinc3 frequency response to increase the filter stop-band rejection by approximately 5 dB. This is achieved by inserting a second notch (NOTCH2) at $f_{NOTCH2} = 1.333 \times f_{NOTCH}$ where f_{NOTCH} is the location of the first notch in the response.
6:0	SF[6:0]	Sinc3 decimation factor (SF).[1] The value (SF) written in these bits controls the oversampling (decimation factor) of the sinc3 filter. The output rate from the sinc3 filter is given by $f_{ADC} = (512{,}000/([SF + 1] \times 64))$ Hz[2] when the chop bit (Bit 15, chop enable) = 0 and the averaging factor (AF) = 0. This is valid for all SF values ≤ 125. For SF = 126, f_{ADC} is forced to 60 Hz. For SF = 127, f_{ADC} is forced to 50 Hz. For information on calculating the f_{ADC} for SF (other than 126 and 127) and AF values, refer to Table 46.

[1] Due to limitations on the digital filter internal data path, there are some limitations on the combinations of the sinc3 decimation factor (SF) and averaging factor (AF) that can be used to generate a required ADC output rate. This restriction limits the minimum ADC update in normal power mode to 4 Hz or 1 Hz in lower power mode.
[2] In low power mode, the ADC is driven directly by the low power oscillator (131 kHz) and not 512 kHz. All f_{ADC} calculations should be divided by 4 (approximately).

Table 46. ADC Conversion Rates and Settling Times

Chop Enabled	Averaging Factor	Running Average	f_{ADC} Normal Mode	f_{ADC} Low Power Mode	$t_{SETTLING}$[1]
No	No	No	$\frac{512{,}000}{[SF+1]\times 64}$	$\frac{131{,}072}{[SF+1]\times 64}$	$\frac{3}{f_{ADC}}$
No	No	Yes	$\frac{512{,}000}{[SF+1]\times 64}$	$\frac{131{,}072}{[SF+1]\times 64}$	$\frac{4}{f_{ADC}}$
No	Yes	No	$\frac{512{,}000}{[SF+1]\times 64\times[3+AF]}$	$\frac{131{,}072}{[SF+1]\times 64\times[3+AF]}$	$\frac{1}{f_{ADC}}$
No	Yes	Yes	$\frac{512{,}000}{[SF+1]\times 64\times[3+AF]}$	$\frac{131{,}072}{[SF+1]\times 64\times[3+AF]}$	$\frac{2}{f_{ADC}}$
Yes	N/A	N/A	$\frac{512{,}000}{[SF+1]\times 64\times[3+AF]+3}$	$\frac{131{,}072}{[SF+1]\times 64\times[3+AF]+3}$	$\frac{2}{f_{ADC}}$

[1] An additional time of approximately 60 µs per ADC is required before the first ADC is available.

Table 47. Allowable Combinations of SF and AF

	AF Range		
SF	**0**	**1 to 7**	**8 to 63**
0 to 31	Yes	Yes	Yes
32 to 63	Yes	Yes	No
64 to 127	Yes	No	No

Table 68. IRQVEC MMR Bit Designations

Bit	Access	Initial Value	Description
31:23	Read only	0	Always read as 0.
22:7	Read only	0	IRQBASE register value.
6:2	Read only	0	Highest priority IRQ source. This is a value between 0 to 19 representing the possible interrupt sources. For example, if the highest currently active IRQ is Timer1, then these bits are [01000].
1:0	Reserved	0	Reserved bits.

Priority Registers

The interrupt priority registers, IRQP0, IRQP1, and IRQP2, allow each interrupt source to have its priority level configured for a level between 0 and 7. Level 0 is the highest priority level.

IRQP0 Register

Name: IRQP0

Address: 0xFFFF0020

Default value: 0x00000000

Access: Read and write

Table 69. IRQP0 MMR Bit Designations

Bit	Name	Description
31:27	Reserved	Reserved bits.
26:24	T3PI	A priority level of 0 to 7 can be set for Timer3.
23	Reserved	Reserved bit.
22:20	T2PI	A priority level of 0 to 7 can be set for Timer2.
19	Reserved	Reserved bit.
18:16	T1PI	A priority level of 0 to 7 can be set for Timer1.
15	Reserved	Reserved bit.
14:12	T0PI	A priority level of 0 to 7 can be set for Timer0.
11:7	Reserved	Reserved bits.
6:4	SWINTP	A priority level of 0 to 7 can be set for the software interrupt source.
3:0	Reserved	Interrupt 0 cannot be prioritized.

IRQP1 Register

Name: IRQP1

Address: 0xFFFF0024

Default value: 0x00000000

Access: Read and write

Table 70. IRQP1 MMR Bit Designations

Bit	Name	Description
31	Reserved	Reserved bit.
30:28	I2CMPI	A priority level of 0 to 7 can be set for I^2C master.
27	Reserved	Reserved bit.
26:24	IRQ1PI	A priority level of 0 to 7 can be set for IRQ1.
23	Reserved	Reserved bit.
22:20	IRQ0PI	A priority level of 0 to 7 can be set for IRQ0.
19	Reserved	Reserved bit.
18:16	SPIMPI	A priority level of 0 to 7 can be set for SPI master.
15	Reserved	Reserved bit.
14:12	UARTPI	A priority level of 0 to 7 can be set for UART.
11	Reserved	Reserved bit.
10:8	ADCPI	A priority level of 0 to 7 can be set for the ADC interrupt source.
7:0	Reserved	Reserved bits.

IRQP2 Register

Name: IRQP2

Address: 0xFFFF0028

Default value: 0x00000000

Access: Read and write

Table 71. IRQP2 MMR Bit Designations

Bit	Name	Description
31:15	Reserved	Reserved bit.
14:12	IRQ3PI	A priority level of 0 to 7 can be set for IRQ3.
11	Reserved	Reserved bit.
10:8	IRQ2PI	A priority level of 0 to 7 can be set for IRQ2.
7	Reserved	Reserved bit.
6:4	SPISPI	A priority level of 0 to 7 can be set for SPI slave.
3	Reserved	Reserved bit.
2:0	I2CSPI	A priority level of 0 to 7 can be set for I^2C slave.

FIQSTAN

If IRQCONN[1] is asserted and FIQVEC is read, then one of these bits asserts. The bit that asserts depends on the priority of the FIQ. If the FIQ is of Priority 0, Bit 0 asserts; Priority 1, Bit 1 asserts; and so forth.

When a bit is set in this register, all interrupts of that priority and lower are blocked.

To clear a bit in this register, all bits of a higher priority must be cleared first. It is possible to clear only one bit as a time. For example, if this register is set to 0x09, writing 0xFF changes the register to 0x08, and writing 0xFF a second time changes the register to 0x00.

FIQSTAN Register

Name: FIQSTAN

Address: 0xFFFF013C

Default value: 0x00000000

Access: Read and write

Table 75. FIQSTAN MMR Bit Designations

Bit	Name	Description
31:8	Reserved	These bits are reserved and should not be written to.
7:0		Setting this bit to 1 enables nesting of FIQ interrupts. Clearing this bit means no nesting or prioritization of FIQs is allowed.

External Interrupts (IRQ0 to IRQ3)

The ADuC7060/ADuC7061 provides up to four external interrupt sources. These external interrupts can be individually configured as level triggered or rising/falling edge triggered.

To enable the external interrupt source, the appropriate bit must first be set in the FIQEN or IRQEN register. To select the required edge or level to trigger on, the IRQCONE register must be appropriately configured.

To properly clear an edge based external IRQ interrupt, set the appropriate bit in the IRQCLRE register.

IRQCONE Register

Name: IRQCONE

Address: 0xFFFF0034

Default value: 0x00000000

Access: Read and write

Table 76. IRQCONE MMR Bit Designations

Bit	Name	Description
31:8	Reserved	These bits are reserved and should not be written to.
7:6	IRQ3SRC[1:0]	[11] = External IRQ3 triggers on falling edge. [10] = External IRQ3 triggers on rising edge. [01] = External IRQ3 triggers on low level. [00] = External IRQ3 triggers on high level.
5:4	IRQ2SRC[1:0]	[11] = External IRQ2 triggers on falling edge. [10] = External IRQ2 triggers on rising edge. [01] = External IRQ2 triggers on low level. [00] = External IRQ2 triggers on high level.
3:2	IRQ1SRC[1:0]	[11] = External IRQ1 triggers on falling edge. [10] = External IRQ1 triggers on rising edge. [01] = External IRQ1 triggers on low level. [00] = External IRQ1 triggers on high level.
1:0	IRQ0SRC[1:0]	[11] = External IRQ0 triggers on falling edge. [10] = External IRQ0 triggers on rising edge. [01] = External IRQ0 triggers on low level. [00] = External IRQ0 triggers on high level.

UART Control Register 1

This 8-bit register controls the operation of the UART in conjunction with COMCON0.

COMCON1 Register

Name: COMCON1

Address: 0xFFFF0710

Default value: 0x00

Access: Read and write

Table 91. COMCON1 MMR Bit Designations

Bit	Name	Description
7:5		Reserved bits. Not used.
4	LOOPBACK	Loopback. Set by user to enable loopback mode. In loopback mode, the transmit pin is forced high.
3:2		Reserved bits. Not used.
1	RTS	Request to send. Set by user to force the RTS output to 0. Cleared by user to force the RTS output to 1.
0	DTR	Data terminal ready. Set by user to force the DTR output to 0. Cleared by user to force the DTR output to 1.

UART Status Register 0

COMSTA0 Register

Name: COMSTA0

Address: 0xFFFF0714

Default value: 0x60

Access: Read only

Function: This 8-bit read-only register reflects the current status on the UART.

Table 92. COMSTA0 MMR Bit Designations

Bit	Name	Description
7		Reserved.
6	TEMT	COMTX and shift register empty status bit. Set automatically if COMTX and the shift register are empty. This bit indicates that the data has been transmitted, that is, no more data is present in the shift register. Cleared automatically when writing to COMTX.
5	THRE	COMTX empty status bit. Set automatically if COMTX is empty. COMTX can be written as soon as this bit is set; the previous data might not have been transmitted yet and can still be present in the shift register. Cleared automatically when writing to COMTX.
4	BI	Break indicator. Set when P1.0/IRQ1/SIN/T0 pin is held low for more than the maximum word length. Cleared automatically.
3	FE	Framing error. Set when the stop bit is invalid. Cleared automatically.
2	PE	Parity error. Set when a parity error occurs. Cleared automatically.
1	OE	Overrun error. Set automatically if data is overwritten before being read. Cleared automatically.
0	DR	Data ready. Set automatically when COMRX is full. Cleared by reading COMRX.

UART Status Register 1

COMSTA1 Register

Name: COMSTA1

Address: 0xFFFF0718

Default value: 0x00

Access: Read only

Function: COMSTA1 is a modem status register.

Table 93. COMSTA1 MMR Bit Designations

Bit	Name	Description
7:5		Reserved. Not used.
4	CTS	Clear to send.
3:1		Reserved. Not used.
0	DCTS	Delta CTS. Set automatically if CTS changed state since COMSTA1 was last read. Cleared automatically by reading COMSTA1.

UART Interrupt Enable Register 0

COMIEN0 Register

Name: COMIEN0

Address: 0xFFFF0704

Default value: 0x00

Access: Read and write

Function: This 8-bit register enables and disables the individual UART interrupt sources.

Table 94. COMIEN0 MMR Bit Designations

Bit	Name	Description
7:4		Reserved. Not used.
3	EDSSI	Modem status interrupt enable bit. Set by user to enable generation of an interrupt if COMSTA1[4] or COMSTA1[0] are set. Cleared by user.
2	ELSI	Receive status interrupt enable bit. Set by user to enable generation of an interrupt if any of the COMSTA0[3:1] register bits are set. Cleared by user.
1	ETBEI	Enable transmit buffer empty interrupt. Set by user to enable an interrupt when the buffer is empty during a transmission; that is, when COMSTA0[5] is set. Cleared by user.
0	ERBFI	Enable receive buffer full interrupt. Set by user to enable an interrupt when the buffer is full during a reception. Cleared by user.

UART Interrupt Identification Register 0

COMIID0 Register

Name: COMIID0

Address: 0xFFFF0708

Default value: 0x01

Access: Read only

Function: This 8-bit register reflects the source of the UART interrupt.

SERIAL CLOCK GENERATION

The I²C master in the system generates the serial clock for a transfer. The master channel can be configured to operate in fast mode (400 kHz) or standard mode (100 kHz).

The bit rate is defined in the I2CDIV MMR as follows:

$$f_{SERIAL\ CLOCK} = \frac{f_{UCLK}}{(2 + DIVH) + (2 + DIVL)}$$

where:
f_{UCLK} is the clock before the clock divider.
DIVH is the high period of the clock.
DIVL is the low period of the clock.

Thus, for 100 kHz operation

DIVH = *DIVL* = 0x33

and for 400 kHz

DIVH = 0x0A, *DIVL* = 0x0F

The I2CDIV register corresponds to DIVH:DIVL.

I²C BUS ADDRESSES

Slave Mode

In slave mode, the I2CID0, I2CID1, I2CID2, and I2CID3 registers contain the device IDs. The device compares the four I2CIDx registers to the address byte received from the bus master. To be correctly addressed, the 7 MSBs of any ID register must be identical to the 7 MSBs of the first received address byte. The least significant bit of the ID registers (the transfer direction bit) is ignored in the process of address recognition.

The ADuC7060/ADuC7061 also supports 10-bit addressing mode. When Bit 1 of I2CSCON (ADR10EN bit) is set to 1, then one 10-bit address is supported in slave mode and is stored in the I2CID0 and I2CID1 registers. The 10-bit address is derived as follows:

I2CID0[0] is the read/write bit and is not part of the I²C address.

I2CID0[7:1] = Address Bits[6:0].

I2CID1[2:0] = Address Bits[9:7].

I2CID1[7:3] must be set to 11110b.

Master Mode

In master mode, the I2CADR0 register is programmed with the I²C address of the device.

In 7-bit address mode, I2CADR0[7:1] are set to the device address. I2CADR0[0] is the read/write bit.

In 10-bit address mode, the 10-bit address is created as follows:

I2CADR0[7:3] must be set to 11110b.

I2CADR0[2:1] = Address Bits[9:8].

I2CADR1[7:0] = Address Bits[7:0].

I2CADR0[0] is the read/write bit.

I²C REGISTERS

The I²C peripheral interface consists overall of 19 MMRs. Nine of these are master related only, nine are slave related only, and one MMR is common to both master and slave modes.

I²C Master Registers

I²C Master Control, I2CMCON Register

Name: I2CMCON

Address: 0xFFFF0900

Default value: 0x0000

Access: Read and write

Function: This 16-bit MMR configures the I²C peripheral in master mode.

I²C Master Status, I2CMSTA, Register

Name: I2CMSTA

Address: 0xFFFF0904

Default value: 0x0000

Access: Read only

Function: This 16-bit MMR is the I²C status register in master mode.

Table 98. I2CMSTA MMR Bit Designations

Bit	Name	Description
15:11		Reserved. These bits are reserved.
10	I2CBBUSY	I²C bus busy status bit. This bit is set to 1 when a start condition is detected on the I²C bus. This bit is cleared when a stop condition is detected on the bus.
9	I2CMRxFO	Master receive FIFO overflow. This bit is set to 1 when a byte is written to the receive FIFO when it is already full. This bit is cleared in all other conditions.
8	I2CMTC	I²C transmission complete status bit. This bit is set to 1 when a transmission is complete between the master and the slave with which it was communicating. If the I2CMCENI bit in I2CMCON is set, an interrupt is generated when this bit is set. Clear this interrupt source.
7	I2CMND	I²C master no acknowledge data bit This bit is set to 1 when a no acknowledge condition is received by the master in response to a data write transfer. If the I2CNACKENI bit in I2CMCON is set, an interrupt is generated when this bit is set. This bit is cleared in all other conditions.
6	I2CMBUSY	I²C master busy status bit. Set to 1 when the master is busy processing a transaction. Cleared if the master is ready or if another master device has control of the bus.
5	I2CAL	I²C arbitration lost status bit. This bit is set to 1 when the I²C master does not gain control of the I²C bus. If the I2CALENI bit in I2CMCON is set, an interrupt is generated when this bit is set. This bit is cleared in all other conditions.
4	I2CMNA	I²C master no acknowledge address bit. This bit is set to 1 when a no acknowledge condition is received by the master in response to an address. If the I2CNACKENI bit in I2CMCON is set, an interrupt is generated when this bit is set. This bit is cleared in all other conditions.
3	I2CMRXQ	I²C master receive request bit. This bit is set to 1 when data enters the receive FIFO. If the I2CMRENI in I2CMCON is set, an interrupt is generated. This bit is cleared in all other conditions.
2	I2CMTXQ	I²C master transmit request bit. This bit goes high if the transmit FIFO is empty or contains only one byte and the master has transmitted an address + write. If the I2CMTENI bit in I2CMCON is set, an interrupt is generated when this bit is set. This bit is cleared in all other conditions.
1:0	I2CMTFSTA	I²C master transmit FIFO status bits. [00] = I²C master transmit FIFO empty. [01] = 1 byte in master transmit FIFO. [10] = 1 byte in master transmit FIFO. [11] = I²C master transmit FIFO full.

Table 112. GPxCON MMR Bit Designations

Bit	Description
31:30	Reserved.
29:28	Reserved.
27:26	Reserved.
25:24	Selects the function of the P0.6/RTS and P1.6/PWM pins.
23:22	Reserved.
21:20	Selects the function of the P0.5/CTS and P1.5/PWM3 pins.
19:18	Reserved.
17:16	Selects the function of the P0.4/IRQ0/PWM1 and P1.4/PWM2 pins.
15:14	Reserved.
13:12	Selects the function of the P0.3/MOSI/SDA and P1.3/TRIP pins.
11:10	Reserved.
9:8	Selects the function of the P0.2/MISO and P1.2/SYNC pins.
7:6	Reserved.
5:4	Selects the function of the P0.1/SCLK/SCL, P1.1/SOUT, and P2.1/IRQ3/PWM5 pins.
3:2	Reserved.
1:0	Selects the function of the P0.0/$\overline{SS}$, P1.0/IRQ1/SIN/T0, P2.0/IRQ2/PWM0/EXTCLK pins.

GPxDAT REGISTERS

GPxDAT are Port x configuration and data registers. They configure the direction of the GPIO pins of Port x, set the output value for the pins that are configured as output, and store the input value of the pins that are configured as input.

Table 113. GPxDAT Registers

Name	Address	Default Value	Access
GP0DAT	0xFFFF0D20	0x000000XX	R/W
GP1DAT	0xFFFF0D30	0x000000XX	R/W
GP2DAT	0xFFFF0D40	0x000000XX	R/W

Table 114. GPxDAT MMR Bit Designations

Bit	Description
31:24	Direction of the data. Set to 1 by user to configure the GPIO pin as an output. Cleared to 0 by user to configure the GPIO pin as an input.
23:16	Port x data output.
15:8	Reflect the state of Port x pins at reset (read only).
7:0	Port x data input (read only).

GPxSET REGISTERS

GPxSET are data set Port x registers.

Table 115. GPxSET Registers

Name	Address	Default Value	Access
GP0SET	0xFFFF0D24	0x000000XX	W
GP1SET	0xFFFF0D34	0x000000XX	W
GP2SET	0xFFFF0D44	0x000000XX	W

Table 116. GPxSET MMR Bit Designations

Bit	Description
31:24	Reserved.
23:16	Data Port x set bit. Set to 1 by user to set bit on Port x; also sets the corresponding bit in the GPxDAT MMR. Cleared to 0 by user; does not affect the data output.
15:0	Reserved.

GPxCLR REGISTERS

GPxCLR are data clear Port x registers.

Table 117. GPxCLR Registers

Name	Address	Default Value	Access
GP0CLR	0xFFFF0D28	0x000000XX	W
GP1CLR	0xFFFF0D38	0x000000XX	W
GP2CLR	0xFFFF0D48	0x000000XX	W

Table 118. GPxCLR MMR Bit Designations

Bit	Description
31:24	Reserved.
23:16	Data Port x clear bit. Set to 1 by user to clear the bit on Port x; also clears the corresponding bit in the GPxDAT MMR. Cleared to 0 by user; does not affect the data output.
15:0	Reserved.

GPxPAR REGISTERS

The GPxPAR registers program the parameters for Port 0, Port 1, and Port 2. Note that the GPxDAT MMR must always be written after changing the GPxPAR MMR. Note that it is not possible to disable the internal pull-up resistor on P0.2.

Table 119. GPxPAR Registers

Name	Address	Default Value	Access
GP0PAR	0xFFFF0D2C	0x00000000	R/W
GP1PAR	0xFFFF0D3C	0x00000000	R/W
GP2PAR	0xFFFF0D4C	0x00000000	R/W

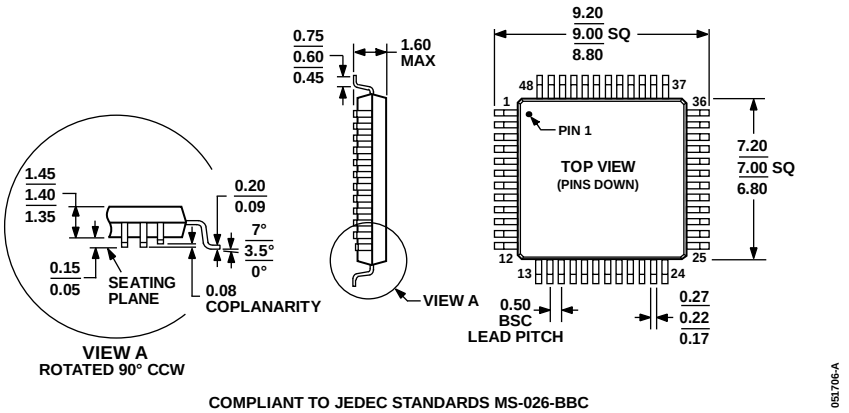

Figure 32. 48-Lead Low Profile Quad Flat Package [LQFP]
(ST-48)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Ordering Quantity
ADuC7060BCPZ32	−40°C to +125°C	48-Lead Lead Frame Chip Scale Package [LFCSP]	CP-48-5	
ADuC7060BCPZ32-RL	−40°C to +125°C	48-Lead Lead Frame Chip Scale Package [LFCSP]	CP-48-5	2,500
ADuC7060BSTZ32	−40°C to +125°C	48-Lead Low Profile Quad Flat Package [LQFP]	ST-48	
ADuC7060BSTZ32-RL	−40°C to +125°C	48-Lead Low Profile Quad Flat Package [LQFP]	ST-48	2,000
ADuC7061BCPZ32	−40°C to +125°C	32-Lead Lead Frame Chip Scale Package [LFCSP]	CP-32-11	
ADuC7061BCPZ32-RL	−40°C to +125°C	32-Lead Lead Frame Chip Scale Package [LFCSP]	CP-32-11	5,000
EVAL-ADuC7060QSPZ		ADuC7060 Quick Start Plus Development System		
EVAL-ADuC7061MKZ		ADuC7061 Quick Start Evaluation System		

[1] Z = RoHS Compliant Part.