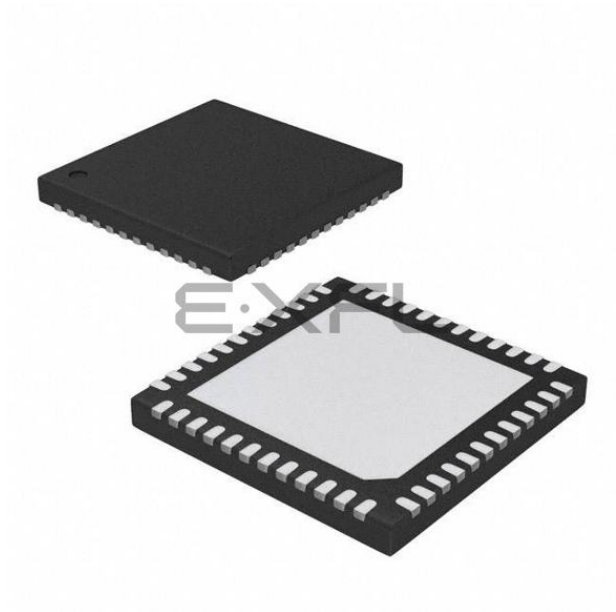

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	10MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	POR, PWM, Temp Sensor, WDT
Number of I/O	14
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 32
Voltage - Supply (Vcc/Vdd)	2.375V ~ 2.625V
Data Converters	A/D 5x24b, 8x24b; D/A 1x14b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad, CSP
Supplier Device Package	48-LFCSP-VQ (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/aduc7060bcpz32

SPI Timing

Table 3. SPI Master Mode Timing (Phase Mode = 1)

Parameter	Description	Min	Typ	Max	Unit
t_{SL}	SCLOCK low pulse width		(SPIDIV + 1) × t_{HCLK}		ns
t_{SH}	SCLOCK high pulse width		(SPIDIV + 1) × t_{HCLK}		ns
t_{DAV}	Data output valid after SCLOCK edge			25	ns
t_{DSU}	Data input setup time before SCLOCK edge[1]	1 × t_{UCLK}			ns
t_{DHD}	Data input hold time after SCLOCK edge[1]	2 × t_{UCLK}			ns
t_{DF}	Data output fall time		30	40	ns
t_{DR}	Data output rise time		30	40	ns
t_{SR}	SCLOCK rise time		30	40	ns
t_{SF}	SCLOCK fall time		30	40	ns

[1] t_{UCLK} = 97.6 ns. It corresponds to the 10.24 MHz internal clock from the PLL.

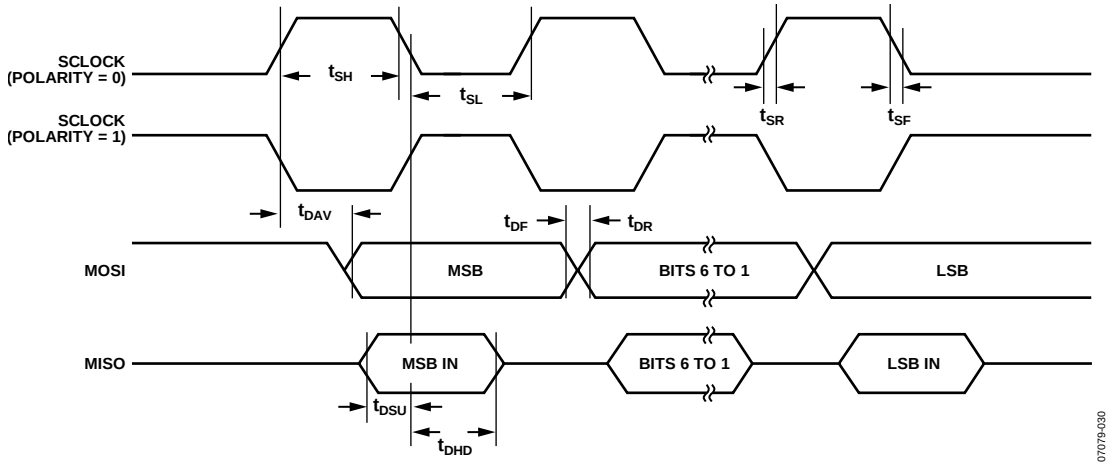

Figure 3. SPI Master Mode Timing (Phase Mode = 1)

Table 4. SPI Master Mode Timing (Phase Mode = 0)

Parameter	Description	Min	Typ	Max	Unit
t_{SL}	SCLOCK low pulse width		(SPIDIV + 1) × t_{HCLK}		ns
t_{SH}	SCLOCK high pulse width		(SPIDIV + 1) × t_{HCLK}		ns
t_{DAV}	Data output valid after SCLOCK edge			25	ns
t_{DOSU}	Data output setup before SCLOCK edge			90	ns
t_{DSU}	Data input setup time before SCLOCK edge[1]	1 × t_{UCLK}			ns
t_{DHD}	Data input hold time after SCLOCK edge[1]	2 × t_{UCLK}			ns
t_{DF}	Data output fall time		30	40	ns
t_{DR}	Data output rise time		30	40	ns
t_{SR}	SCLOCK rise time		30	40	ns
t_{SF}	SCLOCK fall time		30	40	ns

[1] t_{UCLK} = 97.6 ns. It corresponds to the 10.24 MHz internal clock from the PLL.

TERMINOLOGY

Conversion Rate
The conversion rate specifies the rate at which an output result is available from the ADC, when the ADC has settled.

The sigma-delta (Σ-Δ) conversion techniques used on this part mean that whereas the ADC front-end signal is oversampled at a relatively high sample rate, a subsequent digital filter is used to decimate the output, giving a valid 24-bit data conversion result at output rates from 1 Hz to 8 kHz.

Note that, when software switches from one input to another (on the same ADC), the digital filter must first be cleared and then allowed to average a new result. Depending on the configuration of the ADC and the type of filter, this can take multiple conversion cycles.

Integral Nonlinearity (INL)
INL is the maximum deviation of any code from a straight line passing through the endpoints of the transfer function. The endpoints of the transfer function are zero scale, a point ½ LSB below the first code transition, and full scale, a point ½ LSB above the last code transition (111 . . . 110 to 111 . . . 111). The error is expressed as a percentage of full scale.

No Missing Codes
No missing codes is a measure of the differential nonlinearity of the ADC. The error is expressed in bits and specifies the number of codes (ADC results) as 2N bits, where N is no missing codes guaranteed to occur through the full ADC input range.

Offset Error
Offset error is the deviation of the first code transition ADC input voltage from the ideal first code transition.

Offset Error Drift
Offset error drift is the variation in absolute offset error with respect to temperature. This error is expressed as least significant bits per degree Celsius.

Gain Error
Gain error is a measure of the span error of the ADC. It is a measure of the difference between the measured and the ideal span between any two points in the transfer function.

Output Noise
The output noise is specified as the standard deviation (or 1 × Sigma) of the distribution of the ADC output codes collected when the ADC input voltage is at a dc voltage. It is expressed as micro root mean square. The output, or root mean square (rms) noise, can be used to calculate the effective resolution of the ADC as defined by the following equation:

$$Effective\ Resolution = \log2(Full\text{-}Scale\ Range/rms\ Noise)\ \text{bits}$$

The peak-to-peak noise is defined as the deviation of codes that fall within 6.6 × Sigma of the distribution of ADC output codes collected when the ADC input voltage is at dc. The peak-to-peak noise is, therefore, calculated as

$$6.6 \times rms\ Noise$$

The peak-to-peak noise can be used to calculate the ADC (noise free code) resolution for which there is no code flicker within a 6.6-Sigma limit as defined by the following equation:

$$Noise\ Free\ Code\ Resolution = \log2\left(\frac{Full-Scale\ Range}{Peak-to-Peak\ Noise}\right)\ \text{bits}$$

Data Sheet Acronyms

ADC	analog-to-digital converter
ARM	advanced RISC machine
JTAG	joint test action group
LSB	least significant byte/bit
LVF	low voltage flag
MCU	microcontroller
MMR	memory mapped register
MSB	most significant byte/bit
PID	protected identifier
POR	power-on reset
PSM	power supply monitor
rms	root mean square

Permanent Protection

Permanent protection can be set via FEEPRO, similar to how keyed permanent protection is set, with the only difference being that the software key used is 0xDEADDEAD. When the FEEPRO write sequence is saved, only a mass erase sets the software protection key back to 0xFFFFFFFF. This also erases the entire user code space.

Sequence to Write the Software Protection Key and Set Permanent Protection

1. Write in FEEPRO corresponding to the pages to be protected.
2. Write the new (user-defined) 32-bit software protection key in FEEADR (Bits[31:16]) and FEEDAT (Bits[15:0]).
3. Write 10 in FEEMOD (Bits[6:5]) and set FEEMOD (Bit 3).
4. Run the protect command (Code 0x0C) in FEECON.

To remove or modify the protection, the same sequence can be used with a modified value of FEEPRO.

The previous sequence for writing the key and setting permanent protection is illustrated in the following example, this protects writing Page 4 and Page 5 of the Flash/EE:

```
Int a = FEESTA;           // Ensure FEESTA
is cleared
FEEPRO = 0xFFFFFFFB;      // Protect Page 4
and Page 5
FEEADR = 0x66BB;          // 32-bit key
value (Bits[31:16])
FEEDAT = 0xAA55;          // 32-bit key
value (Bits[15:0])
FEEMOD = 0x0048           // Lock security
sequence
FEECON = 0x0C;            // Write key
command
while (FEESTA & 0x04){}   // Wait for
command to finish
```

Command Sequence for Executing a Mass Erase

```
FEEDAT = 0x3CFF;
FEEADR = 0xFFC3;
FEEMOD = FEEMOD|0x8;   //Erase key enable
FEECON = 0x06;         //Mass erase command
```

Table 24. I²C Base Address = 0xFFFF0900

Address	Name	Bytes	Access Type	Default Value	Description
0x0900	I2CMCON	2	R/W	0x0000	I²C master control register.
0x0904	I2CMSTA	2	R	0x0000	I²C master status register.
0x0908	I2CMRX	1	R	0x00	I²C master receive register.
0x090C	I2CMTX	1	W	0x00	I²C master transmit register.
0x0910	I2CMCNT0	2	R/W	0x0000	I²C master read count register. Write the number of required bytes into this register prior to reading from a slave device.
0x0914	I2CMCNT1	1	R	0x00	I²C master current read count register. This register contains the number of bytes already received during a read from slave sequence.
0x0918	I2CADR0	1	R/W	0x00	Address byte register. Write the required slave address here prior to communications.
0x091C	I2CADR1	1	R/W	0x00	Address byte register. Write the required slave address here prior to communications. Only used in 10-bit mode.
0x0924	I2CDIV	2	R/W	0x1F1F	I²C clock control register. Used to configure the SCLK frequency.
0x0928	I2CSCON	2	R/W	0x0000	I²C slave control register.
0x092C	I2CSSTA	2	R/W	0x0000	I²C slave status register.
0x0930	I2CSRX	1	R	0x00	I²C slave receive register.
0x0934	I2CSTX	1	W	0x00	I²C slave transmit register.
0x0938	I2CALT	1	R/W	0x00	I²C hardware general call recognition register.
0x093C	I2CID0	1	R/W	0x00	I²C Slave ID0 register. Slave bus ID register.
0x0940	I2CID1	1	R/W	0x00	I²C Slave ID1 register. Slave bus ID register.
0x0944	I2CID2	1	R/W	0x00	I²C Slave ID2 register. Slave bus ID register.
0x0948	I2CID3	1	R/W	0x00	I²C Slave ID3 register. Slave bus ID register.
0x094C	I2CFSTA	2	R/W	0x0000	I²C FIFO status register. Used in both master and slave modes.

Table 25. SPI Base Address = 0xFFFF0A00

Address	Name	Bytes	Access Type	Default Value	Description
0x0A00	SPISTA	4	R	0x00000000	SPI status MMR.
0x0A04	SPIRX	1	R	0x00	SPI receive MMR.
0x0A08	SPITX	1	W	0x00	SPI transmit MMR.
0x0A0C	SPIDIV	1	W	0x1B	SPI baud rate select MMR.
0x0A10	SPICON	2	R/W	0x0000	SPI control MMR.

Table 26. GPIO Base Address = 0xFFFF0D00

Address	Name	Bytes	Access Type	Default Value	Description
0x0D00	GP0CON0	4	R/W	0x00000000	GPIO Port 0 control MMR.
0x0D04	GP1CON	4	R/W	0x00000000	GPIO Port 1 control MMR.
0x0D08	GP2CON	4	R/W	0x00000000	GPIO Port 2 control MMR.
0x0D20	GP0DAT	4	R/W	0x000000XX	GPIO Port 0 data control MMR.
0x0D24	GP0SET	4	W	0x000000XX	GPIO Port 0 data set MMR.
0x0D28	GP0CLR	4	W	0x000000XX	GPIO Port 0 data clear MMR.
0x0D2C	GP0PAR	4	R/W	0x00000000	GPIO Port 0 pull-up disable MMR.
0x0D30	GP1DAT	4	R/W	0x000000XX	GPIO Port 1 data control MMR.
0x0D34	GP1SET	4	W	0x000000XX	GPIO Port 1 data set MMR.
0x0D38	GP1CLR	4	W	0x000000XX	GPIO Port 1 data clear MMR.
0x0D3C	GP1PAR	4	R/W	0x00000000	GPIO Port 1 pull-up disable MMR.
0x0D40	GP2DAT	4	R/W	0x000000XX	GPIO Port 2 data control MMR.
0x0D44	GP2SET	4	W	0x000000XX	GPIO Port 2 data set MMR.
0x0D48	GP2CLR	4	W	0x000000XX	GPIO Port 2 data clear MMR.
0x0D4C	GP2PAR	4	R/W	0x00000000	GPIO Port 2 pull-up disable MMR.

Table 39. Example Scenarios for Using Diagnostic Current Sources

Diagnostic Test				
Register Setting	**Description**	**Normal Result**	**Fault Result**	**Detected Measurement for Fault**
ADC0DIAG[1:0] = 0	Convert ADC0/ADC1 as normal with diagnostic currents disabled.	Expected differential result across ADC0/ADC1.	Short circuit.	Primary ADC reading ≈ 0 V regardless of PGA setting.
ADC0DIAG[1:0] = 1	Enable a 50 µA diagnostic current source on ADC0 by setting ADC0DIAG[1:0] = 1. Convert ADC0 and ADC1.	Main ADC changes by ΔV = +50 µA × R1. For example, ~100 mV for R1 = 2 kΩ.	Short circuit between ADC0 and ADC1. Short circuit between R1_a and R1_b.	Primary ADC reading ≈ 0 V regardless of PGA setting.
	Convert ADC0 in single-ended mode with diagnostic currents disabled.	Expected voltage on ADC0.	ADC0 open circuit or R1 open circuit.	Primary ADC reading = +full scale, even on the lowest PGA setting.
ADC0DIAG[1:0] = 3	Enable a 50 µA diagnostic current source on both ADC0 and ADC1 by setting ADC0DIAG[1:0] = 3. Convert ADC0 and ADC1.	Primary ADC changes by ΔV = 50 µA × (R1 − R2), that is, ~10 mV for 10% tolerance.	R1 does not match R2.	Primary ADC reading > 10 mV.

SINC3 FILTER

The number entered into Bits[6:0] of the ADCFLT register sets the decimation factor of the sinc3 filter. See Table 46 and Table 47 for further details on the decimation factor values.

The range of operation of the sinc3 filter (SF) word depends on whether the chop function is enabled. With chopping disabled, the minimum SF word allowed is 0 and the maximum is 127, giving an ADC throughput range of 50 Hz to 8 kHz.

For details on how to calculate the ADC sampling frequency based on the value programmed to the SF[6:0] bits in the ADCFLT register, refer to Table 46. When changing conversions speeds, put ADC into idle mode before restarting.

ADC CHOPPING

The ADCs on the ADuC7060/ADuC7061 implements a chopping scheme whereby the ADC repeatedly reverses its inputs. Therefore, the decimated digital output values from the sinc3 filter have a positive and negative offset term associated with them. This results in the ADC including a final summing stage that sums and averages each value from the filter with previous filter output values. This new value is then sent to the ADC data MMR. This chopping scheme results in excellent dc offset and offset drift specifications and is extremely beneficial in applications where drift and noise rejection are required.

PROGRAMMABLE GAIN AMPLIFIER

The primary ADC incorporates an on-chip programmable gain amplifier (PGA). The PGA can be programmed through 10 different settings giving a range of 1 to 512. The gain is controlled by the ADC0PGA[3:0] bits in the ADC0CON MMR.

EXCITATION SOURCES

The ADuC7060/ADuC7061 contains two matched software configurable current sources. These excitation currents are sourced from AVDD. They are individually configurable to give a current range of 200 µA to 1 mA. The current step sizes are 200 µA. These current sources can be used to excite an external resistive bridge or RTD sensors. The IEXCON MMR controls the excitation current sources. Bit 6 of IEXCON must be set to enable Excitation Current Source 0. Similarly, Bit 7 must be set to enable Excitation Current Source 1. The output current of each current source is controlled by the IOUT[3:0] bits of this register.

It is also possible to configure the excitation current sources to output current to a single output pin, either IEXC0 or IEXC1, by using the IEXC0_DIR and IEXC1_DIR bits of IEXCON. This allows up to 2 mA to output current on a single excitation pin.

ADC LOW POWER MODE

The ADuC7060/ADuC7061 allows the primary and auxiliary ADCs to be placed in low power operating mode. When configured for this mode, the ADC throughput time is reduced, but the power consumption of the primary ADC is reduced by a factor of about 4; the auxiliary ADC power consumption is reduced by a factor of roughly 3. The maximum ADC conversion rate in low power mode is 2 kHz. The operating mode of the ADCs is controlled by the ADCMDE register. This register configures the part for either normal mode (default), low power mode, or low power plus mode. Low power plus mode is the same as low power mode except that the PGA is disabled. To place the ADCs into low power mode, the following steps must be completed:

- ADCMDE[4:3]—Setting these bits enables normal mode, low power mode, or low power plus mode.
- ADCMDE[5]—Setting this bit configures the part for low power mode.
- ADCMDE[7]—Clearing this bit further reduces power consumption by reducing the frequency of the ADC clock.

ADC COMPARATOR AND ACCUMULATOR

Every primary ADC result can be compared to a preset threshold level (ADC0TH) as configured via ADCCFG[4:3]. An MCU interrupt is generated if the absolute (sign independent) value of the ADC result is greater than the preprogrammed comparator threshold level. An extended function of this comparator function allows user code to configure a threshold counter (ADC0THV) to monitor the number of primary ADC results that have occurred above or below the preset threshold level. Again, an ADC interrupt is generated when the threshold counter reaches a preset value (ADC0RCR).

Finally, a 32-bit accumulator (ADC0ACC) function can be configured (ADCCFG[6:5]) allowing the primary ADC to add (or subtract) multiple primary ADC sample results. User code can read the accumulated value directly (ADC0ACC) without any further software processing.

TEMPERATURE SENSOR

The ADuC7060/ADuC7061 provides a voltage output from an on-chip band gap reference proportional to absolute temperature. This voltage output can also be routed through the front-end auxiliary ADC multiplexer (effectively, an additional ADC channel input), facilitating an internal temperature sensor channel that measures die temperature.

The internal temperature sensor is not designed for use as an absolute ambient temperature calculator. It is intended for use as an approximate indicator of the temperature of the ADuC7060/ADuC7061 die.

The typical temperature coefficient is 0.28 mV/°C.

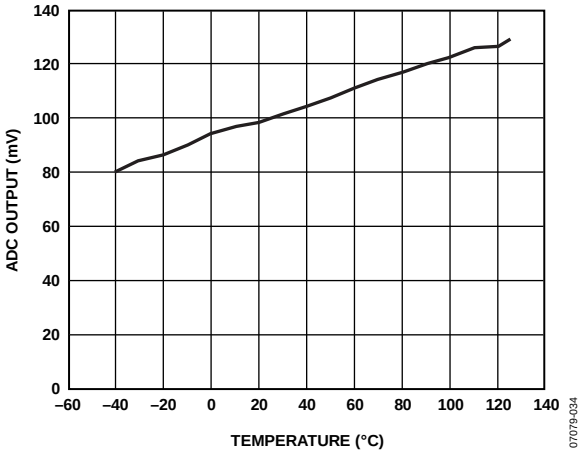

Figure 16. ADC Output vs. Temperature

ADC MMR INTERFACE

The ADCs are controlled and configured through a number of MMRs that are described in detail in the following sections.

In response to an ADC interrupt, user code should interrogate the ADCSTA MMR to determine the source of the interrupt. Each ADC interrupt source can be individually masked via the ADCMSKI MMR described in Table 41.

All primary ADC result ready bits are cleared by a read of the ADC0DAT MMR. If the primary channel ADC is not enabled, all ADC result ready bits are cleared by a read of the ADC1DAT MMR. To ensure that primary ADC and auxiliary ADC conversion data are synchronous, user code should first read the ADC1DAT MMR and then the ADC0DAT MMR. New ADC conversion results are not written to the ADCxDAT MMRs unless the respective ADC result ready bits are first cleared. The only exception to this rule is the data conversion result updates when the ARM core is powered down. In this mode, ADCxDAT registers always contain the most recent ADC conversion result even though the ready bits are not cleared.

ADC Status Register

Name: ADCSTA

Address: 0xFFFF0500

Default value: 0x0000

Access: Read only

Function: This read-only register holds general status information related to the mode of operation or current status of the ADuC7060/ADuC7061 ADCs.

Table 43. ADC0CON MMR Bit Designations

Bit	Name	Description
15	ADC0EN	Primary channel ADC enable. This bit is set to 1 by user code to enable the primary ADC. Clearing this bit to 0 powers down the primary ADC and resets the respective ADC ready bit in the ADCSTA MMR to 0.
14:13	ADC0DIAG[1:0]	Diagnostic current source enable bits. [00] = current sources off. [01] = enables a 50 µA current source on the selected positive input (for example, ADC0). [10] = enables a 50 µA current source on the selected negative input (for example, ADC1). [11] = enables a 50 µA current source on both selected inputs (for example, ADC0 and ADC1).
12	HIGHEXTREF0	This bit must be set high if the external reference for ADC0 exceeds 1.35 V. This results in the reference source being divided by 2. Clear this bit when using the internal reference or an external reference of less than 1.35 V.
11	AMP_CM	This bit is set to 1 by user to set the PGA output common-mode voltage to AVDD/2. This bit is cleared to 0 by user code to set the PGA output common-mode voltage to the PGA input common-mode voltage level.
10	ADC0CODE	Primary channel ADC output coding. This bit is set to 1 by user code to configure primary ADC output coding as unipolar. This bit is cleared to 0 by user code to configure primary ADC output coding as twos complement.
9:6	ADC0CH[3:0]	Primary channel ADC input select. Note that single-ended channels are selected with respect to ADC5. Bias ADC5 to a minimum level of 0.1 V. [0000] = ADC0/ADC1 (differential mode). [0001] = ADC0/ADC5 (single-ended mode). [0010] = ADC1/ADC5 (single-ended mode). [0011] = VREF+, VREF−. Note: This is the reference selected by the ADC0REF bits. [0100] = Not used. This bit combination is reserved for future functionality and should not be written. [0101] = ADC2/ADC3 (differential mode). [0110] = ADC2/ADC5 (single-ended mode). [0111] = ADC3/ADC5 (single-ended mode). [1000] = internal short to ADC1. [1001] = internal short to ADC1.
5:4	ADC0REF[1:0]	Primary channel ADC reference select. [00] = internal reference selected. In ADC low power mode, the voltage reference selection is controlled by ADCMDE[5]. [01] = external reference inputs (VREF+, VREF−) selected. Set the HIGHEXTREF0 bit if the reference voltage exceeds 1.3 V. [10] = auxiliary external reference inputs (ADC4/EXT_REF2IN+, ADC5/EXT_REF2IN−) selected. Set the HIGHEXTREF0 bit if the reference voltage exceeds 1.3 V. [11] = (AVDD, AGND) divide-by-two selected.
3:0	ADC0PGA[3:0].	Primary channel ADC gain select. Note, nominal primary ADC full-scale input voltage = (VREF/gain). [0000] = ADC0 gain of 1. Buffer of negative input is bypassed. [0001] = ADC0 gain of 2. [0010] = ADC0 gain of 4 (default value). Enables the in-amp. [0011] = ADC0 gain of 8. [0100] = ADC0 gain of 16. [0101] = ADC0 gain of 32. [0110] = ADC0 gain of 64 (maximum PGA gain setting). [0111] = ADC0 gain of 128 (extra gain implemented digitally). [1000] = ADC0 gain of 256. [1001] = ADC0 gain of 512. [1XXX] = ADC0 gain is undefined.

Primary Channel ADC Threshold Register

Name: ADC0TH

Address: 0xFFFF053C

Default value: 0x0000

Access: Read and write

Function: This 16-bit MMR sets the threshold against which the absolute value of the primary ADC conversion result is compared. In unipolar mode, ADC0TH[15:0] are compared, and in twos complement mode, ADC0TH[14:0] are compared.

Table 57. ADC0TH MMR Bit Designations

Bit	Description
15:0	ADC0 16-bit comparator threshold register.

Primary Channel ADC Threshold Counter Limit Register

Name: ADC0THC

Address: 0xFFFF0540

Default value: 0x0001

Access: Read and write

Function: This 8-bit MMR determines how many cumulative (values below the threshold decrement or reset the count to 0) primary ADC conversion result readings above ADC0TH must occur before the primary ADC comparator threshold bit is set in the ADCSTA MMR, generating an ADC interrupt. The primary ADC comparator threshold bit is asserted as soon as ADC0THV = ADC0RCR.

Table 58. ADC0THC MMR Bit Designations

Bit	Description
15:8	Reserved.
7:0	ADC0 8-bit threshold counter limit register.

Primary Channel ADC Threshold Counter Register

Name: ADC0THV

Address: 0xFFFF0544

Default value: 0x0000

Access: Read only

Function: This 8-bit MMR is incremented every time the absolute value of a primary ADC conversion result |Result| ≥ ADC0TH. This register is decremented or reset to 0 every time the absolute value of a primary ADC conversion result |Result| < ADC0TH. The configuration of this function is enabled via the primary channel ADC comparator bits in the ADCCFG MMR.

Table 59. ADC0THV MMR Bit Designations

Bit	Description
7:0	ADC0 8-bit threshold exceeded counter register.

Primary Channel ADC Accumulator Register

Name: ADC0ACC

Address: 0xFFFF0548

Default value: 0x00000000

Access: Read only

Function: This 32-bit MMR holds the primary ADC accumulator value. The primary ADC ready bit in the ADCSTA MMR should be used to determine when it is safe to read this MMR. The MMR value is reset to 0 by disabling the accumulator in the ADCCFG MMR or by reconfiguring the primary channel ADC.

Table 60. ADC0ACC MMR Bit Designations

Bit	Description
31:0	ADC0 32-bit accumulator register.

DAC0DAT Register

Name: DAC0DAT

Address: 0xFFFF0604

Default value: 0x00000000

Access: Read and write

Function: This 32-bit MMR contains the DAC output value.

Table 64. DAC0DAT MMR Bit Designations

Bit	Description
31:28	Reserved.
27:16	12-bit data for DAC0.
15:12	Extra four bits used in interpolation mode.
11:0	Reserved.

USING THE DAC

The on-chip DAC architecture consists of a resistor string DAC followed by an output buffer amplifier.

The reference source for the DAC is user selectable in software. It can be AVDD, VREF±, or ADCx/EXT_REF2IN±.

- In 0-to-AVDD mode, the DAC output transfer function spans from 0 V to the voltage at the AVDD pin.
- In VREF± and ADCx/EXT_REF2IN± modes, the DAC output transfer function spans from negative input voltage to the voltage positive input pin. Note that these voltages must never go below 0 V or above AVDD.
- In 0-to-V_{REF} mode, the DAC output transfer function spans from 0 V to the internal 1.2 V reference, V_{REF}.

The DAC can be configured in three different user modes: normal mode, DAC interpolation mode, and op amp mode.

Normal DAC Mode

In this mode of operation, the DAC is configured as a 12-bit voltage output DAC. By default, the DAC buffer is enabled, but the output buffer can be disabled. If the DAC output buffer is disabled, the DAC is capable of driving a capacitive load of only 20 pF. The DAC buffer is disabled by setting the DACBUFBYPASS bit in DAC0CON.

The DAC output buffer amplifier features a true, rail-to-rail output stage implementation. This means that when unloaded, each output is capable of swinging to within less than 5 mV of both AVDD and ground. Moreover, the linearity specification of the DAC (when driving a 5 kΩ resistive load to ground) is guaranteed through the full transfer function except for Code 0 to Code 100 and, in 0-to- AVDD mode only, Code 3995 to Code 4095. Linearity degradation near ground and AVDD is caused by saturation of the output amplifier, and a general representation of its effects (neglecting offset and gain error) is illustrated in Figure 21. The dotted line in Figure 21 indicates the ideal transfer function, and the solid line represents what the transfer function may look like with endpoint nonlinearities due to saturation of the output amplifier. Note that Figure 21 represents a transfer function in 0-to-AVDD mode only. In 0-to-V_{REF} or, VREF±, and ADCx/EXT_REF2IN± modes (with V_{REF} < AVDD or ADCx/EXT_REF2IN± < AVDD), the lower nonlinearity is similar. However, the upper portion of the transfer function follows the ideal line all the way to the end (V_{REF} in this case, not AVDD), showing no signs of endpoint linearity errors.

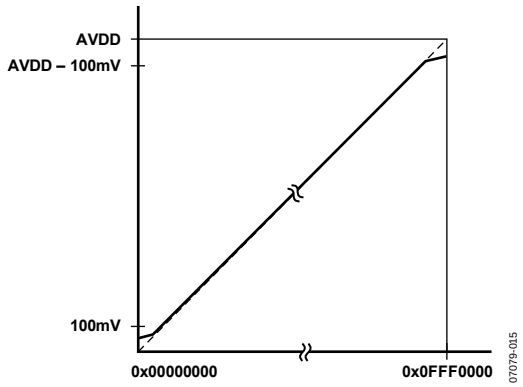

Figure 21. Endpoint Nonlinearities Due to Amplifier Saturation

The endpoint nonlinearities conceptually illustrated in Figure 21 worsen as a function of output loading. Most of the ADuC7060/ADuC7061 data sheet specifications in normal mode assume a 5 kΩ resistive load to ground at the DAC output. As the output is forced to source or sink more current, the nonlinear regions at the top or bottom (respectively) of Figure 21 become larger. With larger current demands, this can significantly limit output voltage swing.

DAC Interpolation Mode

In interpolation mode, a higher DAC output resolution of 16 bits is achieved with a longer update rate than normal mode. The update rate is controlled by the interpolation clock rate selected in the DAC0CON register. In this mode, an external RC filter is required to create a constant voltage.

Op Amp Mode

In op amp mode, the DAC output buffer is used as an op amp with the DAC itself disabled.

ADC6 is the positive input to the op amp, ADC7 is the negative input, and ADC8 is the output. In this mode, the DAC should be powered down by setting Bit 9 of DAC0CON.

NONVOLATILE FLASH/EE MEMORY

The ADuC7060/ADuC7061 incorporates Flash/EE memory technology on chip to provide the user with nonvolatile, in-circuit reprogrammable memory space.

Like EEPROM, flash memory can be programmed in-system at a byte level, although it must first be erased. The erase is performed in page blocks. As a result, flash memory is often and, more correctly, referred to as Flash/EE memory.

Overall, Flash/EE memory represents a step closer to the ideal memory device that includes nonvolatility, in-circuit programmability, high density, and low cost. Incorporated in the ADuC7060/ADuC7061, Flash/EE memory technology allows the user to update program code space in-circuit, without the need to replace one time programmable (OTP) devices at remote operating nodes.

The ADuC7060/ADuC7061 contains a 32 kB array of Flash/EE memory. The lower 30 kB are available to the user and the upper 2 kB contain permanently embedded firmware, allowing in-circuit serial download. These 2 kB of embedded firmware also contain a power-on configuration routine that downloads factory-calibrated coefficients to the various calibrated peripherals (such as ADC, temperature sensor, and band gap references). This 2 kB embedded firmware is hidden from user code.

FLASH/EE MEMORY RELIABILITY

The Flash/EE memory arrays on the parts are fully qualified for two key Flash/EE memory characteristics: Flash/EE memory cycling endurance and Flash/EE memory data retention.

Endurance quantifies the ability of the Flash/EE memory to be cycled through many program, read, and erase cycles. A single endurance cycle is composed of four independent, sequential events, defined as

- Initial page erase sequence
- Read/verify sequence for a single Flash/EE
- Byte program sequence memory
- Second read/verify sequence endurance cycle

In reliability qualification, every half word (16-bit wide) location of the three pages (top, middle, and bottom) in the Flash/EE memory is cycled 10,000 times from 0x0000 to 0xFFFF. The Flash/EE memory endurance qualification is carried out in accordance with JEDEC *Retention Lifetime Specification A117* over the industrial temperature range of −40°C to +125°C. The results allow the specification of a minimum endurance figure over a supply temperature of 10,000 cycles.

Retention quantifies the ability of the Flash/EE memory to retain its programmed data over time. Again, the parts are qualified in accordance with the formal *JEDEC Retention Lifetime Specification A117* at a specific junction temperature (T_J = 85°C). As part of this qualification procedure, the Flash/EE memory is cycled to its specified endurance limit, described previously, before data retention is characterized. This means that the Flash/EE memory is guaranteed to retain its data for its fully specified retention lifetime every time that the Flash/EE memory is reprogrammed. Also note that retention lifetime, based on activation energy of 0.6 eV, derates with T_J, as shown in Figure 22.

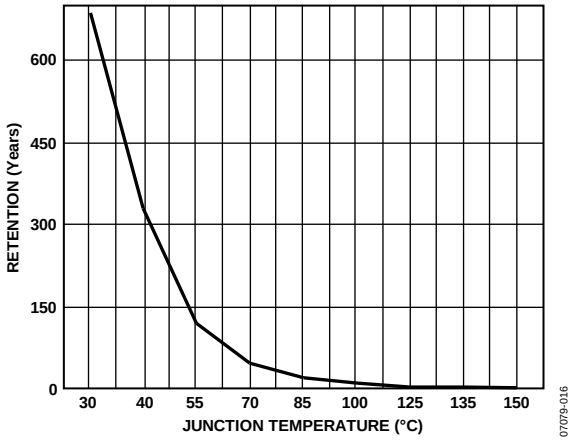

Figure 22. Flash/EE Memory Data Retention

PROGRAMMING

The 30 kB of Flash/EE memory can be programmed in-circuit, using the serial download mode or the provided JTAG mode.

Serial Downloading (In-Circuit Programming)

The ADuC7060/ADuC7061 facilitates code download via the standard UART serial port. The parts enter serial download mode after a reset or power cycle if the NTRST/$\overline{\text{BM}}$ pin is pulled low through an external 1 kΩ resistor. When in serial download mode, the user can download code to the full 30 kB of Flash/EE memory while the device is in-circuit in its target application hardware. An executable PC serial download is provided as part of the development system for serial downloading via the UART.

When the ADuC7060/ADuC7061 enters download mode, the user should be aware that the internal watchdog is enabled with a time-out period of 2 minutes. If the flash erase/write sequence is not completed in this period, a reset occurs.

JTAG Access

The JTAG protocol uses the on-chip JTAG interface to facilitate code download and debug.

IRQCONN

The IRQCONN register is the IRQ and FIQ control register. It contains two active bits: the first to enable nesting and prioritization of IRQ interrupts, and the other to enable nesting and prioritization of FIQ interrupts.

If these bits are cleared, FIQs and IRQs can still be used, but it is not possible to nest IRQs or FIQs. Neither is it possible to set an interrupt source priority level. In this default state, an FIQ does have a higher priority than an IRQ.

IRQCONN Register

Name: IRQCONN

Address: 0xFFFF0030

Default value: 0x00000000

Access: Read and write

Table 72. IRQCONN MMR Bit Designations

Bit	Name	Description
31:2	Reserved	These bits are reserved and should not be written to.
1	ENFIQN	Setting this bit to 1 enables nesting of FIQ interrupts. Clearing this bit means no nesting or prioritization of FIQs is allowed.
0	ENIRQN	Setting this bit to 1 enables nesting of IRQ interrupts. Clearing this bit means no nesting or prioritization of IRQs is allowed.

IRQSTAN

If IRQCONN[0] is asserted and IRQVEC is read, then one of these bits is asserted. The bit that asserts depends on the priority of the IRQ. If the IRQ is of Priority 0, then Bit 0 asserts; Priority 1, then Bit 1 asserts; and so forth. When a bit is set in this register, all interrupts of that priority and lower are blocked.

To clear a bit in this register, all bits of a higher priority must be cleared first. It is possible to clear only one bit at a time. For example, if this register is set to 0x09, writing 0xFF changes the register to 0x08, and writing 0xFF a second time changes the register to 0x00.

IRQSTAN Register

Name: IRQSTAN

Address: 0xFFFF003C

Default value: 0x00000000

Access: Read and write

Table 73. IRQSTAN MMR Bit Designations

Bit	Name	Description
31:8	Reserved	These bits are reserved and should not be written to.
7:0		Setting this bit to 1 enables nesting of FIQ interrupts. Clearing this bit means no nesting or prioritization of FIQs is allowed.

FIQVEC

The FIQ interrupt vector register, FIQVEC, points to a memory address containing a pointer to the interrupt service routine of the currently active FIQ. This register should be read only when an FIQ occurs and FIQ interrupt nesting has been enabled by setting Bit 1 of the IRQCONN register.

FIQVEC Register

Name: FIQVEC

Address: 0xFFFF011C

Default value: 0x00000000

Access: Read only

Table 74. FIQVEC MMR Bit Designations

Bit	Access	Initial Value	Description
31:23	Read only	0	Always read as 0.
22:7	Read only	0	IRQBASE register value.
6:2		0	Highest priority FIQ source. This is a value between 0 to 19 that represents the possible interrupt sources. For example, if the highest currently active FIQ is Timer1, then these bits are [01000].
1:0	Reserved	0	Reserved bits.

Bit	Name	Description
5:4	T0FORMAT	Format. [00] = binary (default). [01] = reserved. [10] = hours:minutes:seconds:hundredths (23 hours to 0 hours). [11] = hours:minutes:seconds:hundredths (255 hours to 0 hours).
3:0	T0SCALE	Prescaler. [0000] = source clock/1 (default). [0100] = source clock/16. [1000] = source clock/256. [1111] = source clock/32,768. Note that all other values are undefined.

TIMER1 OR WAKE-UP TIMER

Timer1 is a 32-bit wake-up timer, count down or count up, with a programmable prescaler. The prescaler is clocked directly from one of four clock sources, namely, the core clock (which is the default selection), external 32.768 kHz watch crystal, or the 32.768 kHz oscillator. The selected clock source can be scaled by a factor of 1, 16, 256, or 32,768. The wake-up timer continues to run when the core clock is disabled. This gives a minimum resolution of 97.66 ns when operating at CD zero, the core is operating at 10.24 MHz, and with a prescaler of 1 (ignoring the external GPIOs).

The counter can be formatted as a plain 32-bit value or as hours:minutes:seconds:hundredths.

Timer1 reloads the value from T1LD either when Timer1 overflows or immediately when T1LD is written.

The Timer1 interface consists of four MMRS.

- T1LD and T1VAL are 32-bit registers and hold 32-bit, unsigned integers. T1VAL is read only.
- T1CLRI is an 8-bit register. Writing any value to this register clears the Timer1 interrupt.
- T1CON is the configuration MMR, described in Table 81.

Timer1 Load Registers

Name: T1LD

Address: 0xFFFF0340

Default value: 0x00000000

Access: Read and write

Function: T1LD is a 32-bit register that holds the 32-bit value that is loaded into the counter.

Timer1 Clear Register

Name: T1CLRI

Address: 0xFFFF034C

Access: Write only

Function: This 8-bit, write-only MMR is written (with any value) by user code to clear the interrupt.

Timer1 Value Register

Name: T1VAL

Address: 0xFFFF0344

Default value: 0xFFFFFFFF

Access: Read only

Function: T1VAL is a 32-bit register that holds the current value of Timer1.

On power-up, PWMCON defaults to 0x0012 (HOFF = 1 and HMODE = 1). All GPIO pins associated with the PWM are configured in PWM mode by default (seeTable 86). Clear the PWM trip interrupt by writing any value to the PWMCLRI MMR. Note that when using the PWM trip interrupt, clear the PWM interrupt before exiting the ISR. This prevents generation of multiple interrupts.

Table 86. PWM Output Selection

PWMCON MMR[1]				PWM Outputs[2]			
ENA	**HOFF**	**POINV**	**DIR**	**PWM0**	**PWM1**	**PWM2**	**PWM3**
0	0	X	X	1	1	1	1
X	1	X	X	1	0	1	0
1	0	0	0	0	0	HS1	LS1
1	0	0	1	HS1	LS1	0	0
1	0	1	0	HS1	LS1	1	1
1	0	1	1	1	1	HS1	LS1

[1] X is don't care.
[2] HS = high side, LS = low side.

Table 87. Compare Registers

Name	Address	Default Value	Access
PWM0COM0	0xFFFF0F84	0x0000	R/W
PWM0COM1	0xFFFF0F88	0x0000	R/W
PWM0COM2	0xFFFF0F8C	0x0000	R/W
PWM1COM0	0xFFFF0F94	0x0000	R/W
PWM1COM1	0xFFFF0F98	0x0000	R/W
PWM1COM2	0xFFFF0F9C	0x0000	R/W
PWM2COM0	0xFFFF0FA4	0x0000	R/W
PWM2COM1	0xFFFF0FA8	0x0000	R/W
PWM2COM2	0xFFFF0FAC	0x0000	R/W

PWM0COM0 Compare Register

Name: PWM0COM0

Address: 0xFFFF0F84

Default value: 0x0000

Access: Read and write

Function: PWM0 output pin goes high when the PWM timer reaches the count value stored in this register.

PWM0COM1 Compare Register

Name: PWM0COM1

Address: 0xFFFF0F88

Default value: 0x0000

Access: Read and write

Function: PWM0 output pin goes low when the PWM timer reaches the count value stored in this register.

PWM0COM2 Compare Register

Name: PWM0COM2

Address: 0xFFFF0F8C

Default value: 0x0000

Access: Read and write

Function: PWM1 output pin goes low when the PWM timer reaches the count value stored in this register.

PWM0LEN Register

Name: PWM0LEN

Address: 0xFFFF0F90

Default value: 0x0000

Access: Read and write

Function: PWM1 output pin goes high when the PWM timer reaches the value stored in this register.

PWM1COM0 Compare Register

Name: PWM1COM0

Address: 0xFFFF0F94

Default value: 0x0000

Access: Read and write

Function: PWM2 output pin goes high when the PWM timer reaches the count value stored in this register.

PWM1COM1 Compare Register

Name: PWM1COM1

Address: 0xFFFF0F98

Default value: 0x0000

Access: Read and write

Function: PWM2 output pin goes low when the PWM timer reaches the count value stored in this register.

PWM1COM2 Compare Register

Name: PWM1COM2

Address: 0xFFFF0F9C

Default value: 0x0000

Access: Read and write

Function: PWM3 output pin goes low when the PWM timer reaches the count value stored in this register.

PWM1LEN Register

Name: PWM1LEN

Address: 0xFFFF0FA0

Default value: 0x0000

Access: Read and write

Function: PWM3 output pin goes high when the PWM timer reaches the value stored in this register.

UART Transmit Register

Write to this 8-bit register (COMTX) to transmit data using the UART.

COMTX Register

Name: COMTX

Address: 0xFFFF0700

Access: Write only

UART Receive Register

This 8-bit register (COMRX) is read to receive data transmitted using the UART.

COMRX Register

Name: COMRX

Address: 0xFFFF0700

Default value: 0x00

Access: Read only

UART Divisor Latch Register 0

This 8-bit register (COMDIV0) contains the least significant byte of the divisor latch that controls the baud rate at which the UART operates.

COMDIV0 Register

Name: COMDIV0

Address: 0xFFFF0700

Default value: 0x00

Access: Read and write

UART Divisor Latch Register 1

This 8-bit register contains the most significant byte of the divisor latch that controls the baud rate at which the UART operates.

COMDIV1 Register

Name: COMDIV1

Address: 0xFFFF0704

Default value: 0x00

Access: Read and write

UART Control Register 0

This 8-bit register (COMCON0) controls the operation of the UART in conjunction with COMCON1.

COMCON0 Register

Name: COMCON0

Address: 0xFFFF070C

Default value: 0x00

Access: Read and write

Table 90. COMCON0 MMR Bit Designations

Bit	Name	Description
7	DLAB	Divisor latch access. Set by user to enable access to the COMDIV0 and COMDIV1 registers. Cleared by user to disable access to COMDIV0 and COMDIV1 and enable access to COMRX, COMTX, and COMIEN0.
6	BRK	Set break. Set by user to force transmit to 0. Cleared to operate in normal mode.
5	SP	Stick parity. Set by user to force parity to defined values. 1 if EPS = 1 and PEN = 1. 0 if EPS = 0 and PEN = 1.
4	EPS	Even parity select bit. Set for even parity. Cleared for odd parity.
3	PEN	Parity enable bit. Set by user to transmit and check the parity bit. Cleared by user for no parity transmission or checking.
2	Stop	Stop bit. Set by user to transmit 1.5 stop bits if the word length is 5 bits, or 2 stop bits if the word length is 6 bits, 7 bits, or 8 bits. The receiver checks the first stop bit only, regardless of the number of stop bits selected. Cleared by user to generate one stop bit in the transmitted data.
1:0	WLS	Word length select. [00] = 5 bits. [01] = 6 bits. [10] = 7 bits. [11] = 8 bits.

UART Control Register 1

This 8-bit register controls the operation of the UART in conjunction with COMCON0.

COMCON1 Register

Name: COMCON1

Address: 0xFFFF0710

Default value: 0x00

Access: Read and write

Table 91. COMCON1 MMR Bit Designations

Bit	Name	Description
7:5		Reserved bits. Not used.
4	LOOPBACK	Loopback. Set by user to enable loopback mode. In loopback mode, the transmit pin is forced high.
3:2		Reserved bits. Not used.
1	RTS	Request to send. Set by user to force the RTS output to 0. Cleared by user to force the RTS output to 1.
0	DTR	Data terminal ready. Set by user to force the DTR output to 0. Cleared by user to force the DTR output to 1.

UART Status Register 0

COMSTA0 Register

Name: COMSTA0

Address: 0xFFFF0714

Default value: 0x60

Access: Read only

Function: This 8-bit read-only register reflects the current status on the UART.

Table 92. COMSTA0 MMR Bit Designations

Bit	Name	Description
7		Reserved.
6	TEMT	COMTX and shift register empty status bit. Set automatically if COMTX and the shift register are empty. This bit indicates that the data has been transmitted, that is, no more data is present in the shift register. Cleared automatically when writing to COMTX.
5	THRE	COMTX empty status bit. Set automatically if COMTX is empty. COMTX can be written as soon as this bit is set; the previous data might not have been transmitted yet and can still be present in the shift register. Cleared automatically when writing to COMTX.
4	BI	Break indicator. Set when P1.0/IRQ1/SIN/T0 pin is held low for more than the maximum word length. Cleared automatically.
3	FE	Framing error. Set when the stop bit is invalid. Cleared automatically.
2	PE	Parity error. Set when a parity error occurs. Cleared automatically.
1	OE	Overrun error. Set automatically if data is overwritten before being read. Cleared automatically.
0	DR	Data ready. Set automatically when COMRX is full. Cleared by reading COMRX.

Table 95. COMIID0 MMR Bit Designations

Status Bits[2:1]	Bit 0	Priority	Definition	Clearing Operation
00	1		No interrupt	
11	0	1	Receive line status interrupt	Read COMSTA0
10	0	2	Receive buffer full interrupt	Read COMRX
01	0	3	Transmit buffer empty interrupt	Write data to COMTX or read COMIID0
00	0	4	Modem status interrupt	Read COMSTA1 register

Table 96. COMDIV2 MMR Bit Designations

Bit	Name	Description
15	FBEN	Fractional baud rate generator enable bit. Set by user to enable the fractional baud rate generator. Cleared by user to generate the baud rate using the standard 450 UART baud rate generator.
14:13		Reserved.
12:11	FBM[1:0]	M. If FBM = 0, M = 4. See Equation 2 for the calculation of the baud rate using a fractional divider and Table 88 for common baud rate values.
10:0	FBN[10:0]	N. See Equation 2 for the calculation of the baud rate using a fractional divider and Table 88 for common baud rate values.

UART Fractional Divider Register

This 16-bit register (COMDIV2) controls the operation of the fractional divider for the ADuC7060/ADuC7061.

COMDIV2 Register

Name: COMDIV2

Address: 0xFFFF072C

Default value: 0x0000

Access: Read and write

Table 104. I2CSCON MMR Bit Designations

Bit	Name	Description
15:11		Reserved bits.
10	I2CSTXENI	Slave transmit interrupt enable bit. Set this bit to enable an interrupt after a slave transmits a byte. Clear this interrupt source.
9	I2CSRXENI	Slave receive interrupt enable bit. Set this bit to enable an interrupt after the slave receives data. Clear this interrupt source.
8	I2CSSENI	I^2C stop condition detected interrupt enable bit. Set this bit to enable an interrupt on detecting a stop condition on the I^2C bus. Clear this interrupt source.
7	I2CNACKEN	I^2C no acknowledge enable bit. Set this bit to no acknowledge the next byte in the transmission sequence. Clear this bit to let the hardware control the acknowledge/no acknowledge sequence.
6		Reserved. A value of 0 should be written to this bit.
5	I2CSETEN	I^2C early transmit interrupt enable bit. Setting this bit enables a transmit request interrupt just after the positive edge of SCL during the read bit transmission. Clear this bit to enable a transmit request interrupt just after the negative edge of SCL during the read bit transmission.
4	I2CGCCLR	I^2C general call status and ID clear bit. Writing a 1 to this bit clears the general call status and ID bits in the I2CSSTA register. Clear this bit at all other times.
3	I2CHGCEN	Hardware general call enable. When this bit and Bit 2 are set, and having received a general call (Address 0x00) and a data byte, the device checks the contents of the I2CALT against the receive register. If the contents match, the device has received a hardware general call. This is used if a device needs urgent attention from a master device without knowing which master it needs to turn to. This is a "to whom it may concern" call. The ADuC7060/ADuC7061 watches for these addresses. The device that requires attention embeds its own address into the message. All masters listen, and the one that can handle the device contacts its slave and acts appropriately. The LSB of the I2CALT register should always be written to 1, as per the I^2C January 2000 bus specification.
2	I2CGCEN	General call enable bit. Set this bit to enable the slave device to acknowledge an I^2C general call, Address 0x00 (write). The device then recognizes a data bit. If it receives a 0x06 (reset and write programmable part of the slave address by hardware) as the data byte, the I^2C interface resets as per the I^2C January 2000 bus specification. This command can be used to reset an entire I^2C system. If it receives a 0x04 (write programmable part of the slave address by hardware) as the data byte, the general call interrupt status bit sets on any general call. The user must take corrective action by reprogramming the device address.
1	ADR10EN	I^2C 10-bit address mode. Set to 1 to enable 10-bit address mode. Clear to 0 to enable normal address mode.
0	I2CSEN	I^2C slave enable bit. Set by user to enable I^2C slave mode. Clear to disable I^2C slave mode.

GENERAL-PURPOSE I/O

The ADuC7060/ADuC7061 features up to 16 general-purpose bidirectional input/output (GPIO) pins. In general, many of the GPIO pins have multiple functions that are configurable by user code. By default, the GPIO pins are configured in GPIO mode. All GPIO pins have an internal pull-up resistor with a drive capability of 1.6 mA.

All I/O pins are 3.3 V tolerant, meaning that the GPIOs support an input voltage of 3.3 V.

When the ADuC7060/ADuC7061 enters power-saving mode, the GPIO pins retain their state.

The GPIO pins are grouped into three port buses.

Table 110 lists all the GPIO pins and their alternative functions. A GPIO pin alternative function can be selected by writing to the correct bits of the GPxCON register.

Table 110. GPIO Multifunction Pin Descriptions

	Configuration via GPxCON Including GP0CON0		
Port	**Pin Mnemonic**	**00**	**01**
0	P0.0/$\overline{SS}$	GPIO	$\overline{SS}$ (SPI slave select).
	P0.1/SCLK/SCL	GPIO	SCLK/SCL (serial clock/SPI clock).
	P0.2/MISO	GPIO	MISO (SPI—master in/slave out).
	P0.3/MOSI/SDA	GPIO	MOSI (SPI—master out/slave in).
	P0.4/IRQ0/PWM1	GPIO/IRQ0	PWM1 (PWM Output 1).
	P0.5/CTS	GPIO	CTS. UART clear to send pin.
	P0.6/RTS	GPIO	RTS. UART request to send pin.
1	P1.0/IRQ1/SIN/T0	GPIO/IRQ1	SIN (serial input).
	P1.1/SOUT	GPIO	SOUT (serial output).
	P1.2/SYNC	GPIO	PWM sync (PWM sync input pin).
	P1.3/TRIP	GPIO	PWM trip (PWM trip input pin).
	P1.4/PWM2	GPIO	PWM2 (PWM Output 2).
	P1.5/PWM3	GPIO	PWM3 (PWM Output 3).
	P1.6/PWM4	GPIO	PWM4 (PWM Output 4).
2	P2.0/IRQ2/PWM0/EXTCLK	GPIO/IRQ2/EXTCLK	PWM0 (PWM Output 0).
	P2.1/IRQ3/PWM5	GPIO/IRQ3	PWM5 (PWM Output 5).

GPxCON REGISTERS

GPxCON are the Port x (where x is 0, 1, or 2) control registers, which select the function of each pin of Port x as described in Table 112.

Table 111. GPxCON Registers

Name	Address	Default Value	Access
GP0CON0	0xFFFF0D00	0x00000000	R/W
GP1CON	0xFFFF0D04	0x00000000	R/W
GP2CON	0xFFFF0D08	0x00000000	R/W