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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	10MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	POR, PWM, Temp Sensor, WDT
Number of I/O	14
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 32
Voltage - Supply (Vcc/Vdd)	2.375V ~ 2.625V
Data Converters	A/D 5x24b, 8x24b; D/A 1x14b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/aduc7060bstz32-rl

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
ADC SPECIFICATIONS: ANALOG INPUT	Internal V_{REF} = 1.2 V				
Main Channel					
Absolute Input Voltage Range	Applies to both VIN+ and VIN−	0.1		V_{DD} − 0.7	V
Input Voltage Range	Gain = 1[1]	0		1.2	V
(Differential Voltage Between AIN+ and AIN−)	Gain = 2[1]	0		600	mV
	Gain = 4[1]	0		300	mV
	Gain = 8[1]	0		150	mV
	Gain = 16[1]	0		75	mV
	Gain = 32[1]	0		37.5	mV
	Gain = 64[1]	0		18.75	mV
	Gain = 128[1]	0		9.375	mV
Common Mode Voltage, V_{CM}[10]	V_{CM} = (AIN(+) + AIN(−))/2, gain = 4 to 128	0.5			V
Input Leakage Current[1]	ADC0 and ADC1		10	18[1]	nA
	ADC2, ADC3, ADC4, and ADC5		15	30[1]	nA
	ADC6, ADC7, ADC8, and ADC9, VREF+, VREF−		15	25[1]	nA
	Measurements are taken when the ADC is not opearating				
Common-Mode Rejection DC[1]					
On ADC Input	ADC = 7.8 mV	113			dB
	ADC = 1 V[1]		95		dB
Common-Mode Rejection 50 Hz/60 Hz[1]	50 Hz/60 Hz ± 1 Hz, 16.6 Hz and 50 Hz update rate, chop on				
	ADC = 7.8 mV, range ± 20 mV	95			dB
	ADC = 1 V, range ± 1.2 V	90			dB
Normal-Mode Rejection 50 Hz/60 Hz[1]					
On ADC Input	50 Hz/60 Hz ± 1 Hz, 16.6 Hz f_{ADC}, chop on	75			dB
	50 Hz/60 Hz ± 1 Hz, 16.6 Hz f_{ADC}, chop off	67			dB
Auxiliary Channel					
Absolute Input Voltage Range[1]	Buffer enabled	0.1		AVDD − 0.1	V
	Buffer disabled	AGND		AVDD	V
Input Voltage Range	Range-based reference source	0		1.2	V
Common-Mode Rejection DC[1]					
On ADC Input	ADC = 1 V[1]		87		dB
Common-Mode Rejection 50 Hz/60 Hz[1]	50 Hz/60 Hz ± 1 Hz, 16.6 Hz and 50 Hz update rate, chop on				
	ADC = 1 V, range ± 1.2 V	90			dB
Normal-Mode Rejection 50 Hz/60 Hz[1]					
On ADC Input	50 Hz/60 Hz ± 1 Hz, 16.6 Hz f_{ADC}, chop on	75			dB
	50 Hz/60 Hz ± 1 Hz, 16.6 Hz f_{ADC}, chop off	67			dB
VOLTAGE REFERENCE					
ADC Precision Reference					
Internal V_{REF}			1.2		V
Initial Accuracy	Measured at T_A = 25°C	−0.1		+0.1	%
Reference Temperature Coefficient (Tempco)[1, 11]		−20	±10	+20	ppm/°C
Power Supply Rejection[1]			70		dB
External Reference Input Range[12]		0.1		AVDD	V
V_{REF} Divide-by-2 Initial Error[1]			0.1		%

TIMING SPECIFICATIONS

I²C Timing

Table 2. I²C® Timing in Standard Mode (100 kHz)

Parameter	Description	Slave		Unit
		Min	Max	
t_L	SCLOCK low pulse width	4.7		µs
t_H	SCLOCK high pulse width	4.0		ns
t_{SHD}	Start condition hold time	4.0		µs
t_{DSU}	Data setup time	250		ns
t_{DHD}	Data hold time	0	3.45	µs
t_{RSU}	Setup time for repeated start	4.7		µs
t_{PSU}	Stop condition setup time	4.0		µs
t_{BUF}	Bus-free time between a stop condition and a start condition	4.7		µs
t_R	Rise time for both CLOCK and SDATA		1	µs
t_F	Fall time for both CLOCK and SDATA		300	ns

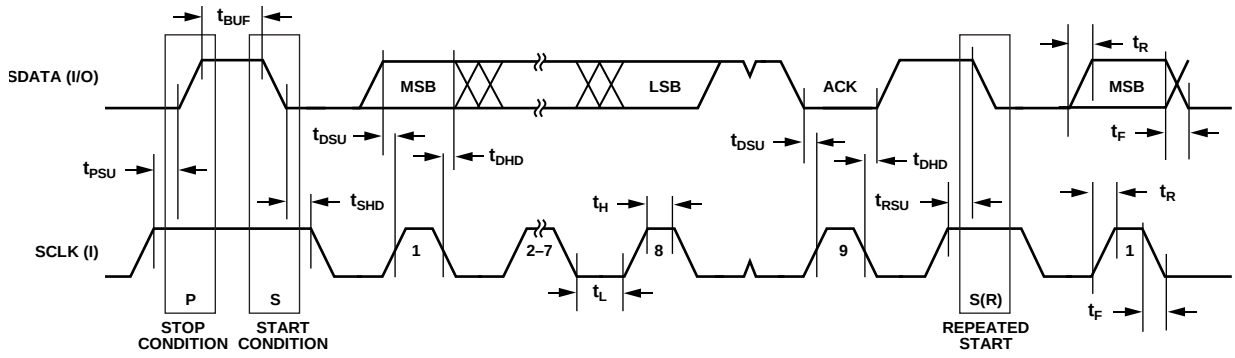

Figure 2. I²C Compatible Interface Timing

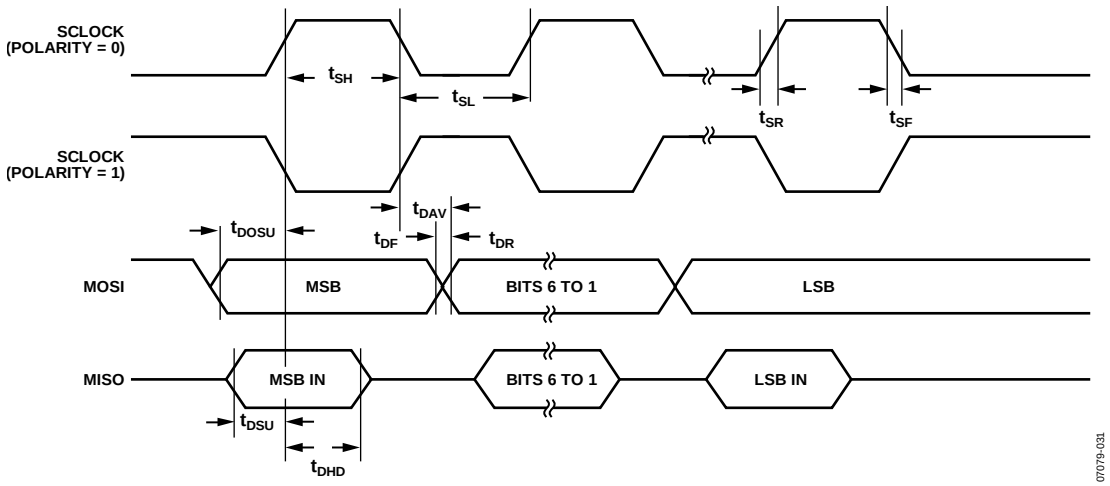

Figure 4. SPI Master Mode Timing (Phase Mode = 0)

Table 5. SPI Slave Mode Timing (Phase Mode = 1)

Parameter	Description	Min	Typ	Max	Unit
$t_{\overline{CS}}$	$\overline{CS}$ to SCLOCK edge[1]	$(2 \times t_{HCLK}) + (2 \times t_{UCLK})$			ns
t_{SL}	SCLOCK low pulse width	$2 \times t_{UCLK}$			ns
t_{SH}	SCLOCK high pulse width	$2 \times t_{UCLK}$			ns
t_{DAV}	Data output valid after SCLOCK edge			40	ns
t_{DSU}	Data input setup time before SCLOCK edge[1]	$1 \times t_{UCLK}$			ns
t_{DHD}	Data input hold time after SCLOCK edge[1]	$2 \times t_{UCLK}$			ns
t_{DF}	Data output fall time		30	40	ns
t_{DR}	Data output rise time		30	40	ns
t_{SR}	SCLOCK rise time	1			ns
t_{SF}	SCLOCK fall time	1			ns
t_{SFS}	$\overline{CS}$ high after SCLOCK edge	0			ns

[1] t_{UCLK} = 97.6 ns. It corresponds to the 10.24 MHz internal clock from the PLL.

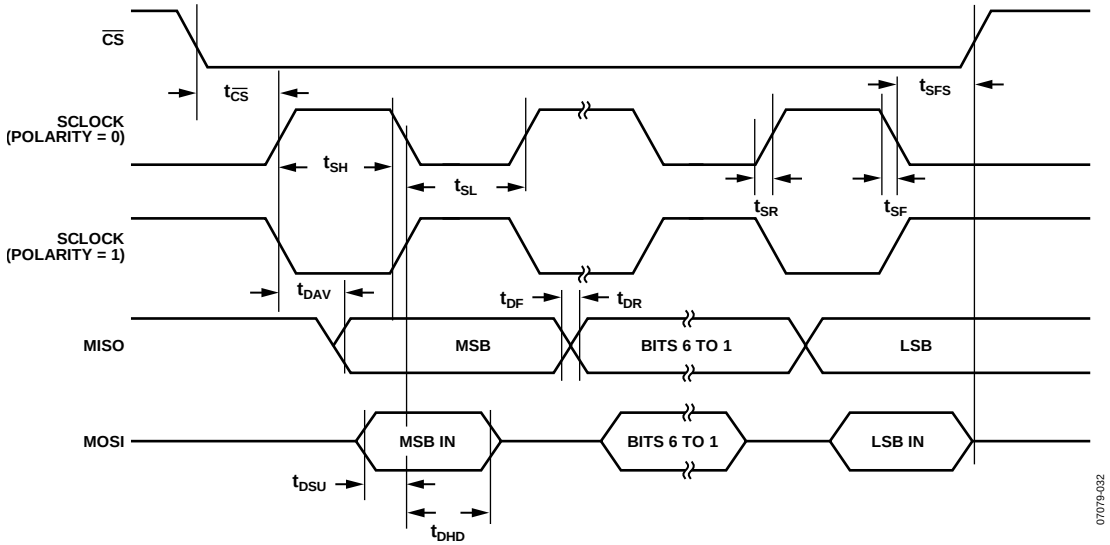

Figure 5. SPI Slave Mode Timing (Phase Mode = 1)

Pin No.	Mnemonic	Type[1]	Description
12	ADC5/EXT_REF2IN−	I	Single-Ended or Differential Analog Input 5/External Reference Negative Input. This is a dual function analog input pin. ADC5 serves as the analog input for the auxiliary ADC. EXT_REF2IN− serves as the external reference negative input by ADC for the auxiliary channel.
13	ADC4/EXT_REF2IN+	I	Multifunction Analog Input Pin. This pin can be used for the single-ended or differential Analog Input 4, which is the analog input for the auxiliary ADC, or it can be used for the external reference positive input for the auxiliary channel.
14	ADC3	I	Single-Ended or Differential Analog Input 3. Analog input for the primary and auxiliary ADCs.
15	ADC2	I	Single-Ended or Differential Analog Input 2. Analog input for the primary and auxiliary ADCs.
16	IEXC1	O	Programmable Current Source. Analog output pin.
17	IEXC0	O	Programmable Current Source. Analog output pin.
18	GND_SW	I	Switch to Internal Analog Ground Reference. When this input pin is not used, connect it directly to the AGND system ground.
19	ADC1	I	Single-Ended or Differential Analog Input 1. Analog input for the primary ADC. Negative differential input for primary ADC.
20	ADC0	I	Single-Ended or Differential Analog Input 0. Analog input for the primary ADC. Positive differential input for primary ADC.
21	VREF+	I	External Reference Positive Input for the Primary Channel. Analog input pin.
22	VREF−	I	External Reference Negative Input for the Primary Channel. Analog input pin.
23	AGND	S	Analog Ground.
24	AVDD	S	Analog Supply Pin.
25	ADC6	I	Analog Input 6 for Auxiliary ADC. Single-ended or differential Analog Input 6.
26	ADC7	I	Analog Input 7 for Auxiliary ADC. Single-ended or differential Analog Input 7.
27	ADC8	I	Analog Input 8 for Auxiliary ADC. Single-ended or differential Analog Input 8.
28	ADC9	I	Analog Input 9 for Auxiliary ADC. Single-ended or differential Analog Input 9.
29	DGND	S	Digital Ground.
30	DVDD	S	Digital Supply Pin.
31	P0.0/$\overline{SS}$	I/O	General-Purpose Input and General-Purpose Output P0.0/SPI Slave Select Pin (Active Low). This is a dual function input/output pin.
32	P0.1/SCLK/SCL	I/O	General-Purpose Input and General-Purpose Output P0.1/SPI Clock Pin/I²C Clock Pin. This is a triple function input/output pin.
33	P0.2/MISO	I/O	General-Purpose Input and General-Purpose Output P0.2/SPI Master Input Slave Output. This is a dual function input/output pin.
34	P0.3/MOSI/SDA	I/O	General-Purpose Input and General-Purpose Output P0.3/SPI Master Output Slave Input/I²C Data Pin. This is a triple function input/output pin.
35	XTALO	O	External Crystal Oscillator Output Pin.
36	XTALI	I	External Crystal Oscillator Input Pin.
37	P0.4/IRQ0/PWM1	I/O	General-Purpose Input and General-Purpose Output P0.4/External Interrupt Request 0/PWM1 Output. This is a triple function input/output pin.
38	P2.0/IRQ2/PWM0/EXTCLK	I/O	General-Purpose Input and General-Purpose Output P2.0/External Interrupt Request 2/PWM0 Output/External Clock Input. This is a multifunction input/output pin.
39	P1.4/PWM2	I/O	General-Purpose Input and General-Purpose Output P1.4/PWM2 Output. This is a dual function input/output pin.
40	P1.5/PWM3	I/O	General-Purpose Input and General-Purpose Output P1.5/PWM3 Output. This is a dual function input/output pin.
41	P1.6/PWM4	I/O	General-Purpose Input and General-Purpose Output P1.6/PWM4 Output. This is a dual function input/output pin.
42	P2.1/IRQ3/PWM5	I/O	General-Purpose Input and General-Purpose Output P2.1/External Interrupt Request 3/PWM5 Output. This is a triple function input/output pin.

TERMINOLOGY

Conversion Rate
The conversion rate specifies the rate at which an output result is available from the ADC, when the ADC has settled.

The sigma-delta (Σ-Δ) conversion techniques used on this part mean that whereas the ADC front-end signal is oversampled at a relatively high sample rate, a subsequent digital filter is used to decimate the output, giving a valid 24-bit data conversion result at output rates from 1 Hz to 8 kHz.

Note that, when software switches from one input to another (on the same ADC), the digital filter must first be cleared and then allowed to average a new result. Depending on the configuration of the ADC and the type of filter, this can take multiple conversion cycles.

Integral Nonlinearity (INL)
INL is the maximum deviation of any code from a straight line passing through the endpoints of the transfer function. The endpoints of the transfer function are zero scale, a point ½ LSB below the first code transition, and full scale, a point ½ LSB above the last code transition (111 . . . 110 to 111 . . . 111). The error is expressed as a percentage of full scale.

No Missing Codes
No missing codes is a measure of the differential nonlinearity of the ADC. The error is expressed in bits and specifies the number of codes (ADC results) as 2N bits, where N is no missing codes guaranteed to occur through the full ADC input range.

Offset Error
Offset error is the deviation of the first code transition ADC input voltage from the ideal first code transition.

Offset Error Drift
Offset error drift is the variation in absolute offset error with respect to temperature. This error is expressed as least significant bits per degree Celsius.

Gain Error
Gain error is a measure of the span error of the ADC. It is a measure of the difference between the measured and the ideal span between any two points in the transfer function.

Output Noise
The output noise is specified as the standard deviation (or 1 × Sigma) of the distribution of the ADC output codes collected when the ADC input voltage is at a dc voltage. It is expressed as micro root mean square. The output, or root mean square (rms) noise, can be used to calculate the effective resolution of the ADC as defined by the following equation:

$$Effective\ Resolution = \log2(Full\text{-}Scale\ Range/rms\ Noise)\ \text{bits}$$

The peak-to-peak noise is defined as the deviation of codes that fall within 6.6 × Sigma of the distribution of ADC output codes collected when the ADC input voltage is at dc. The peak-to-peak noise is, therefore, calculated as

$$6.6 \times rms\ Noise$$

The peak-to-peak noise can be used to calculate the ADC (noise free code) resolution for which there is no code flicker within a 6.6-Sigma limit as defined by the following equation:

$$Noise\ Free\ Code\ Resolution = \log2\left(\frac{Full-Scale\ Range}{Peak-to-Peak\ Noise}\right)\ \text{bits}$$

Data Sheet Acronyms

ADC	analog-to-digital converter
ARM	advanced RISC machine
JTAG	joint test action group
LSB	least significant byte/bit
LVF	low voltage flag
MCU	microcontroller
MMR	memory mapped register
MSB	most significant byte/bit
PID	protected identifier
POR	power-on reset
PSM	power supply monitor
rms	root mean square

Table 19. Timer Address Base = 0xFFFF0300

Address	Name	Bytes	Access Type	Default Value	Description
0x0320	T0LD	4	R/W	0x00000000	Timer0 load register.
0x0324	T0VAL	4	R	0xFFFFFFFF	Timer0 value register.
0x0328	T0CON	4	R/W	0x01000000	Timer0 control MMR.
0x032C	T0CLRI	1	W	N/A	Timer0 interrupt clear register.
0x0330	T0CAP	4	R	0x00000000	Timer0 capture register.
0x0340	T1LD	4	R/W	0x00000000	Timer1 load register.
0x0344	T1VAL	4	R	0xFFFFFFFF	Timer1 value register.
0x0348	T1CON	2	R/W	0x0000	Timer1 control MMR.
0x034C	T1CLRI	1	W	N/A	Timer1 interrupt clear register.
0x0360	T2LD	2	R/W	0x3BF8	Timer2 load register.
0x0364	T2VAL	2	R	0x3BF8	Timer2 value register.
0x0368	T2CON	2	R/W	0x0000	Timer2 control MMR.
0x036C	T2CLRI	1	W	N/A	Timer2 interrupt clear register.
0x0380	T3LD	2	R/W	0x0000	Timer3 load register.
0x0384	T3VAL	2	R	0xFFFF	Timer3 value register.
0x0388	T3CON	4	R/W	0x00000000	Timer3 control MMR.
0x038C	T3CLRI	1	W	N/A	Timer3 interrupt clear register.
0x0390	T3CAP	2	R	0x0000	Timer3 capture register.

Table 20. PLL Base Address = 0xFFFF0400

Address	Name	Bytes	Access Type	Default Value	Description
0x0404	POWKEY1	2	W	0xXXXX	POWCON0 prewrite key.
0x0408	POWCON0	1	R/W	0x7B	Power control and core speed control register.
0x040C	POWKEY2	2	W	0xXXXX	POWCON0 postwrite key.
0x0410	PLLKEY1	2	W	0xXXXX	PLLCON prewrite key.
0x0414	PLLCON	1	R/W	0x00	PLL clock source selection MMR.
0x0418	PLLKEY2	2	W	0xXXXX	PLLCON postwrite key.
0x0434	POWKEY3	2	W	0xXXXX	POWCON1 prewrite key.
0x0438	POWCON1	2	R/W	0x124	Power control register.
0x043C	POWKEY4	2	W	0xXXXX	POWCON1 postwrite key.
0x0464	GP0KEY1	2	W	0xXXXX	GP0CON1 prewrite key.
0x0468	GP0CON1	1	R/W	0x00	Configures P0.0, P0.1, P0.2, and P0.3 as analog inputs or digital I/Os. Also enables SPI or I^2C mode.
0x046C	GP0KEY2	2	W	0xXXXX	GP0CON1 postwrite key.

RESET

There are four kinds of resets: external reset, power-on reset, watchdog reset, and software reset. The RSTSTA register indicates the source of the last reset and can be written by user code to initiate a software reset event.

The bits in this register can be cleared to 0 by writing to the RSTCLR MMR at 0xFFFF0234. The bit designations in RSTCLR mirror those of RSTSTA. These registers can be used during a reset exception service routine to identify the source of the reset. The implications of all four kinds of reset events are tabulated in Table 30.

RSTSTA Register

Name: RSTSTA

Address: 0xFFFF0230

Default value: Depends on type of reset

Access: Read and write

Function: This 8-bit register indicates the source of the last reset event and can be written by user code to initiate a software reset.

RSTCLR Register

Name: RSTCLR

Address: 0xFFFF0234

Access: Write only

Function: This 8-bit write only register clears the corresponding bit in RSTSTA.

Table 29. RSTSTA/RSTCLR MMR Bit Designations

Bit	Description
7:4	Not used. These bits are not used and always read as 0.
3	External reset. Automatically set to 1 when an external reset occurs. This bit is cleared by setting the corresponding bit in RSTCLR.
2	Software reset. This bit is set to 1 by user code to generate a software reset. This bit is cleared by setting the corresponding bit in RSTCLR.[1]
1	Watchdog timeout. Automatically set to 1 when a watchdog timeout occurs. Cleared by setting the corresponding bit in RSTCLR.
0	Power-on reset. Automatically set when a power-on reset occurs. Cleared by setting the corresponding bit in RSTCLR.

[1] If the software reset bit in RSTSTA is set, any write to RSTCLR that does not clear this bit generates a software reset.

Table 30. Device Reset Implications

RESET	Reset External Pins to Default State	Kernel Executed	Reset All External MMRs (Excluding RSTSTA)	Peripherals Reset	Watchdog Timer Reset	RAM Valid	RSTSTA (Status After Reset Event)
POR	Yes	Yes	Yes	Yes	Yes	Yes/No	RSTSTA[0] = 1
Watchdog	Yes	Yes	Yes	Yes	No	Yes	RSTSTA[1] = 1
Software	Yes	Yes	Yes	Yes	No	Yes	RSTSTA[2] = 1
External Pin	Yes	Yes	Yes	Yes	No	Yes	RSTSTA[3] = 1

Table 34. Typical Current Consumption at 25°C in mA[1]

POWCON0[6:3]	Mode	CD = 0	CD = 1	CD = 2	CD = 3	CD = 4	CD = 5	CD = 6	CD = 7
1111	Active[2]	5.22	4.04	2.69	2.01	1.67	1.51	1.42	1.38
1110	Pause[3]	2.6	1.95	1.6	1.49	1.4	1.33	1.31	1.3
1100	Nap[3]	1.33	1.29	1.29	1.29	1.29	1.29	1.29	1.29
1000	Sleep[3]	0.085	0.085	0.085	0.085	0.085	0.085	0.085	0.085
0000	Stop[3]	0.055	0.055	0.055	0.055	0.055	0.055	0.055	0.055

[1] All values listed in Table 34 have been taken with both ADCs turned off.
[2] In active mode, GP0PAR bit 7 =1.
[3] The values for pause, nap, sleep, and stop modes are measured with the NTRST pin low. To minimize I_{DD} due to nTRST in all modes, set GP0PAR Bit 7 =1. This disables the internal pull-down on the nTRST pin and means there is no ground path for the external pull-up resistor through the nTRST pin. By default, GP0PAR Bit 7 = 0, therefore, setting this bit in user code will not affect the $\overline{BM}$operation.

Name: PLLKEY1

Address: 0xFFFF0410

Default value: 0xXXXX

Access: Write

Function: When writing to the PLLCON register, the value of 0xAA must be written to this register in the instruction immediately before writing to PLLCON.

Table 35. PLLCON MMR Bit Designations

Bit	Name	Description
7:3	Reserved	These bits must always be set to 0.
2	EXTCLK	Set this bit to 1 to select external clock input from P2.0. Clear this bit to disable the external clock.
1:0	OSEL	Oscillator selection bits. [00] = internal 32,768 Hz oscillator. [01] = internal 32,768 Hz oscillator. [10] = external crystal. [11] = internal 32,768 Hz oscillator.

Name: PLLCON

Address: 0xFFFF0414

Default value: 0x00

Access: Read and write

Function: This register selects the clock input to the PLL.

Name: PLLKEY2

Address: 0xFFFF0418

Default value: 0xXXXX

Access: Write

Function: When writing to PLLCON, the value of 0x55 must be written to this register in the instruction immediately after writing to PLLCON.

ADC CIRCUIT INFORMATION

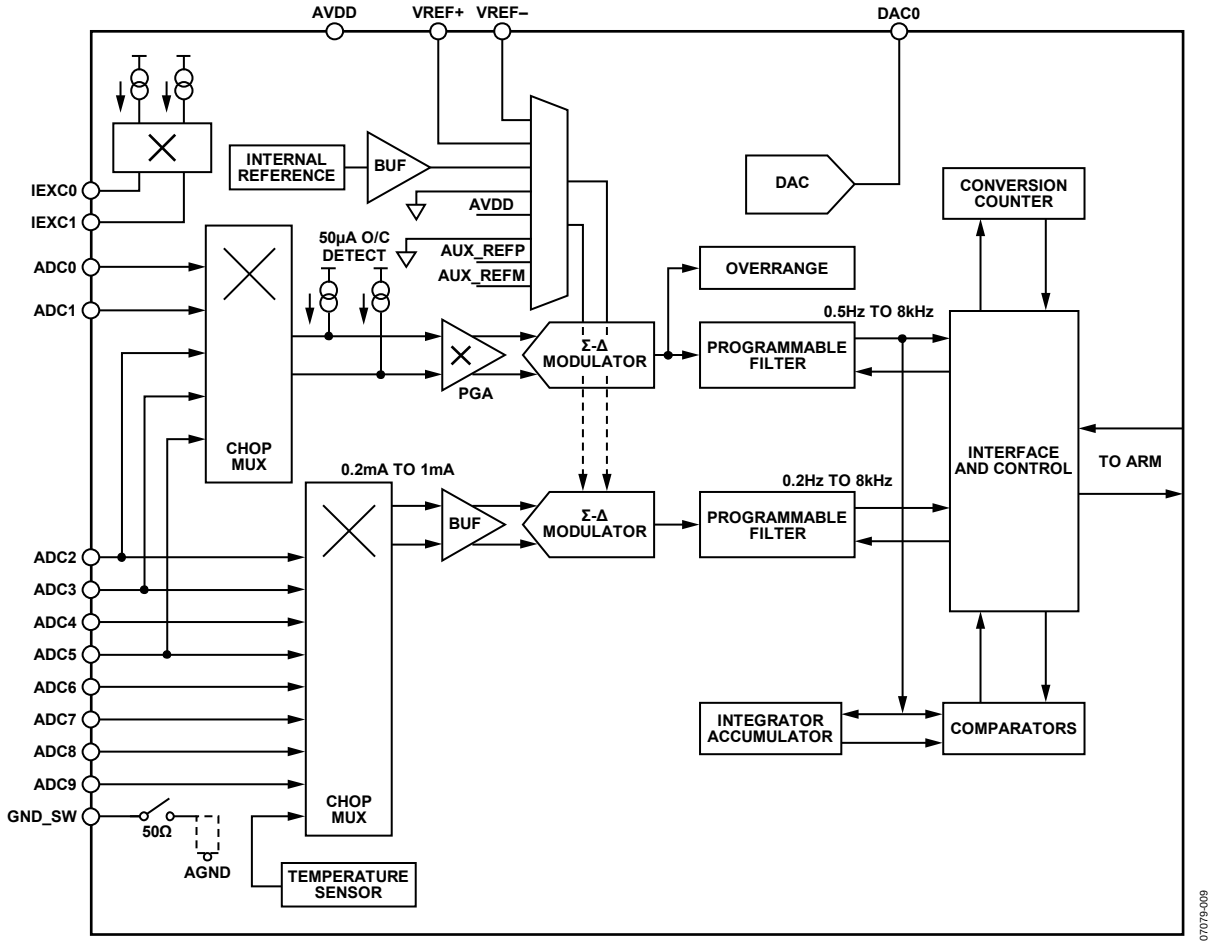

Figure 14. Analog Block Diagram

The ADuC7060/ADuC7061 incorporates two independent multichannel Σ-Δ ADCs. The primary ADC is a 24-bit, 4-channel ADC. The auxiliary ADC is a 24-bit Σ-Δ ADC, with up to seven single-ended input channels.

The primary ADC input has a mux and a programmable gain amplifier on its input stage. The mux on the primary channel can be configured as two fully differential input channels or as four single-ended input channels.

The auxiliary ADC incorporates a buffer on its input stage. Digital filtering is present on both ADCs, which allows measurement of a wide dynamic range and low frequency signals such as those in pressure sensor, temperature sensor, weigh scale, or strain gage type applications.

The ADuC7060/ADuC7061 auxiliary ADC can be configured as four fully differential input channels or as seven single-ended input channels.

Because of internal buffering, the internal channels can convert signals directly from sensors without the need for external signal conditioning.

Table 36. Primary ADC—Typical Output RMS Noise in Normal Mode (μV)[1]

ADC Register Status	Data Update Rate	Selectable Input Range (PGA Settings)									
		±1.2 V (PGA = 1)	±600 mV (PGA = 2)	±300 mV (PGA = 4)	±150 mV (PGA = 8)	±75 mV (PGA = 16)	±37.5 mV (PGA = 32)	±18.75 mV (PGA = 64)	±9.375 mV (PGA = 128)	±4.68 mV (PGA = 256)	±2.34 mV (PGA = 512)
Chop On	4 Hz	0.62 μV	0.648 μV	0.175 μV	0.109 μV	0.077 μV	0.041 μV	0.032 μV	0.0338 μV	0.032 μV	0.033 μV
Chop Off	50 Hz	1.97 μV	1.89 μV	0.570 μV	0.38 μV	0.27 μV	0.147 μV	0.123 μV	0.12 μV	0.098 μV	0.098 μV
Chop Off	1 kHz	8.54 μV	8.4 μV	2.55 μV	1.6 μV	1.17 μV	0.658 μV	0.53 μV	0.55 μV	0.56 μV	0.52 μV
Chop Off	8 kHz	54.97 μV	55.54 μV	14.30 μV	7.88 μV	4.59 μV	2.5 μV	1.71 μV	1.75 μV	0.915 μV	0.909 μV

[1] The input voltage range is centered around the common-mode voltage and should meet the input voltage range specified in the Electrical Specifications section.

Table 37. Primary ADC—Typical Output RMS Effective Number of Bits in Normal Mode (Peak-to-Peak Bits in Parentheses)

ADC Register Status	Data Update Rate	Input Voltage Noise (mV)									
		±1.2 V (PGA = 1)	±600 mV (PGA = 2)	±300 mV (PGA = 4)	±150 mV (PGA = 8)	±75 mV (PGA = 16)	±37.5 mV (PGA = 32)	±18.75 mV (PGA = 64)	±9.375 mV (PGA = 128)	±4.68 mV (PGA = 256)	±2.34 mV (PGA = 512)
Chop On	4 Hz	21.9 (19.1 p-p)	20.8 (18.1 p-p)	21.7 (19.0 p-p)	21.4 (18.7 p-p)	20.9 (18.2 p-p)	20.8 (18.1 p-p)	20.2 (17.4 p-p)	19.1 (16.4 p-p)	18.2 (15.4 p-p)	17.1 (14.4 p-p)
Chop Off	50 Hz	20.2 (17.5 p-p)	19.3 (16.6 p-p)	20.0 (17.3 p-p)	19.6 (16.9 p-p)	19.1 (16.4 p-p)	19.0 (16.2 p-p)	18.2 (15.5 p-p)	17.3 (14.6 p-p)	16.6 (13.8 p-p)	15.5 (12.8 p-p)
Chop Off	1 kHz	18.1 (15.3 p-p)	17.1 (14.4 p-p)	17.8 (15.1 p-p)	17.5 (14.8 p-p)	17.0 (14.2 p-p)	16.8 (14.1 p-p)	16.1 (13.4 p-p)	15.1 (12.3 p-p)	14.0 (11.3 p-p)	13.1 (10.4 p-p)
Chop Off	8 kHz	15.4 (12.7 p-p)	14.4 (11.7 p-p)	15.4 (12.6 p-p)	15.2 (12.5 p-p)	15.0 (12.3 p-p)	14.9 (12.2 p-p)	14.4 (11.7 p-p)	13.4 (10.7 p-p)	13.3 (10.6 p-p)	12.3 (9.6 p-p)

Table 38. Auxilary ADC—Typical Output RMS Noise

ADC Register	Data Update Rate	RMS Value
Chop On	4 Hz	0.633 μV
Chop On	10 Hz	0.810 μV
Chop Off	1 kHz	7.4 μV
Chop Off	8 kHz	54.18 μV

REFERENCE SOURCES

Both the primary and auxiliary ADCs have the option of using the internal reference voltage or one of two external differential reference sources. The first external reference is applied to the VREF+/VREF− pins. The second external reference is applied to the ADC4/EXT_REF2IN+ and ADC5/EXT_REF2IN− pins. By default, each ADC uses the internal 1.2 V reference source.

For details on how to configure the external reference source for the primary ADC, see the description of the ADC0REF[1:0] bits in the ADC0 control register, ADC0CON.

For details on how to configure the external reference source for the auxiliary ADC, see the description of the ADC1REF[2:0] bits in the ADC1 control register, ADC1CON.

If an external reference source of greater than 1.35 V is needed for ADC0, the HIGHEXTREF0 bit must be set in ADC0CON.

Similarly, if an external reference source of greater than 1.35 V is used for ADC1, the HIGHEXTREF1 bit must be set in ADC1CON.

DIAGNOSTIC CURRENT SOURCES

To detect a connection failure to an external sensor, the ADuC7060/ADuC7061 incorporates a 50 μA constant current source on the selected analog input channels to both the primary and auxiliary ADCs.

The diagnostic current sources for the primary ADC analog inputs are controlled by the ADC0DIAG[1:0] bits in the ADC0CON register.

Similarly, the diagnostic current sources for the auxiliary ADC analog inputs are controlled by the ADC1DIAG[1:0] bits in the ADC1CON register.

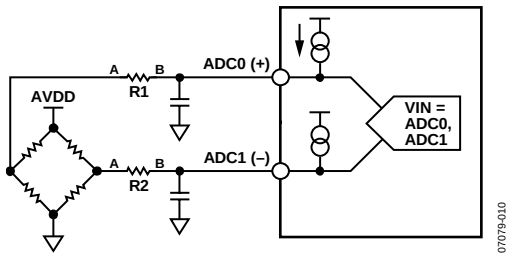

Figure 15. Example Circuit Using Diagnostic Current Sources

ADC Interrupt Mask Register

Name: ADCMSKI

Address: 0xFFFF0504

Default value: 0x0000

Access: Read and write

Function: This register allows the ADC interrupt sources to be enabled individually. The bit positions in this register are the same as the lower eight bits in the ADCSTA MMR. If a bit is set by user code to 1, the respective interrupt is enabled. By default, all bits are 0, meaning all ADC interrupt sources are disabled.

Table 41. ADCMSKI MMR Bit Designations

Bit	Name	Description
7		Not used. This bit is reserved for future functionality and should not be monitored by user code.
6	ADC0ATHEX_INTEN	ADC0 accumulator comparator threshold exceeded interrupt enable bit. When set to 1, this bit enables an interrupt when the ADC0ATHEX bit in the ADCSTA register is set. When this bit is cleared, this interrupt source is disabled.
5		Not used. This bit is reserved for future functionality and should not be monitored by user code.
4	ADC0THEX_INTEN	Primary channel ADC comparator threshold exceeded interrupt enable bit. When set to 1, this bit enables an interrupt when the ADC0THEX bit in the ADCSTA register is set. When this bit is cleared, this interrupt source is disabled.
3	ADC0OVR_INTEN	When set to 1, this bit enables an interrupt when the ADC0OVR bit in the ADCSTA register is set. When this bit is cleared, this interrupt source is disabled.
2		Not used. This bit is reserved for future functionality and should not be monitored by user code.
1	ADC1RDY_INTEN	Auxiliary ADC result ready bit. When set to 1, this bit enables an interrupt when the ADC1RDY bit in the ADCSTA register is set. When this bit is cleared, this interrupt source is disabled.
0	ADC0RDY_INTEN	Primary ADC result ready bit. When set to 1, this bit enables an interrupt when the ADC0RDY bit in the ADCSTA register is set. When this bit is cleared, this interrupt source is disabled.

ADC Mode Register

Name: ADCMDE

Address: 0xFFFF0508

Default value: 0x03

Access: Read and write

Function: The ADC mode MMR is an 8-bit register that configures the mode of operation of the ADC subsystem.

Table 42. ADCMDE MMR Bit Designations

Bit	Name	Description
7	ADCCLKSEL	Set this bit to 1 to enable ADCCLK = 512 kHz. This bit should be set for normal ADC operation. Clear this bit to enable ADCCLK = 131 kHz. This bit should be cleared for low power ADC operation.
6		Not used. This bit is reserved for future functionality and should not be monitored by user code.
5	ADCLPMEN	Enable low power mode. This bit has no effect if ADCMDE[4:3] = 00 (ADC is in normal mode). This bit must be set to 1 in low power mode. Clearing this bit in low power mode results in erratic ADC results.

Auxiliary ADC Control Register

Name: ADC1CON

Address: 0xFFFF0510

Default value: 0x0000

Access: Read and write

Function: The auxiliary ADC control MMR is a 16-bit register.

Table 44. ADC1CON MMR Bit Designations

Bit	Name	Description
15	ADC1EN	Auxiliary channel ADC enable. This bit is set to 1 by user code to enable the auxiliary ADC. Clearing this bit to 0 powers down the auxiliary ADC.
14:13	ADC1DIAG[1:0]	Diagnostic current source enable bits. This is the same current source as that used on ADC0DIAG[1:0]. The ADCs cannot enable the diagnostic current sources at the same time. [00]= current sources off. [01] = enables a 50 µA current source on selected positive input (for example, ADC2). [10] = enables a 50 µ A current source on selected negative input (for example, ADC3). [11] = enables a 50 µ A current source on both selected inputs (for example, ADC2 and ADC3).
12	HIGHEXTREF1	This bit must be set high if the external reference for ADC1 exceeds 1.35 V. This results in the reference source being divided by 2. Clear this bit when using the internal reference or an external reference of less than 1.35 V.
11	ADC1CODE	Auxiliary channel ADC output coding. This bit is set to 1 by user code to configure auxiliary ADC output coding as unipolar. This bit is cleared to 0 by user code to configure auxiliary ADC output coding as twos complement.
10:7	ADC1CH[3:0]	Auxiliary channel ADC input select. Note: Single-ended channels are selected with respect to ADC5. Bias ADC5 to a minimum level of 0.1 V. [0000] = ADC2/ADC3 (differential mode). [0001] = ADC4/ADC5 (differential mode). [0010] = ADC6/ADC7 (differential mode). [0011] = ADC8/ADC9 (differential mode). [0100] = ADC2/ADC5 (single-ended mode). [0101] = ADC3/ADC5 (single-ended mode). [0110] = ADC4/ADC5 (single-ended mode). [0111] = ADC6/ADC5 (single-ended mode). [1000] = ADC7/ADC5 (single-ended mode). [1001] = ADC8/ADC5 (single-ended mode). [1010] = ADC9/ADC5 (single-ended mode). [1011] = internal temperature sensor+/internal temperature sensor−. [1100] = VREF+, VREF−. Note: This is the reference selected by the ADC1REF bits. [1101] = DAC_OUT/AGND. [1110] = undefined. [1111] = internal short to ADC3.

Excitation Current Sources Control Register

Name: IEXCON

Address: 0xFFFF0570

Default value: 0x00

Access: Read and write

Function: This 8-bit MMR controls the two excitation current sources, IEXC0 and IEXC1.

Table 62. IEXCON MMR Bit Designations

Bit	Name	Description
7	IEXC1_EN	Enable bit for IEXC1 current source. Set this bit to 1 to enable Excitation Current Source 1. Clear this bit to disable Excitation Current Source 1.
6	IEXC0_EN	Enable bit for IEXC0 current source. Set this bit to 1 to enable Excitation Current Source 0. Clear this bit to disable Excitation Current Source 0.
5	IEXC1_DIR	Set this bit to 1 to direct Excitation Current Source 1 to the IEXC0 pin. Set this bit to 0 to direct Excitation Current Source 1 to the IEXC1 pin.
4	IEXC0_DIR	Set this bit to 1 to direct Excitation Current Source 0 to the IEXC1 pin. Set this bit to 0 to direct Excitation Current Source 0 to the IEXC0 pin.
3:1	IOUT[3:1]	These bits control the excitation current level for each source. IOUT[3:1] = 000, excitation current = 0 µA + (IOUT[0] × 10 µA). IOUT[3:1] = 001, excitation current = 200 µA + (IOUT[0] × 10 µA). IOUT[3:1] = 010, excitation current = 400 µA + (IOUT[0] × 10 µA). IOUT[3:1] = 011, excitation current = 600 µA + (IOUT[0] × 10 µA). IOUT[3:1] = 100, excitation current = 800 µA + (IOUT[0] × 10 µA). IOUT[3:1] = 101, excitation current = 1 mA + (IOUT[0] × 10 µA). All other values are undefined.
0	IOUT[0]	Set this bit to 1 to enable 10 µA diagnostic current source. Clear this bit to 0 to disable 10 µA diagnostic current source.

EXAMPLE APPLICATION CIRCUITS

Figure 18 shows a simple bridge sensor interface to the ADuC7060/ADuC7061, including the RC filters on the analog input channels. Notice that the sense lines from the bridge (connecting to the reference inputs) are wired separately from the excitation lines (going to DVDD/AVDD and ground). This results in a total of six wires going to the bridge. This 6-wire connection scheme is a feature of most off-the-shelf bridge transducers (such as load cells) that helps to minimize errors that would otherwise result from wire impedances.

In Figure 19, the AD592 is an external temperature sensor used to measure the thermocouple cold junction, and its output is connected to the auxiliary channel. The ADR280 is an external 1.2 V reference part—alternatively, the internal reference can be used. Here, the thermocouple is connected to the primary ADC as a differential input to ADC0/ADC1. Note the resistor between VREF+ and ADC1 to bias the ADC inputs above 100 mV.

Figure 20 shows a simple 4-wire RTD interface circuit. As with the bridge transducer implementation in Figure 18, if a power supply and a serial connection to the outside world are added, Figure 20 represents a complete system.

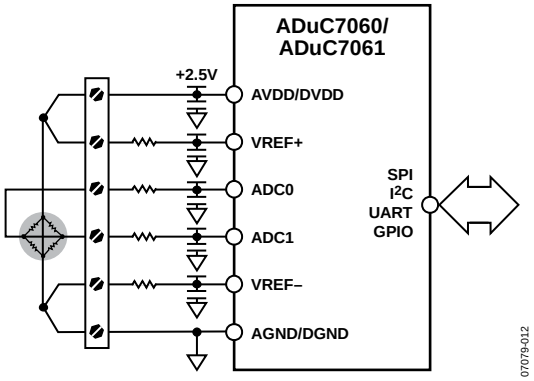

Figure 18. Bridge Interface Circuit

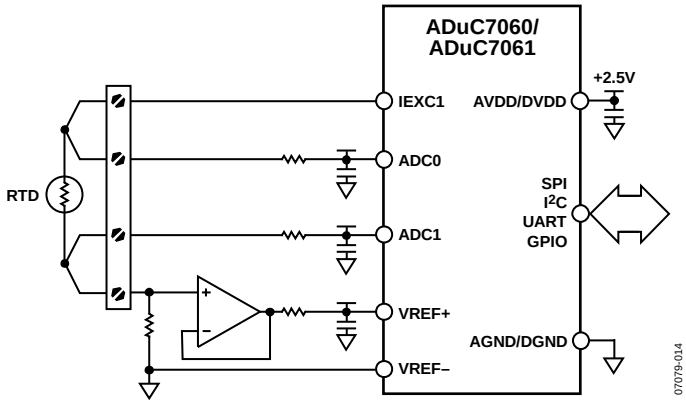

Figure 20. Example of an RTD Interface Circuit

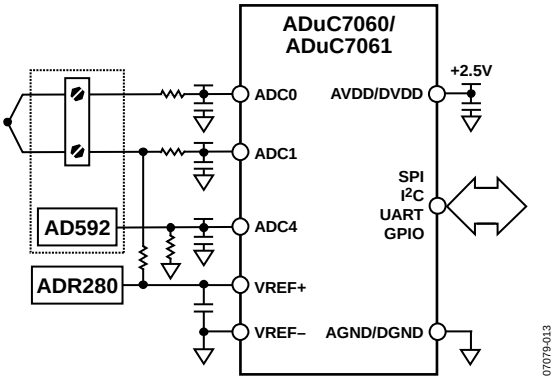

Figure 19. Example of a Thermocouple Interface Circuit

FIQSTA Register

Name: FIQSTA

Address: 0xFFFF0100

Default value: 0x00000000

Access: Read only

PROGRAMMED INTERRUPTS

Because the programmed interrupts are not maskable, they are controlled by another register (SWICFG) that writes into both IRQSTA and IRQSIG registers and/or the FIQSTA and FIQSIG registers at the same time.

SWICFG

SWICFG is a 32-bit register dedicated to software interrupt, described in Table 66. This MMR allows control of a programmed source interrupt.

SWICFG Register

Name: SWICFG

Address: 0xFFFF0010

Default value: 0x00000000

Access: Write only

Table 66. SWICFG MMR Bit Designations

Bit	Description
31:3	Reserved.
2	Programmed interrupt FIQ. Setting/clearing this bit corresponds to setting/clearing Bit 1 of FIQSTA and FIQSIG.
1	Programmed interrupt IRQ. Setting/clearing this bit corresponds to setting/clearing Bit 1 of IRQSTA and IRQSIG.
0	Reserved.

Any interrupt signal must be active for at least the minimum interrupt latency time to be detected by the interrupt controller and to be detected by the user in the IRQSTA/FIQSTA register.

VECTORED INTERRUPT CONTROLLER (VIC)

Each ADuC7060/ADuC7061 incorporates an enhanced interrupt control system or vectored interrupt controller. The vectored interrupt controller for IRQ interrupt sources is enabled by setting Bit 0 of the IRQCONN register. Similarly, Bit 1 of IRQCONN enables the vectored interrupt controller for the FIQ interrupt sources. The vectored interrupt controller provides the following enhancements to the standard IRQ/FIQ interrupts:

- Vectored interrupts—allows a user to define separate interrupt service routine addresses for every interrupt source. This is achieved by using the IRQBASE and IRQVEC registers.
- IRQ/FIQ interrupts—can be nested up to eight levels depending on the priority settings. An FIQ still has a higher priority than an IRQ. Therefore, if the VIC is enabled for both the FIQ and IRQ and prioritization is maximized, it is possible to have 16 separate interrupt levels.
- Programmable interrupt priorities—using the IRQP0 to IRQP2 registers, an interrupt source can be assigned an interrupt priority level value from 0 to 7.

VIC MMRS

IRQBASE

The vector base register, IRQBASE, is used to point to the start address of memory used to store 32 pointer addresses. These pointer addresses are the addresses of the individual interrupt service routines.

IRQBASE Register

Name: IRQBASE

Address: 0xFFFF0014

Default value: 0x00000000

Access: Read and write

Table 67. IRQBASE MMR Bit Designations

Bit	Access	Initial Value	Description
31:16	Read only	Reserved	Always read as 0.
15:0	R/W	0	Vector base address.

IRQVEC

The IRQ interrupt vector register, IRQVEC, points to a memory address containing a pointer to the interrupt service routine of the currently active IRQ. This register should be read only when an IRQ occurs and IRQ interrupt nesting has been enabled by setting Bit 0 of the IRQCONN register.

IRQVEC Register

Name: IRQVEC

Address: 0xFFFF001C

Default value: 0x00000000

Access: Read only

Table 68. IRQVEC MMR Bit Designations

Bit	Access	Initial Value	Description
31:23	Read only	0	Always read as 0.
22:7	Read only	0	IRQBASE register value.
6:2	Read only	0	Highest priority IRQ source. This is a value between 0 to 19 representing the possible interrupt sources. For example, if the highest currently active IRQ is Timer1, then these bits are [01000].
1:0	Reserved	0	Reserved bits.

Priority Registers

The interrupt priority registers, IRQP0, IRQP1, and IRQP2, allow each interrupt source to have its priority level configured for a level between 0 and 7. Level 0 is the highest priority level.

IRQP0 Register

Name: IRQP0

Address: 0xFFFF0020

Default value: 0x00000000

Access: Read and write

Table 69. IRQP0 MMR Bit Designations

Bit	Name	Description
31:27	Reserved	Reserved bits.
26:24	T3PI	A priority level of 0 to 7 can be set for Timer3.
23	Reserved	Reserved bit.
22:20	T2PI	A priority level of 0 to 7 can be set for Timer2.
19	Reserved	Reserved bit.
18:16	T1PI	A priority level of 0 to 7 can be set for Timer1.
15	Reserved	Reserved bit.
14:12	T0PI	A priority level of 0 to 7 can be set for Timer0.
11:7	Reserved	Reserved bits.
6:4	SWINTP	A priority level of 0 to 7 can be set for the software interrupt source.
3:0	Reserved	Interrupt 0 cannot be prioritized.

IRQP1 Register

Name: IRQP1

Address: 0xFFFF0024

Default value: 0x00000000

Access: Read and write

Table 70. IRQP1 MMR Bit Designations

Bit	Name	Description
31	Reserved	Reserved bit.
30:28	I2CMPI	A priority level of 0 to 7 can be set for I^2C master.
27	Reserved	Reserved bit.
26:24	IRQ1PI	A priority level of 0 to 7 can be set for IRQ1.
23	Reserved	Reserved bit.
22:20	IRQ0PI	A priority level of 0 to 7 can be set for IRQ0.
19	Reserved	Reserved bit.
18:16	SPIMPI	A priority level of 0 to 7 can be set for SPI master.
15	Reserved	Reserved bit.
14:12	UARTPI	A priority level of 0 to 7 can be set for UART.
11	Reserved	Reserved bit.
10:8	ADCPI	A priority level of 0 to 7 can be set for the ADC interrupt source.
7:0	Reserved	Reserved bits.

IRQP2 Register

Name: IRQP2

Address: 0xFFFF0028

Default value: 0x00000000

Access: Read and write

Table 71. IRQP2 MMR Bit Designations

Bit	Name	Description
31:15	Reserved	Reserved bit.
14:12	IRQ3PI	A priority level of 0 to 7 can be set for IRQ3.
11	Reserved	Reserved bit.
10:8	IRQ2PI	A priority level of 0 to 7 can be set for IRQ2.
7	Reserved	Reserved bit.
6:4	SPISPI	A priority level of 0 to 7 can be set for SPI slave.
3	Reserved	Reserved bit.
2:0	I2CSPI	A priority level of 0 to 7 can be set for I^2C slave.

IRQCLRE Register

Name: IRQCLRE

Address: 0xFFFF0038

Default value: 0x00000000

Access: Read and write

Table 77. IRQCLRE MMR Bit Designations

Bit	Name	Description
31:20	Reserved	These bits are reserved and should not be written to.
19	IRQ3CLRI	A 1 must be written to this bit in the IRQ3 interrupt service routine to clear an edge triggered IRQ3 interrupt.
18	IRQ2CLRI	A 1 must be written to this bit in the IRQ2 interrupt service routine to clear an edge triggered IRQ2 interrupt.
17:15	Reserved	These bits are reserved and should not be written to.
14	IRQ1CLRI	A 1 must be written to this bit in the IRQ1 interrupt service routine to clear an edge triggered IRQ1 interrupt.
13	IRQ0CLRI	A 1 must be written to this bit in the IRQ0 interrupt service routine to clear an edge triggered IRQ0 interrupt.
12:0	Reserved	These bits are reserved and should not be written to.

UART SERIAL INTERFACE

Each ADuC7060/ADuC7061 features a 16450-compatible UART. The UART is a full-duplex, universal, asynchronous receiver/transmitter. A UART performs serial-to-parallel conversion on data characters received from a peripheral device and parallel-to-serial conversion on data characters received from the ARM7TDMI. The UART features a fractional divider that facilitates high accuracy baud rate generation and a network addressable mode. The UART functionality is available on the P1.0/IRQ1/SIN/T0 and P1.1/SOUT pins of the ADuC7060/ADuC7061.

The serial communication adopts an asynchronous protocol that supports various word lengths, stop bits, and parity generation options selectable in the configuration register.

BAUD RATE GENERATION

The ADuC7060/ADuC7061 features two methods of generating the UART baud rate: normal 450 UART baud rate generation and ADuC7060/ADuC7061 fractional divider.

Normal 450 UART Baud Rate Generation

The baud rate is a divided version of the core clock using the value in COMDIV0 and COMDIV1 MMRs (16-bit value, divisor latch (DL)). The standard baud rate generator formula is

$$Baud\ Rate = \frac{10.24\ \text{MHz}}{16 \times 2 \times DL} \quad (1)$$

Table 88 lists common baud rate values.

Table 88. Baud Rate Using the Standard Baud Rate Generator

Baud Rate	DL	Actual Baud Rate	% Error
9600	0x21	9696	1.01%
19,200	0x11	18,824	1.96%
115,200	0x3	106,667	7.41%

ADuC7060/ADuC7061 Fractional Divider

The fractional divider combined with the normal baud rate generator allows the generation of accurate high speed baud rates.

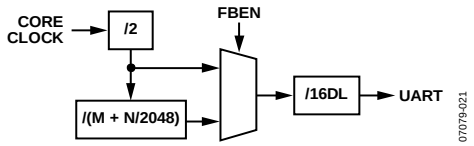

Figure 27. Fractional Divider Baud Rate Generation

Calculation of the baud rate using a fractional divider is as follows:

$$Baud\ Rate = \frac{10.24\ \text{MHz}}{16 \times DL \times 2 \times (M + \frac{N}{2048})} \quad (2)$$

$$M + \frac{N}{2048} = \frac{10.24\ \text{MHz}}{Baud\ Rate \times 16 \times DL \times 2}$$

Table 89 lists common baud rate values.

Table 89. Baud Rate Using the Fractional Baud Rate Generator

Baud Rate	DL	M	N	Actual Baud Rate	% Error
9600	0x21	1	21	9598.55	0.015%
19,200	0x10	1	85	19,203	0.015%
115,200	0x2	1	796	115,218	0.015%

UART REGISTER DEFINITIONS

The UART interface consists of the following 11 registers:

COMTX: 8-bit transmit register
COMRX: 8-bit receive register
COMDIV0: divisor latch (low byte)
COMDIV1: divisor latch (high byte)
COMCON0: line control register
COMCON1: line control register
COMSTA0: line status register
COMSTA1: line status register
COMIEN0: interrupt enable register
COMIID0: interrupt identification register
COMDIV2: 16-bit fractional baud divide register

COMTX, COMRX, and COMDIV0 share the same address location. COMTX and COMRX can be accessed when Bit 7 in the COMCON0 register is cleared. COMDIV0 or COMDIV1 can be accessed when Bit 7 of COMCON0 or COMCON1, respectively, is set.

UART Status Register 1

COMSTA1 Register

Name: COMSTA1

Address: 0xFFFF0718

Default value: 0x00

Access: Read only

Function: COMSTA1 is a modem status register.

Table 93. COMSTA1 MMR Bit Designations

Bit	Name	Description
7:5		Reserved. Not used.
4	CTS	Clear to send.
3:1		Reserved. Not used.
0	DCTS	Delta CTS. Set automatically if CTS changed state since COMSTA1 was last read. Cleared automatically by reading COMSTA1.

UART Interrupt Enable Register 0

COMIEN0 Register

Name: COMIEN0

Address: 0xFFFF0704

Default value: 0x00

Access: Read and write

Function: This 8-bit register enables and disables the individual UART interrupt sources.

Table 94. COMIEN0 MMR Bit Designations

Bit	Name	Description
7:4		Reserved. Not used.
3	EDSSI	Modem status interrupt enable bit. Set by user to enable generation of an interrupt if COMSTA1[4] or COMSTA1[0] are set. Cleared by user.
2	ELSI	Receive status interrupt enable bit. Set by user to enable generation of an interrupt if any of the COMSTA0[3:1] register bits are set. Cleared by user.
1	ETBEI	Enable transmit buffer empty interrupt. Set by user to enable an interrupt when the buffer is empty during a transmission; that is, when COMSTA0[5] is set. Cleared by user.
0	ERBFI	Enable receive buffer full interrupt. Set by user to enable an interrupt when the buffer is full during a reception. Cleared by user.

UART Interrupt Identification Register 0

COMIID0 Register

Name: COMIID0

Address: 0xFFFF0708

Default value: 0x01

Access: Read only

Function: This 8-bit register reflects the source of the UART interrupt.

I²C Address 1, I2CADR1, Register

Name: I2CADR1

Address: 0xFFFF091C

Default value: 0x00

Access: Read and write

Function: This 8-bit MMR is used in 10-bit addressing mode only. This register contains the least significant byte of the address.

Table 102. I2CADR1 MMR in 10-Bit Address Mode

Bit	Name	Description
7:0	I2CLADR	These bits contain ADDR[7:0] in 10-bit addressing mode.

I²C Master Clock Control, I2CDIV, Register

Name: I2CDIV

Address: 0xFFFF0924

Default value: 0x1F1F

Access: Read and write

Function: This MMR controls the frequency of the I²C clock generated by the master on to the SCL pin. For further details, see the Serial Clock Generation section.

Table 103. I2CDIV MMR Bit Designations

Bit	Name	Description
15:8	DIVH	These bits control the duration of the high period of SCL.
7:0	DIVL	These bits control the duration of the low period of SCL.

I²C Slave Registers

I²C Slave Control, I2CSCON, Register

Name: I2CSCON

Address: 0xFFFF0928

Default value: 0x0000

Access: Read and write

Function: This 16-bit MMR configures the I²C peripheral in slave mode.