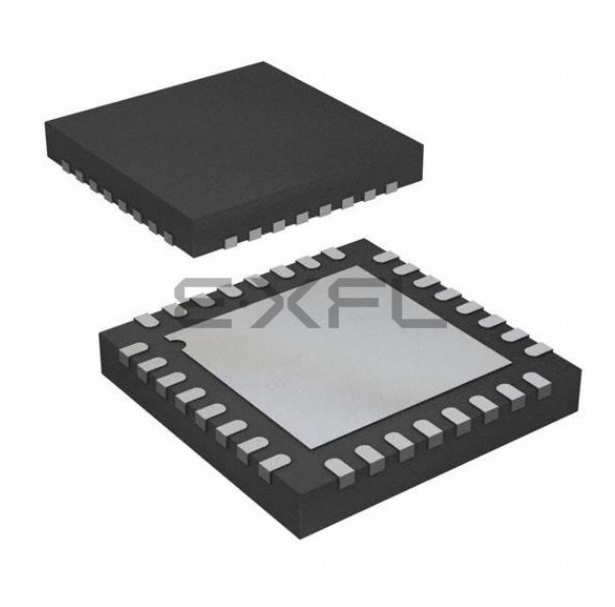

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	10MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	POR, PWM, Temp Sensor, WDT
Number of I/O	8
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 32
Voltage - Supply (Vcc/Vdd)	2.375V ~ 2.625V
Data Converters	A/D 5x24b, 8x24b; D/A 1x14b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VFQFN Exposed Pad, CSP
Supplier Device Package	32-LFCSP-VQ (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/aduc7061bcpz32

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TIMING SPECIFICATIONS

I²C Timing

Table 2. I²C® Timing in Standard Mode (100 kHz)

Parameter	Description	Slave		Unit
		Min	Max	
t_L	SCLOCK low pulse width	4.7		µs
t_H	SCLOCK high pulse width	4.0		ns
t_{SHD}	Start condition hold time	4.0		µs
t_{DSU}	Data setup time	250		ns
t_{DHD}	Data hold time	0	3.45	µs
t_{RSU}	Setup time for repeated start	4.7		µs
t_{PSU}	Stop condition setup time	4.0		µs
t_{BUF}	Bus-free time between a stop condition and a start condition	4.7		µs
t_R	Rise time for both CLOCK and SDATA		1	µs
t_F	Fall time for both CLOCK and SDATA		300	ns

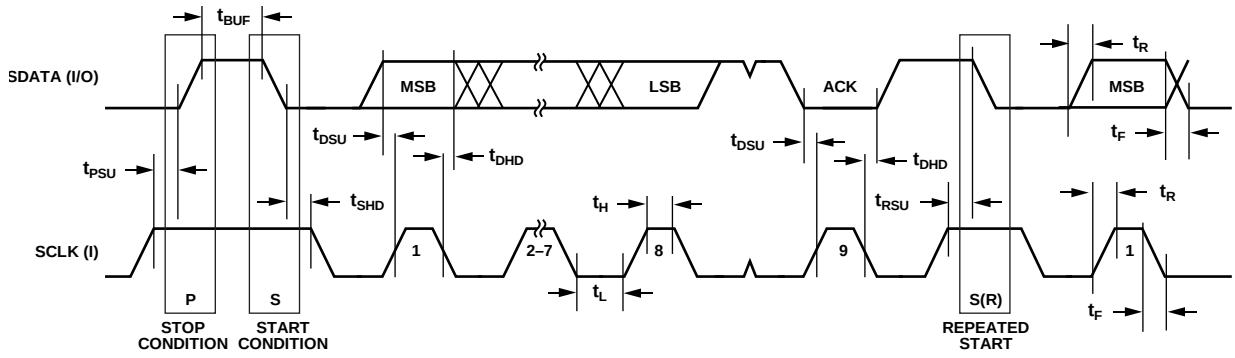

Figure 2. I²C Compatible Interface Timing

Pin No.	Mnemonic	Type[1]	Description
43	DGND	S	Digital Ground.
44	DVDD	S	Digital Supply Pin.
45	NTRST/$\overline{BM}$	I	JTAG Reset/Boot Mode. Input pin used for debug and download only and boot mode ($\overline{BM}$). The ADuC7060 enters serial download mode if $\overline{BM}$ is low at reset and executes code if $\overline{BM}$ is pulled high at reset through a 13 kΩ resistor.
46	TDO	O	JTAG Data Out. Output pin used for debug and download only.
47	TDI	I	JTAG Data In. Input pin used for debug and download only. Add an external pull-up resistor (~100 kΩ) to this pin.
48	TCK	I	JTAG Clock Pin. Input pin used for debug and download only. Add an external pull-up resistor (~100 kΩ) to this pin.

[1] I = input, O = output, I/O = input/output, and S = supply.

Table 36. Primary ADC—Typical Output RMS Noise in Normal Mode (μV)[1]

ADC Register Status	Data Update Rate	Selectable Input Range (PGA Settings)									
		±1.2 V (PGA = 1)	±600 mV (PGA = 2)	±300 mV (PGA = 4)	±150 mV (PGA = 8)	±75 mV (PGA = 16)	±37.5 mV (PGA = 32)	±18.75 mV (PGA = 64)	±9.375 mV (PGA = 128)	±4.68 mV (PGA = 256)	±2.34 mV (PGA = 512)
Chop On	4 Hz	0.62 μV	0.648 μV	0.175 μV	0.109 μV	0.077 μV	0.041 μV	0.032 μV	0.0338 μV	0.032 μV	0.033 μV
Chop Off	50 Hz	1.97 μV	1.89 μV	0.570 μV	0.38 μV	0.27 μV	0.147 μV	0.123 μV	0.12 μV	0.098 μV	0.098 μV
Chop Off	1 kHz	8.54 μV	8.4 μV	2.55 μV	1.6 μV	1.17 μV	0.658 μV	0.53 μV	0.55 μV	0.56 μV	0.52 μV
Chop Off	8 kHz	54.97 μV	55.54 μV	14.30 μV	7.88 μV	4.59 μV	2.5 μV	1.71 μV	1.75 μV	0.915 μV	0.909 μV

[1] The input voltage range is centered around the common-mode voltage and should meet the input voltage range specified in the Electrical Specifications section.

Table 37. Primary ADC—Typical Output RMS Effective Number of Bits in Normal Mode (Peak-to-Peak Bits in Parentheses)

ADC Register Status	Data Update Rate	Input Voltage Noise (mV)									
		±1.2 V (PGA = 1)	±600 mV (PGA = 2)	±300 mV (PGA = 4)	±150 mV (PGA = 8)	±75 mV (PGA = 16)	±37.5 mV (PGA = 32)	±18.75 mV (PGA = 64)	±9.375 mV (PGA = 128)	±4.68 mV (PGA = 256)	±2.34 mV (PGA = 512)
Chop On	4 Hz	21.9 (19.1 p-p)	20.8 (18.1 p-p)	21.7 (19.0 p-p)	21.4 (18.7 p-p)	20.9 (18.2 p-p)	20.8 (18.1 p-p)	20.2 (17.4 p-p)	19.1 (16.4 p-p)	18.2 (15.4 p-p)	17.1 (14.4 p-p)
Chop Off	50 Hz	20.2 (17.5 p-p)	19.3 (16.6 p-p)	20.0 (17.3 p-p)	19.6 (16.9 p-p)	19.1 (16.4 p-p)	19.0 (16.2 p-p)	18.2 (15.5 p-p)	17.3 (14.6 p-p)	16.6 (13.8 p-p)	15.5 (12.8 p-p)
Chop Off	1 kHz	18.1 (15.3 p-p)	17.1 (14.4 p-p)	17.8 (15.1 p-p)	17.5 (14.8 p-p)	17.0 (14.2 p-p)	16.8 (14.1 p-p)	16.1 (13.4 p-p)	15.1 (12.3 p-p)	14.0 (11.3 p-p)	13.1 (10.4 p-p)
Chop Off	8 kHz	15.4 (12.7 p-p)	14.4 (11.7 p-p)	15.4 (12.6 p-p)	15.2 (12.5 p-p)	15.0 (12.3 p-p)	14.9 (12.2 p-p)	14.4 (11.7 p-p)	13.4 (10.7 p-p)	13.3 (10.6 p-p)	12.3 (9.6 p-p)

Table 38. Auxilary ADC—Typical Output RMS Noise

ADC Register	Data Update Rate	RMS Value
Chop On	4 Hz	0.633 μV
Chop On	10 Hz	0.810 μV
Chop Off	1 kHz	7.4 μV
Chop Off	8 kHz	54.18 μV

REFERENCE SOURCES

Both the primary and auxiliary ADCs have the option of using the internal reference voltage or one of two external differential reference sources. The first external reference is applied to the VREF+/VREF− pins. The second external reference is applied to the ADC4/EXT_REF2IN+ and ADC5/EXT_REF2IN− pins. By default, each ADC uses the internal 1.2 V reference source.

For details on how to configure the external reference source for the primary ADC, see the description of the ADC0REF[1:0] bits in the ADC0 control register, ADC0CON.

For details on how to configure the external reference source for the auxiliary ADC, see the description of the ADC1REF[2:0] bits in the ADC1 control register, ADC1CON.

If an external reference source of greater than 1.35 V is needed for ADC0, the HIGHEXTREF0 bit must be set in ADC0CON.

Similarly, if an external reference source of greater than 1.35 V is used for ADC1, the HIGHEXTREF1 bit must be set in ADC1CON.

DIAGNOSTIC CURRENT SOURCES

To detect a connection failure to an external sensor, the ADuC7060/ADuC7061 incorporates a 50 μA constant current source on the selected analog input channels to both the primary and auxiliary ADCs.

The diagnostic current sources for the primary ADC analog inputs are controlled by the ADC0DIAG[1:0] bits in the ADC0CON register.

Similarly, the diagnostic current sources for the auxiliary ADC analog inputs are controlled by the ADC1DIAG[1:0] bits in the ADC1CON register.

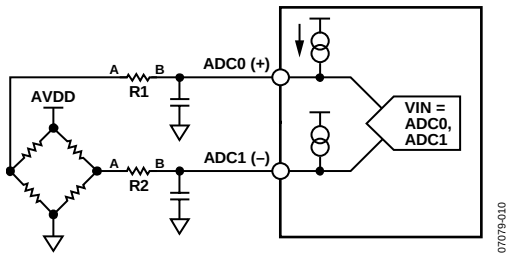

Figure 15. Example Circuit Using Diagnostic Current Sources

ADC COMPARATOR AND ACCUMULATOR

Every primary ADC result can be compared to a preset threshold level (ADC0TH) as configured via ADCCFG[4:3]. An MCU interrupt is generated if the absolute (sign independent) value of the ADC result is greater than the preprogrammed comparator threshold level. An extended function of this comparator function allows user code to configure a threshold counter (ADC0THV) to monitor the number of primary ADC results that have occurred above or below the preset threshold level. Again, an ADC interrupt is generated when the threshold counter reaches a preset value (ADC0RCR).

Finally, a 32-bit accumulator (ADC0ACC) function can be configured (ADCCFG[6:5]) allowing the primary ADC to add (or subtract) multiple primary ADC sample results. User code can read the accumulated value directly (ADC0ACC) without any further software processing.

TEMPERATURE SENSOR

The ADuC7060/ADuC7061 provides a voltage output from an on-chip band gap reference proportional to absolute temperature. This voltage output can also be routed through the front-end auxiliary ADC multiplexer (effectively, an additional ADC channel input), facilitating an internal temperature sensor channel that measures die temperature.

The internal temperature sensor is not designed for use as an absolute ambient temperature calculator. It is intended for use as an approximate indicator of the temperature of the ADuC7060/ADuC7061 die.

The typical temperature coefficient is 0.28 mV/°C.

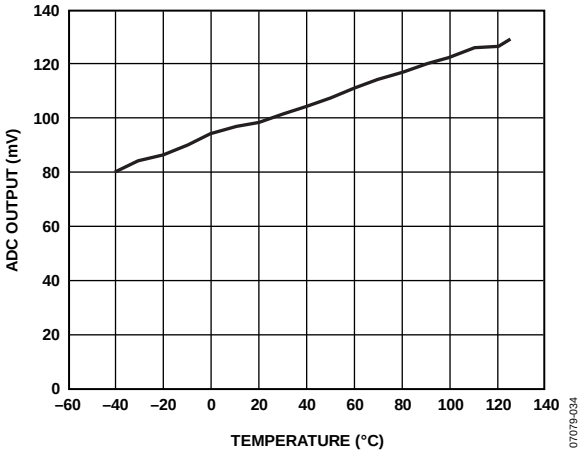

Figure 16. ADC Output vs. Temperature

ADC MMR INTERFACE

The ADCs are controlled and configured through a number of MMRs that are described in detail in the following sections.

In response to an ADC interrupt, user code should interrogate the ADCSTA MMR to determine the source of the interrupt. Each ADC interrupt source can be individually masked via the ADCMSKI MMR described in Table 41.

All primary ADC result ready bits are cleared by a read of the ADC0DAT MMR. If the primary channel ADC is not enabled, all ADC result ready bits are cleared by a read of the ADC1DAT MMR. To ensure that primary ADC and auxiliary ADC conversion data are synchronous, user code should first read the ADC1DAT MMR and then the ADC0DAT MMR. New ADC conversion results are not written to the ADCxDAT MMRs unless the respective ADC result ready bits are first cleared. The only exception to this rule is the data conversion result updates when the ARM core is powered down. In this mode, ADCxDAT registers always contain the most recent ADC conversion result even though the ready bits are not cleared.

ADC Status Register

Name: ADCSTA

Address: 0xFFFF0500

Default value: 0x0000

Access: Read only

Function: This read-only register holds general status information related to the mode of operation or current status of the ADuC7060/ADuC7061 ADCs.

ADC Interrupt Mask Register

Name: ADCMSKI

Address: 0xFFFF0504

Default value: 0x0000

Access: Read and write

Function: This register allows the ADC interrupt sources to be enabled individually. The bit positions in this register are the same as the lower eight bits in the ADCSTA MMR. If a bit is set by user code to 1, the respective interrupt is enabled. By default, all bits are 0, meaning all ADC interrupt sources are disabled.

Table 41. ADCMSKI MMR Bit Designations

Bit	Name	Description
7		Not used. This bit is reserved for future functionality and should not be monitored by user code.
6	ADC0ATHEX_INTEN	ADC0 accumulator comparator threshold exceeded interrupt enable bit. When set to 1, this bit enables an interrupt when the ADC0ATHEX bit in the ADCSTA register is set. When this bit is cleared, this interrupt source is disabled.
5		Not used. This bit is reserved for future functionality and should not be monitored by user code.
4	ADC0THEX_INTEN	Primary channel ADC comparator threshold exceeded interrupt enable bit. When set to 1, this bit enables an interrupt when the ADC0THEX bit in the ADCSTA register is set. When this bit is cleared, this interrupt source is disabled.
3	ADC0OVR_INTEN	When set to 1, this bit enables an interrupt when the ADC0OVR bit in the ADCSTA register is set. When this bit is cleared, this interrupt source is disabled.
2		Not used. This bit is reserved for future functionality and should not be monitored by user code.
1	ADC1RDY_INTEN	Auxiliary ADC result ready bit. When set to 1, this bit enables an interrupt when the ADC1RDY bit in the ADCSTA register is set. When this bit is cleared, this interrupt source is disabled.
0	ADC0RDY_INTEN	Primary ADC result ready bit. When set to 1, this bit enables an interrupt when the ADC0RDY bit in the ADCSTA register is set. When this bit is cleared, this interrupt source is disabled.

ADC Mode Register

Name: ADCMDE

Address: 0xFFFF0508

Default value: 0x03

Access: Read and write

Function: The ADC mode MMR is an 8-bit register that configures the mode of operation of the ADC subsystem.

Table 42. ADCMDE MMR Bit Designations

Bit	Name	Description
7	ADCCLKSEL	Set this bit to 1 to enable ADCCLK = 512 kHz. This bit should be set for normal ADC operation. Clear this bit to enable ADCCLK = 131 kHz. This bit should be cleared for low power ADC operation.
6		Not used. This bit is reserved for future functionality and should not be monitored by user code.
5	ADCLPMEN	Enable low power mode. This bit has no effect if ADCMDE[4:3] = 00 (ADC is in normal mode). This bit must be set to 1 in low power mode. Clearing this bit in low power mode results in erratic ADC results.

Auxiliary ADC Control Register

Name: ADC1CON

Address: 0xFFFF0510

Default value: 0x0000

Access: Read and write

Function: The auxiliary ADC control MMR is a 16-bit register.

Table 44. ADC1CON MMR Bit Designations

Bit	Name	Description
15	ADC1EN	Auxiliary channel ADC enable. This bit is set to 1 by user code to enable the auxiliary ADC. Clearing this bit to 0 powers down the auxiliary ADC.
14:13	ADC1DIAG[1:0]	Diagnostic current source enable bits. This is the same current source as that used on ADC0DIAG[1:0]. The ADCs cannot enable the diagnostic current sources at the same time. [00]= current sources off. [01] = enables a 50 µA current source on selected positive input (for example, ADC2). [10] = enables a 50 µ A current source on selected negative input (for example, ADC3). [11] = enables a 50 µ A current source on both selected inputs (for example, ADC2 and ADC3).
12	HIGHEXTREF1	This bit must be set high if the external reference for ADC1 exceeds 1.35 V. This results in the reference source being divided by 2. Clear this bit when using the internal reference or an external reference of less than 1.35 V.
11	ADC1CODE	Auxiliary channel ADC output coding. This bit is set to 1 by user code to configure auxiliary ADC output coding as unipolar. This bit is cleared to 0 by user code to configure auxiliary ADC output coding as twos complement.
10:7	ADC1CH[3:0]	Auxiliary channel ADC input select. Note: Single-ended channels are selected with respect to ADC5. Bias ADC5 to a minimum level of 0.1 V. [0000] = ADC2/ADC3 (differential mode). [0001] = ADC4/ADC5 (differential mode). [0010] = ADC6/ADC7 (differential mode). [0011] = ADC8/ADC9 (differential mode). [0100] = ADC2/ADC5 (single-ended mode). [0101] = ADC3/ADC5 (single-ended mode). [0110] = ADC4/ADC5 (single-ended mode). [0111] = ADC6/ADC5 (single-ended mode). [1000] = ADC7/ADC5 (single-ended mode). [1001] = ADC8/ADC5 (single-ended mode). [1010] = ADC9/ADC5 (single-ended mode). [1011] = internal temperature sensor+/internal temperature sensor−. [1100] = VREF+, VREF−. Note: This is the reference selected by the ADC1REF bits. [1101] = DAC_OUT/AGND. [1110] = undefined. [1111] = internal short to ADC3.

ADC Configuration Register

Name: ADCCFG

Address: 0xFFFF0518

Default value: 0x00

Access: Read and write

Function: The 8-bit ADC configuration MMR controls extended functionality related to the on-chip ADCs.

Table 48. ADCCFG MMR Bit Designations

Bit	Name	Description
7	GNDSW_EN	Analog ground switch enable. This bit is set to 1 by user software to connect the external GND_SW pin to an internal analog ground reference point. This bit can be used to connect and disconnect external circuits and components to ground under program control and thereby minimize dc current consumption when the external circuit or component is not being used. This bit is used in conjunction with ADCCFG[1] to select a 20 kΩ resistor to ground. When this bit is cleared, the analog ground switch is disconnected from the external pin.
6:5	ADC0ACCEN[1:0]	Primary channel (32-bit) accumulator enable. [00] = accumulator disabled and reset to 0. The accumulator must be disabled for a full ADC conversion (ADCSTA[0] set twice) before the accumulator can be re-enabled to ensure that the accumulator is reset. [01] = accumulator active. Positive current values are added to the accumulator total; the accumulator can overflow if allowed to run for >65,535 conversions. Negative current values are subtracted from the accumulator total; the accumulator is clamped to a minimum value of 0. [10] = accumulator active. Same as [01] except that there is no clamp. Positive current values are added to the accumulator total; the accumulator can overflow if allowed to run for >65,535 conversions. The absolute values of negative current are subtracted from the accumulator total; the accumulator in this mode continues to accumulate negatively, below 0. [11] = accumulator and comparator active. This causes an ADC0 interrupt if ADCMSKI[6] is set.
4:3	ADC0CMPEN[1:0]	Primary ADC comparator enable bits. [00] = comparator disabled. [01] = comparator active. Interrupt asserted if absolute value of ADC0 conversion result |I| ≥ ADC0TH. [10] = comparator count mode active. Interrupt asserted if absolute value of ADC0 conversion result |I| ≥ ADC0TH for the number of ADC0THC conversions. A conversion value |I| < ADC0TH resets the threshold counter value (ADC0THV) to 0. [11] = comparator count mode active, interrupt asserted if absolute value of ADC0 conversion result |I| ≥ ADC0TH for the number of ADC0THC conversions. A conversion value |I| < ADC0TH decrements the threshold counter value (ADC0THV) toward 0.
2	ADC0OREN	ADC0 overrange enable. Set by the user to enable a coarse comparator on the primary channel ADC. If the reading is grossly (>30% approximate) overrange for the active gain setting, the overrange bit in the ADCSTA MMR is set. The ADC reading must be outside this range for greater than 125 µs for the flag to be set. Do not use this feature in ADC low power mode.
1	GNDSW_RES_EN	Set to 1 to enable a 20 kΩ resistor in series with the ground switch. Clear this bit to disable this resistor.
0	ADCRCEN	ADC result counter enable. Set by user to enable the result count mode. ADC interrupts occur if ADC0RCR = ADC0RCV. Cleared to disable the result counter. ADC interrupts occur after every conversion.

IRQCONN

The IRQCONN register is the IRQ and FIQ control register. It contains two active bits: the first to enable nesting and prioritization of IRQ interrupts, and the other to enable nesting and prioritization of FIQ interrupts.

If these bits are cleared, FIQs and IRQs can still be used, but it is not possible to nest IRQs or FIQs. Neither is it possible to set an interrupt source priority level. In this default state, an FIQ does have a higher priority than an IRQ.

IRQCONN Register

Name: IRQCONN

Address: 0xFFFF0030

Default value: 0x00000000

Access: Read and write

Table 72. IRQCONN MMR Bit Designations

Bit	Name	Description
31:2	Reserved	These bits are reserved and should not be written to.
1	ENFIQN	Setting this bit to 1 enables nesting of FIQ interrupts. Clearing this bit means no nesting or prioritization of FIQs is allowed.
0	ENIRQN	Setting this bit to 1 enables nesting of IRQ interrupts. Clearing this bit means no nesting or prioritization of IRQs is allowed.

IRQSTAN

If IRQCONN[0] is asserted and IRQVEC is read, then one of these bits is asserted. The bit that asserts depends on the priority of the IRQ. If the IRQ is of Priority 0, then Bit 0 asserts; Priority 1, then Bit 1 asserts; and so forth. When a bit is set in this register, all interrupts of that priority and lower are blocked.

To clear a bit in this register, all bits of a higher priority must be cleared first. It is possible to clear only one bit at a time. For example, if this register is set to 0x09, writing 0xFF changes the register to 0x08, and writing 0xFF a second time changes the register to 0x00.

IRQSTAN Register

Name: IRQSTAN

Address: 0xFFFF003C

Default value: 0x00000000

Access: Read and write

Table 73. IRQSTAN MMR Bit Designations

Bit	Name	Description
31:8	Reserved	These bits are reserved and should not be written to.
7:0		Setting this bit to 1 enables nesting of FIQ interrupts. Clearing this bit means no nesting or prioritization of FIQs is allowed.

FIQVEC

The FIQ interrupt vector register, FIQVEC, points to a memory address containing a pointer to the interrupt service routine of the currently active FIQ. This register should be read only when an FIQ occurs and FIQ interrupt nesting has been enabled by setting Bit 1 of the IRQCONN register.

FIQVEC Register

Name: FIQVEC

Address: 0xFFFF011C

Default value: 0x00000000

Access: Read only

Table 74. FIQVEC MMR Bit Designations

Bit	Access	Initial Value	Description
31:23	Read only	0	Always read as 0.
22:7	Read only	0	IRQBASE register value.
6:2		0	Highest priority FIQ source. This is a value between 0 to 19 that represents the possible interrupt sources. For example, if the highest currently active FIQ is Timer1, then these bits are [01000].
1:0	Reserved	0	Reserved bits.

FIQSTAN

If IRQCONN[1] is asserted and FIQVEC is read, then one of these bits asserts. The bit that asserts depends on the priority of the FIQ. If the FIQ is of Priority 0, Bit 0 asserts; Priority 1, Bit 1 asserts; and so forth.

When a bit is set in this register, all interrupts of that priority and lower are blocked.

To clear a bit in this register, all bits of a higher priority must be cleared first. It is possible to clear only one bit as a time. For example, if this register is set to 0x09, writing 0xFF changes the register to 0x08, and writing 0xFF a second time changes the register to 0x00.

FIQSTAN Register

Name: FIQSTAN

Address: 0xFFFF013C

Default value: 0x00000000

Access: Read and write

Table 75. FIQSTAN MMR Bit Designations

Bit	Name	Description
31:8	Reserved	These bits are reserved and should not be written to.
7:0		Setting this bit to 1 enables nesting of FIQ interrupts. Clearing this bit means no nesting or prioritization of FIQs is allowed.

External Interrupts (IRQ0 to IRQ3)

The ADuC7060/ADuC7061 provides up to four external interrupt sources. These external interrupts can be individually configured as level triggered or rising/falling edge triggered.

To enable the external interrupt source, the appropriate bit must first be set in the FIQEN or IRQEN register. To select the required edge or level to trigger on, the IRQCONE register must be appropriately configured.

To properly clear an edge based external IRQ interrupt, set the appropriate bit in the IRQCLRE register.

IRQCONE Register

Name: IRQCONE

Address: 0xFFFF0034

Default value: 0x00000000

Access: Read and write

Table 76. IRQCONE MMR Bit Designations

Bit	Name	Description
31:8	Reserved	These bits are reserved and should not be written to.
7:6	IRQ3SRC[1:0]	[11] = External IRQ3 triggers on falling edge. [10] = External IRQ3 triggers on rising edge. [01] = External IRQ3 triggers on low level. [00] = External IRQ3 triggers on high level.
5:4	IRQ2SRC[1:0]	[11] = External IRQ2 triggers on falling edge. [10] = External IRQ2 triggers on rising edge. [01] = External IRQ2 triggers on low level. [00] = External IRQ2 triggers on high level.
3:2	IRQ1SRC[1:0]	[11] = External IRQ1 triggers on falling edge. [10] = External IRQ1 triggers on rising edge. [01] = External IRQ1 triggers on low level. [00] = External IRQ1 triggers on high level.
1:0	IRQ0SRC[1:0]	[11] = External IRQ0 triggers on falling edge. [10] = External IRQ0 triggers on rising edge. [01] = External IRQ0 triggers on low level. [00] = External IRQ0 triggers on high level.

TIMER0

Timer0 is a 32-bit, general-purpose timer, count down or count up, with a programmable prescaler. The prescaler source can be the low power 32.768 kHz oscillator, the core clock, or from one of two external GPIOs. This source can be scaled by a factor of 1, 16, 256, or 32,768. This gives a minimum resolution of 97.66 ns with a prescaler of 1 (ignoring the external GPIOs).

The counter can be formatted as a standard 32-bit value or as hours:minutes:seconds:hundredths.

Timer0 has a capture register (T0CAP) that is triggered by a selected IRQ source initial assertion. When triggered, the current timer value is copied to T0CAP, and the timer continues to run. Use this feature to determine the assertion of an event with increased accuracy. Note that only peripherals that have their IRQ source enabled can be used with the timer capture feature.

The Timer0 interface consists of five MMRS: T0LD, T0VAL, T0CAP, T0CLRI, and T0CON.

- T0LD, T0VAL, and T0CAP are 32-bit registers and hold 32-bit, unsigned integers of which T0VAL and T0CAP are read only.
- T0CLRI is an 8-bit register and writing any value to this register clears the Timer0 interrupt.
- T0CON is the configuration MMR, which is described in Table 80.

Timer0 features a postscaler that allows the user to count between 1 and 256 the number of Timer0 timeouts. To activate the postscaler, the user sets Bit 18 and writes the desired number to count into Bits[24:31] of T0CON. When that number of timeouts is reached, Timer0 can generate an interrupt if T0CON[18] is set.

Note that, if the part is in a low power mode and Timer0 is clocked from the GPIO or low power oscillator source, Timer0 continues to operate.

Timer0 reloads the value from T0LD when Timer0 overflows.

Timer0 Load Registers

Name: T0LD

Address: 0xFFFF0320

Default value: 0x00000000

Access: Read and write

Function: T0LD is a 32-bit register that holds the 32-bit value that is loaded into the counter.

Timer0 Clear Register

Name: T0CLRI

Address: 0xFFFF032C

Access: Write only

Function: This 8-bit, write-only MMR is written (with any value) by user code to clear the interrupt.

Timer0 Value Register

Name: T0VAL

Address: 0xFFFF0324

Default value: 0xFFFFFFFF

Access: Read only

Function: T0VAL is a 32-bit register that holds the current value of Timer0.

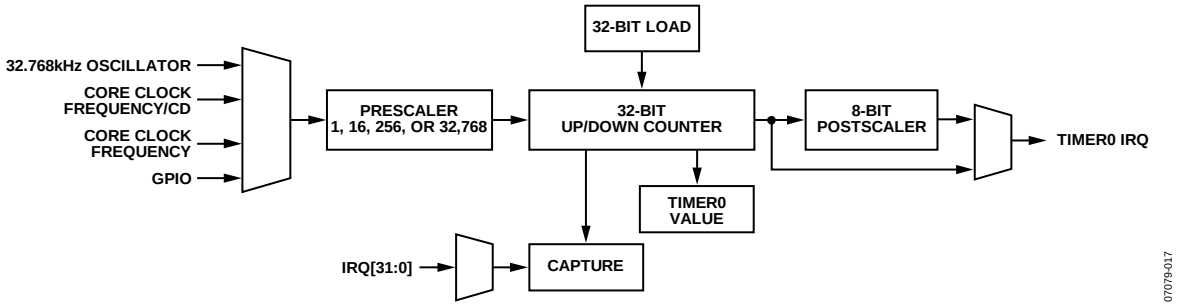

Figure 23. Timer0 Block Diagram

Bit	Name	Description
5:4	T0FORMAT	Format. [00] = binary (default). [01] = reserved. [10] = hours:minutes:seconds:hundredths (23 hours to 0 hours). [11] = hours:minutes:seconds:hundredths (255 hours to 0 hours).
3:0	T0SCALE	Prescaler. [0000] = source clock/1 (default). [0100] = source clock/16. [1000] = source clock/256. [1111] = source clock/32,768. Note that all other values are undefined.

TIMER1 OR WAKE-UP TIMER

Timer1 is a 32-bit wake-up timer, count down or count up, with a programmable prescaler. The prescaler is clocked directly from one of four clock sources, namely, the core clock (which is the default selection), external 32.768 kHz watch crystal, or the 32.768 kHz oscillator. The selected clock source can be scaled by a factor of 1, 16, 256, or 32,768. The wake-up timer continues to run when the core clock is disabled. This gives a minimum resolution of 97.66 ns when operating at CD zero, the core is operating at 10.24 MHz, and with a prescaler of 1 (ignoring the external GPIOs).

The counter can be formatted as a plain 32-bit value or as hours:minutes:seconds:hundredths.

Timer1 reloads the value from T1LD either when Timer1 overflows or immediately when T1LD is written.

The Timer1 interface consists of four MMRS.

- T1LD and T1VAL are 32-bit registers and hold 32-bit, unsigned integers. T1VAL is read only.
- T1CLRI is an 8-bit register. Writing any value to this register clears the Timer1 interrupt.
- T1CON is the configuration MMR, described in Table 81.

Timer1 Load Registers

Name: T1LD

Address: 0xFFFF0340

Default value: 0x00000000

Access: Read and write

Function: T1LD is a 32-bit register that holds the 32-bit value that is loaded into the counter.

Timer1 Clear Register

Name: T1CLRI

Address: 0xFFFF034C

Access: Write only

Function: This 8-bit, write-only MMR is written (with any value) by user code to clear the interrupt.

Timer1 Value Register

Name: T1VAL

Address: 0xFFFF0344

Default value: 0xFFFFFFFF

Access: Read only

Function: T1VAL is a 32-bit register that holds the current value of Timer1.

Figure 24. Timer1 Block Diagram

Timer1 Control Register

Name: T1CON

Address: 0xFFFF0348

Default value: 0x0000

Access: Read and write

Function: This 16-bit MMR configures the mode of operation of Timer1.

Table 81. T1CON MMR Bit Designations

Bit	Name	Description
15:11		Reserved.
10: 9	T1CLKSEL	Clock source select. [00] = 32.768 kHz oscillator. [01] = 10.24 MHz/CD. [10] = XTALI. [11] = 10.24 MHz.
8	T1DIR	Count up. Set by user for Timer1 to count up. Cleared by user for Timer1 to count down (default).
7	T1EN	Timer1 enable bit. Set by user to enable Timer1. Cleared by user to disable Timer1 (default).
6	T1MOD	Timer1 mode. Set by user to operate in periodic mode. Cleared by user to operate in free running mode (default).
5:4	T1FORMAT	Format. [00] = binary (default). [01] = reserved. [10] = hours:minutes:seconds:hundredths (23 hours to 0 hours). This is only valid with a 32 kHz clock. [11] = hours:minutes:seconds:hundredths (255 hours to 0 hours). This is only valid with a 32 kHz clock.
3:0	T1SCALE	Prescaler. [0000] = source clock/1 (default). [0100] = source clock/16. [1000] = source clock/256. This setting should be used in conjunction with Timer1 in the format hours:minutes:seconds:hundredths. See Format 10 and Format 11 listed with Bits[5:4] in this table (Table 81). [1111] = source clock/32,768.

Timer2 Control Register

Name: T2CON

Address: 0xFFFF0368

Default value: 0x0000

Access: Read and write

Function: This 16-bit MMR configures the mode of operation of Timer2, as described in detail in Table 82.

Table 82. T2CON MMR Bit Designations

Bit	Name	Description
15:9		Reserved. These bits are reserved and should be written as 0 by user code.
8	T2DIR	Count up/count down enable. Set by user code to configure Timer2 to count up. Cleared by user code to configure Timer2 to count down.
7	T2EN	Timer2 enable. Set by user code to enable Timer2. Cleared by user code to disable Timer2.
6	T2MOD	Timer2 operating mode. Set by user code to configure Timer2 to operate in periodic mode. Cleared by user to configure Timer2 to operate in free running mode.
5	WDOGMDEN	Watchdog timer mode enable. Set by user code to enable watchdog mode. Cleared by user code to disable watchdog mode.
4		Reserved. This bit is reserved and should be written as 0 by user code.
3:2	T2SCALE	Timer2 clock (32.768 kHz) prescaler. 00 = 32.768 kHz (default). 01 = source clock/16. 10 = source clock/256. 11 = reserved.
1	WDOGENI	Watchdog timer IRQ enable. Set by user code to produce an IRQ instead of a reset when the watchdog reaches 0. Cleared by user code to disable the IRQ option.
0	T2PDOFF	Stop Timer2 when power-down is enabled. Set by user code to stop Timer2 when the peripherals are powered down using Bit 4 in the POWCON0 MMR. Cleared by user code to enable Timer2 when the peripherals are powered down using Bit 4 in the POWCON0 MMR.

On power-up, PWMCON defaults to 0x0012 (HOFF = 1 and HMODE = 1). All GPIO pins associated with the PWM are configured in PWM mode by default (seeTable 86). Clear the PWM trip interrupt by writing any value to the PWMCLRI MMR. Note that when using the PWM trip interrupt, clear the PWM interrupt before exiting the ISR. This prevents generation of multiple interrupts.

Table 86. PWM Output Selection

PWMCON MMR[1]				PWM Outputs[2]			
ENA	**HOFF**	**POINV**	**DIR**	**PWM0**	**PWM1**	**PWM2**	**PWM3**
0	0	X	X	1	1	1	1
X	1	X	X	1	0	1	0
1	0	0	0	0	0	HS1	LS1
1	0	0	1	HS1	LS1	0	0
1	0	1	0	HS1	LS1	1	1
1	0	1	1	1	1	HS1	LS1

[1] X is don't care.
[2] HS = high side, LS = low side.

Table 87. Compare Registers

Name	Address	Default Value	Access
PWM0COM0	0xFFFF0F84	0x0000	R/W
PWM0COM1	0xFFFF0F88	0x0000	R/W
PWM0COM2	0xFFFF0F8C	0x0000	R/W
PWM1COM0	0xFFFF0F94	0x0000	R/W
PWM1COM1	0xFFFF0F98	0x0000	R/W
PWM1COM2	0xFFFF0F9C	0x0000	R/W
PWM2COM0	0xFFFF0FA4	0x0000	R/W
PWM2COM1	0xFFFF0FA8	0x0000	R/W
PWM2COM2	0xFFFF0FAC	0x0000	R/W

UART Control Register 1

This 8-bit register controls the operation of the UART in conjunction with COMCON0.

COMCON1 Register

Name: COMCON1

Address: 0xFFFF0710

Default value: 0x00

Access: Read and write

Table 91. COMCON1 MMR Bit Designations

Bit	Name	Description
7:5		Reserved bits. Not used.
4	LOOPBACK	Loopback. Set by user to enable loopback mode. In loopback mode, the transmit pin is forced high.
3:2		Reserved bits. Not used.
1	RTS	Request to send. Set by user to force the RTS output to 0. Cleared by user to force the RTS output to 1.
0	DTR	Data terminal ready. Set by user to force the DTR output to 0. Cleared by user to force the DTR output to 1.

UART Status Register 0

COMSTA0 Register

Name: COMSTA0

Address: 0xFFFF0714

Default value: 0x60

Access: Read only

Function: This 8-bit read-only register reflects the current status on the UART.

Table 92. COMSTA0 MMR Bit Designations

Bit	Name	Description
7		Reserved.
6	TEMT	COMTX and shift register empty status bit. Set automatically if COMTX and the shift register are empty. This bit indicates that the data has been transmitted, that is, no more data is present in the shift register. Cleared automatically when writing to COMTX.
5	THRE	COMTX empty status bit. Set automatically if COMTX is empty. COMTX can be written as soon as this bit is set; the previous data might not have been transmitted yet and can still be present in the shift register. Cleared automatically when writing to COMTX.
4	BI	Break indicator. Set when P1.0/IRQ1/SIN/T0 pin is held low for more than the maximum word length. Cleared automatically.
3	FE	Framing error. Set when the stop bit is invalid. Cleared automatically.
2	PE	Parity error. Set when a parity error occurs. Cleared automatically.
1	OE	Overrun error. Set automatically if data is overwritten before being read. Cleared automatically.
0	DR	Data ready. Set automatically when COMRX is full. Cleared by reading COMRX.

I²C Master Status, I2CMSTA, Register

Name: I2CMSTA

Address: 0xFFFF0904

Default value: 0x0000

Access: Read only

Function: This 16-bit MMR is the I²C status register in master mode.

Table 98. I2CMSTA MMR Bit Designations

Bit	Name	Description
15:11		Reserved. These bits are reserved.
10	I2CBBUSY	I²C bus busy status bit. This bit is set to 1 when a start condition is detected on the I²C bus. This bit is cleared when a stop condition is detected on the bus.
9	I2CMRxFO	Master receive FIFO overflow. This bit is set to 1 when a byte is written to the receive FIFO when it is already full. This bit is cleared in all other conditions.
8	I2CMTC	I²C transmission complete status bit. This bit is set to 1 when a transmission is complete between the master and the slave with which it was communicating. If the I2CMCENI bit in I2CMCON is set, an interrupt is generated when this bit is set. Clear this interrupt source.
7	I2CMND	I²C master no acknowledge data bit This bit is set to 1 when a no acknowledge condition is received by the master in response to a data write transfer. If the I2CNACKENI bit in I2CMCON is set, an interrupt is generated when this bit is set. This bit is cleared in all other conditions.
6	I2CMBUSY	I²C master busy status bit. Set to 1 when the master is busy processing a transaction. Cleared if the master is ready or if another master device has control of the bus.
5	I2CAL	I²C arbitration lost status bit. This bit is set to 1 when the I²C master does not gain control of the I²C bus. If the I2CALENI bit in I2CMCON is set, an interrupt is generated when this bit is set. This bit is cleared in all other conditions.
4	I2CMNA	I²C master no acknowledge address bit. This bit is set to 1 when a no acknowledge condition is received by the master in response to an address. If the I2CNACKENI bit in I2CMCON is set, an interrupt is generated when this bit is set. This bit is cleared in all other conditions.
3	I2CMRXQ	I²C master receive request bit. This bit is set to 1 when data enters the receive FIFO. If the I2CMRENI in I2CMCON is set, an interrupt is generated. This bit is cleared in all other conditions.
2	I2CMTXQ	I²C master transmit request bit. This bit goes high if the transmit FIFO is empty or contains only one byte and the master has transmitted an address + write. If the I2CMTENI bit in I2CMCON is set, an interrupt is generated when this bit is set. This bit is cleared in all other conditions.
1:0	I2CMTFSTA	I²C master transmit FIFO status bits. [00] = I²C master transmit FIFO empty. [01] = 1 byte in master transmit FIFO. [10] = 1 byte in master transmit FIFO. [11] = I²C master transmit FIFO full.

I²C Master Receive, I2CMRX, Register

Name: I2CMRX

Address: 0xFFFF0908

Default value: 0x00

Access: Read only

Function: This 8-bit MMR is the I²C master receive register.

I²C Master Transmit, I2CMTX, Register

Name: I2CMTX

Address: 0xFFFF090C

Default value: 0x00

Access: Write only

Function: This 8-bit MMR is the I²C master transmit register.

I²C Master Read Count, I2CMCNT0, Register

Name: I2CMCNT0

Address: 0xFFFF0910

Default value: 0x0000

Access: Read and write

Function: This 16-bit MMR holds the required number of bytes when the master begins a read sequence from a slave device.

Table 99. I2CMCNT0 MMR Bit Designations

Bit	Name	Description
15:9		Reserved.
8	I2CRECNT	Set this bit if more than 256 bytes are required from the slave. Clear this bit when reading 256 bytes or fewer.
7:0	I2CRCNT	These eight bits hold the number of bytes required during a slave read sequence, minus 1. If only a single byte is required, set these bits to 0.

I²C Master Current Read Count, I2CMCNT1, Register

Name: I2CMCNT1

Address: 0xFFFF0914

Default value: 0x00

Access: Read only

Function: This 8-bit MMR holds the number of bytes received so far during a read sequence with a slave device.

I²C Address 0, I2CADR0, Register

Name: I2CADR0

Address: 0xFFFF0918

Default value: 0x00

Access: Read and write

Function: This 8-bit MMR holds the 7-bit slave address and the read/write bit when the master begins communicating with a slave.

Table 100. I2CADR0 MMR in 7-Bit Address Mode

Bit	Name	Description
7:1	I2CADR	These bits contain the 7-bit address of the required slave device.
0	R/$\overline{W}$	Bit 0 is the read/write bit. When this bit = 1, a read sequence is requested. When this bit = 0, a write sequence is requested.

Table 101. I2CADR0 MMR in 10-Bit Address Mode

Bit	Name	Description
7:3		These bits must be set to [11110b] in 10-bit address mode.
2:1	I2CMADR	These bits contain ADDR[9:8] in 10-bit addressing mode.
0	R/$\overline{W}$	Read/write bit. When this bit = 1, a read sequence is requested. When this bit = 0, a write sequence is requested.

Table 112. GPxCON MMR Bit Designations

Bit	Description
31:30	Reserved.
29:28	Reserved.
27:26	Reserved.
25:24	Selects the function of the P0.6/RTS and P1.6/PWM pins.
23:22	Reserved.
21:20	Selects the function of the P0.5/CTS and P1.5/PWM3 pins.
19:18	Reserved.
17:16	Selects the function of the P0.4/IRQ0/PWM1 and P1.4/PWM2 pins.
15:14	Reserved.
13:12	Selects the function of the P0.3/MOSI/SDA and P1.3/TRIP pins.
11:10	Reserved.
9:8	Selects the function of the P0.2/MISO and P1.2/SYNC pins.
7:6	Reserved.
5:4	Selects the function of the P0.1/SCLK/SCL, P1.1/SOUT, and P2.1/IRQ3/PWM5 pins.
3:2	Reserved.
1:0	Selects the function of the P0.0/$\overline{SS}$, P1.0/IRQ1/SIN/T0, P2.0/IRQ2/PWM0/EXTCLK pins.

GPxDAT REGISTERS

GPxDAT are Port x configuration and data registers. They configure the direction of the GPIO pins of Port x, set the output value for the pins that are configured as output, and store the input value of the pins that are configured as input.

Table 113. GPxDAT Registers

Name	Address	Default Value	Access
GP0DAT	0xFFFF0D20	0x000000XX	R/W
GP1DAT	0xFFFF0D30	0x000000XX	R/W
GP2DAT	0xFFFF0D40	0x000000XX	R/W

Table 114. GPxDAT MMR Bit Designations

Bit	Description
31:24	Direction of the data. Set to 1 by user to configure the GPIO pin as an output. Cleared to 0 by user to configure the GPIO pin as an input.
23:16	Port x data output.
15:8	Reflect the state of Port x pins at reset (read only).
7:0	Port x data input (read only).

GPxSET REGISTERS

GPxSET are data set Port x registers.

Table 115. GPxSET Registers

Name	Address	Default Value	Access
GP0SET	0xFFFF0D24	0x000000XX	W
GP1SET	0xFFFF0D34	0x000000XX	W
GP2SET	0xFFFF0D44	0x000000XX	W

Table 116. GPxSET MMR Bit Designations

Bit	Description
31:24	Reserved.
23:16	Data Port x set bit. Set to 1 by user to set bit on Port x; also sets the corresponding bit in the GPxDAT MMR. Cleared to 0 by user; does not affect the data output.
15:0	Reserved.

GPxCLR REGISTERS

GPxCLR are data clear Port x registers.

Table 117. GPxCLR Registers

Name	Address	Default Value	Access
GP0CLR	0xFFFF0D28	0x000000XX	W
GP1CLR	0xFFFF0D38	0x000000XX	W
GP2CLR	0xFFFF0D48	0x000000XX	W

Table 118. GPxCLR MMR Bit Designations

Bit	Description
31:24	Reserved.
23:16	Data Port x clear bit. Set to 1 by user to clear the bit on Port x; also clears the corresponding bit in the GPxDAT MMR. Cleared to 0 by user; does not affect the data output.
15:0	Reserved.

GPxPAR REGISTERS

The GPxPAR registers program the parameters for Port 0, Port 1, and Port 2. Note that the GPxDAT MMR must always be written after changing the GPxPAR MMR. Note that it is not possible to disable the internal pull-up resistor on P0.2.

Table 119. GPxPAR Registers

Name	Address	Default Value	Access
GP0PAR	0xFFFF0D2C	0x00000000	R/W
GP1PAR	0xFFFF0D3C	0x00000000	R/W
GP2PAR	0xFFFF0D4C	0x00000000	R/W

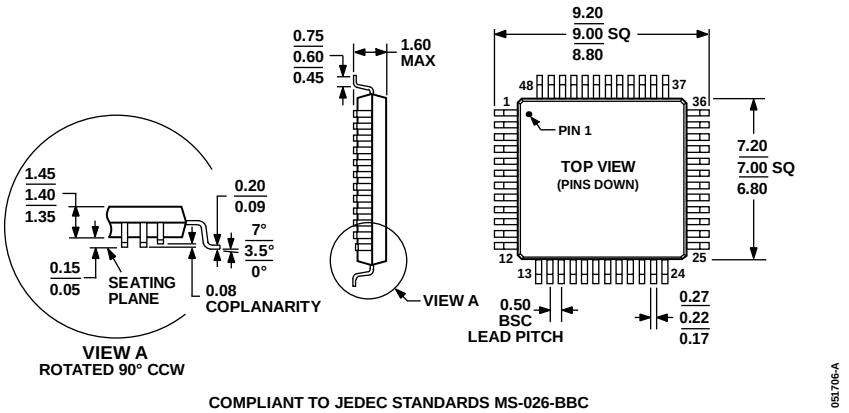

Figure 32. 48-Lead Low Profile Quad Flat Package [LQFP]
(ST-48)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Ordering Quantity
ADuC7060BCPZ32	−40°C to +125°C	48-Lead Lead Frame Chip Scale Package [LFCSP]	CP-48-5	
ADuC7060BCPZ32-RL	−40°C to +125°C	48-Lead Lead Frame Chip Scale Package [LFCSP]	CP-48-5	2,500
ADuC7060BSTZ32	−40°C to +125°C	48-Lead Low Profile Quad Flat Package [LQFP]	ST-48	
ADuC7060BSTZ32-RL	−40°C to +125°C	48-Lead Low Profile Quad Flat Package [LQFP]	ST-48	2,000
ADuC7061BCPZ32	−40°C to +125°C	32-Lead Lead Frame Chip Scale Package [LFCSP]	CP-32-11	
ADuC7061BCPZ32-RL	−40°C to +125°C	32-Lead Lead Frame Chip Scale Package [LFCSP]	CP-32-11	5,000
EVAL-ADuC7060QSPZ		ADuC7060 Quick Start Plus Development System		
EVAL-ADuC7061MKZ		ADuC7061 Quick Start Evaluation System		

[1] Z = RoHS Compliant Part.