Nuvoton Technology Corporation - W78E516B40FL Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8052
Core Size	8-Bit
Speed	40MHz
Connectivity	EBI/EMI, UART/USART
Peripherals	POR
Number of I/O	36
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-BQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/w78e516b40fl

5.3 Clock

The W78E516B is designed with either a crystal oscillator or an external clock. Internally, the clock is divided by two before it is used by default. This makes the W78E516B relatively insensitive to duty cycle variations in the clock.

5.4 Crystal Oscillator

The W78E516B incorporates a built-in crystal oscillator. To make the oscillator work, a crystal must be connected across pins XTAL1 and XTAL2. In addition, a load capacitor must be connected from each pin to ground, and a resistor must also be connected from XTAL1 to XTAL2 to provide a DC bias when the crystal frequency is above 24 MHz.

5.5 External Clock

An external clock should be connected to pin XTAL1. Pin XTAL2 should be left unconnected. The XTAL1 input is a CMOS-type input, as required by the crystal oscillator. As a result, the external clock signal should have an input one level of greater than 3.5 volts.

5.6 Power Management

Idle Mode

Setting the IDL bit in the PCON register enters the idle mode. In the idle mode, the internal clock to the processor is stopped. The peripherals and the interrupt logic continue to be clocked. The processor will exit idle mode when either an interrupt or a reset occurs.

Power-down Mode

When the PD bit in the PCON register is set, the processor enters the power-down mode. In this mode all of the clocks are stopped, including the oscillator. To exit from power-down mode is by a hardware reset or external interrupts $\overline{\text{INT0}}$ to $\overline{\text{INT1}}$ when enabled and set to level triggered.

5.7 Reduce EMI Emission

The W78E516B allows user to diminish the gain of on-chip oscillator amplifier by using programmer to clear the B7 bit of security register. Once B7 is set to 0, a half of gain will be decreased. Care must be taken if user attempts to diminish the gain of oscillator amplifier, reducing a half of gain may affect the external crystal operating improperly at high frequency above 24 MHz. The value of R and C1, C2 may need some adjustment while running at lower gain.

5.8 Reset

The external RESET signal is sampled at S5P2. To take effect, it must be held high for at least two machine cycles while the oscillator is running. An internal trigger circuit in the reset line is used to deglitch the reset line when the W78E516B is used with an external RC network. The reset logic also has a special glitch removal circuit that ignores glitches on the reset line. During reset, the ports are initialized to FFH, the stack pointer to 07H, PCON (with the exception of bit 4) to 00H, and all of the other SFR registers except SBUF to 00H. SBUF is not reset.

W78E516B Special Function Registers (SFRs) and Reset Values

F8									FF
F0	+B 00000000						**CHPENR** **00000000**		F7
E8									EF
E0	+ACC 00000000								E7
D8	**+P4** **xxxx1111**								DF
D0	+PSW 00000000								D7
C8	+T2CON 00000000		RCAP2L 00000000	RCAP2H 00000000	TL2 00000000	TH2 00000000			CF
C0	XICON 00000000		**P4CONA** **00000000**	**P4CONB** **00000000**	**SFRAL** **00000000**	**SFRAH** **00000000**	**SFRFD** **00000000**	**SFRCN** **00000000**	C7
B8	+IP 00000000							**CHPCON** **0xx00000**	BF
B0	+P3 00000000				**P43AL** **00000000**	**P43AH** **00000000**			B7
A8	+IE 00000000				**P42AL** **00000000**	**P42AH** **00000000**	**P2ECON** **0000XX00**		AF
A0	+P2 11111111								A7
98	+SCON 00000000	SBUF xxxxxxxx					**P2EAL** **00000000**	**P2EAH** **00000000**	9F
90	+P1 11111111				**P41AL** **00000000**	**P41AH** **00000000**			97
88	+TCON 00000000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000			8F
80	+P0 11111111	SP 00000111	DPL 00000000	DPH 00000000	**P40AL** **00000000**	**P40AH** **00000000**		PCON 00110000	87

Notes:

1. The SFRs marked with a plus sign(+) are both byte- and bit-addressable.
2. The text of SFR with bold type characters are extension function registers.

P2ECON (AEH)

BIT	NAME	FUNCTION
7	P43CSINV	The active polarity of P4.3 when pin P4.3 is defined as read and/or write strobe signal. = 1: P4.3 is active high when pin P4.3 is defined as read and/or write strobe signal. = 0: P4.3 is active low when pin P4.3 is defined as read and/or write strobe signal.
6	P42CSINV	The similarity definition as P43SINV.
5	P41CSINV	The similarity definition as P43SINV.
5	P41CSINV	The similarity definition as P43SINV.
4	P40CSINV	The similarity definition as P43SINV.
3	-	Reserve
2	-	Reserve
1	-	0
0	-	0

5.11 Port 4 Base Address Registers

P40AH, P40AL:

The Base address register for comparator of P4.0. P40AH contains the high-order byte of address, P40AL contains the low-order byte of address.

P41AH, P41AL:

The Base address register for comparator of P4.1. P41AH contains the high-order byte of address, P41AL contains the low-order byte of address.

P42AH, P42AL:

The Base address register for comparator of P4.2. P42AH contains the high-order byte of address, P42AL contains the low-order byte of address.

P43AH, P43AL:

The Base address register for comparator of P4.3. P43AH contains the high-order byte of address, P43AL contains the low-order byte of address.

P4 (D8H)

BIT	NAME	FUNCTION
7	-	Reserve
6	-	Reserve
5	-	Reserve
4	-	Reserve
3	P43	Port 4 Data bit which outputs to pin P4.3 at mode 0.
2	P42	Port 4 Data bit which outputs to pin P4.2 at mode 0.
1	P41	Port 4 Data bit which outputs to pin P4.1at mode 0.
0	P40	Port 4 Data bit which outputs to pin P4.0 at mode 0.

Here is an example to program the P4.0 as a write strobe signal at the I/O port address 1234H – 1237H and positive polarity, and P4.1 – P4.3 are used as general I/O ports.

```
MOV  P40AH, #12H
MOV  P40AL, #34H            ; Base I/O address 1234H for P4.0
MOV  P4CONA, #00001010B     ; P4.0 a write strobe signal and address line A0 and A1 are masked.
MOV  P4CONB, #00H           ; P4.1 – P4.3 as general I/O port which are the same as PORT1
MOV  P2ECON, #10H           ; Write the P40SINV = 1 to inverse the P4.0 write strobe polarity
                            ; default is negative.
```

Then any instruction MOVX @DPTR, A (with DPTR = 1234H – 1237H) will generate the positive polarity write strobe signal at pin P4.0. And the instruction MOV P4, #XX will output the bit3 to bit1 of data #XX to pin P4.3 – P4.1.

SFRAH, SFRAL: The objective address of on-chip Flash EPROM in the in-system programming mode. SFRFAH contains the high-order byte of address, SFRFAL contains the low-order byte of address.

SFRFD: The programming data for on-chip Flash EPROM in programming mode.

SFRCN: The control byte of on-chip Flash EPROM programming mode.

SFRCN (C7)

BIT	NAME	FUNCTION
7	-	Reserve.
6	WFWIN	On-chip Flash EPROM bank select for in-system programming. = 0: 64K bytes Flash EPROM bank is selected as destination for re-programming. = 1: 4K bytes Flash EPROM bank is selected as destination for re-programming.
5	OEN	Flash EPROM output enable.
4	CEN	Flash EPROM chip enable.
3, 2, 1, 0	CTRL[3:0]	The flash control signals

MODE	WFWIN	CTRL<3:0>	OEN	CEN	SFRAH, SFRAL	SFRFD
Erase 64KB APROM	0	0010	1	0	X	X
Program 64KB APROM	0	0001	1	0	Address in	Data in
Read 64KB APROM	0	0000	0	0	Address in	Data out
Erase 4KB LDROM	1	0010	1	0	X	X
Program 4KB LDROM	1	0001	1	0	Address in	Data in
Read 4KB LDROM	1	0000	0	0	Address in	Data out

5.13 In-System Programming Control Register (CHPCON)

CHPCON (BFH)

BIT	NAME	FUNCTION
7	SWRESET (F04KMODE)	When this bit is set to 1, and both FBOOTSL and FPROGEN are set to 1. It will enforce microcontroller reset to initial condition just like power on reset. This action will re-boot the microcontroller and start to normal operation. To read this bit in logic-1 can determine that the F04KBOOT mode is running.
6	-	Reserve.
5	-	Reserve.
4	ENAUXRAM	1: Enable on-chip AUX-RAM. 0: Disable the on-chip AUX-RAM
3	0	Must set to 0.
2	0	Must set to 0.
1	FBOOTSL	The Program Location Select. 0: The Loader Program locates at the 64 KB APROM. 4KB LDROM is destination for re-programming. 1: The Loader Program locates at the 4 KB memory bank. 64KB APROM is destination for re-programming.
0	FPROGEN	FLASH EPROM Programming Enable. = 1: enable. The microcontroller enter the in-system programming mode after entering the idle mode and wake-up from interrupt. During in-system programming mode, the operation of erase, program and read are achieve when device enters idle mode. = 0: disable. The on-chip flash memory is read-only. In-system programmability is disabled.

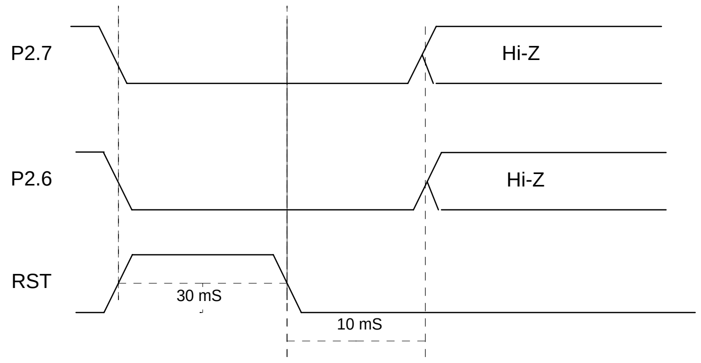
F04KBOOT Mode (Boot from LDROM)

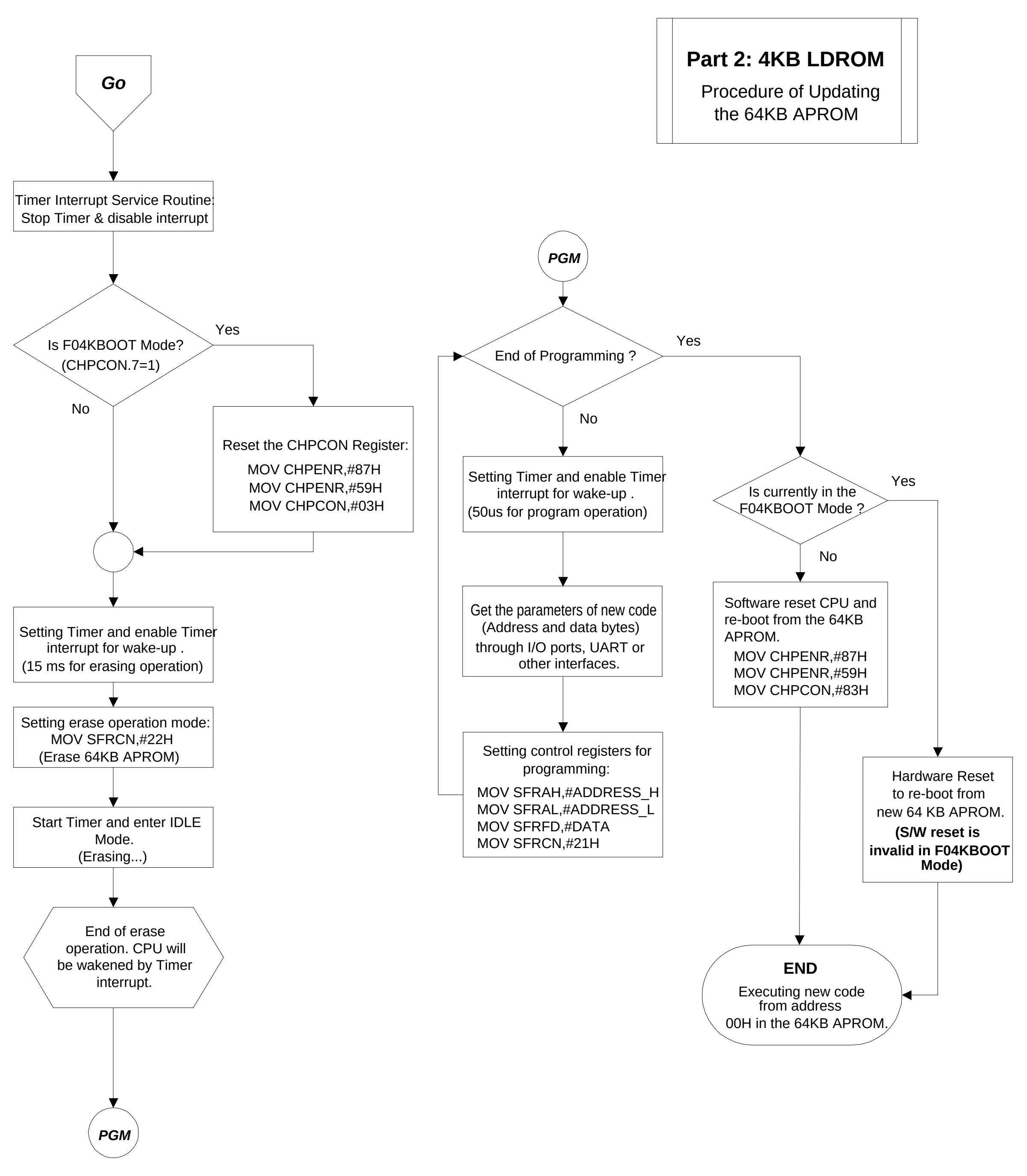
By default, the W78E516B boots from APROM program after a power on reset. On some occasions, user can force the W78E516B to boot from the LDROM program via following settings. The possible situation that you need to enter F04KBOOT mode when the APROM program can not run properly and device can not jump back to LDROM to execute in-system programming function. Then you can use this F04KBOOT mode to force the W78E516B jumps to LDROM and executes in-system programming procedure. When you design your system, you may reserve the pins P2.6, P2.7 to switches or jumpers. For example in a CD-ROM system, you can connect the P2.6 and P2.7 to PLAY and EJECT buttons on the panel. When the APROM program fails to execute the normal application program. User can press both two buttons at the same time and then turn on the power of the personal computer to force the W78E516B to enter the F04KBOOT mode. After power on of personal computer, you can release both buttons and finish the in-system programming procedure to update the APROM code. In application system design, user must take care of the P2, P3, ALE, $\overline{EA}$ and $\overline{PSEN}$ pin value at reset to prevent from accidentally activating the programming mode or F04KBOOT mode.

F04KBOOT MODE

P4.3	P2.7	P2.6	MODE
X	L	L	FO4KBOOT
L	X	X	FO4KBOOT

The Reset Timing For Entering F04KBOOT Mode

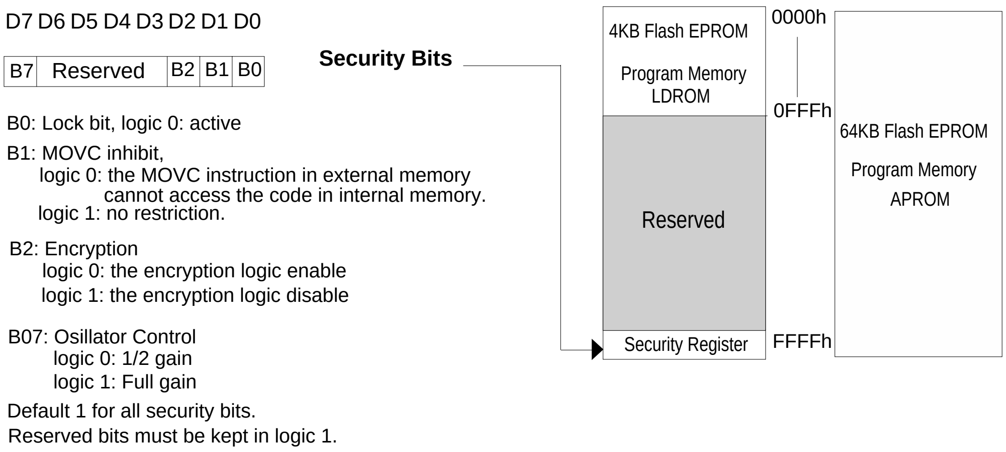



Part 2: 4KB LDROM
Procedure of Updating the 64KB APROM
Go
Timer Interrupt Service Routine: Stop Timer & disable interrupt
Is F04KBOOT Mode? (CHPCON.7=1)
Yes
No
Reset the CHPCON Register:
MOV CHPENR,#87H
MOV CHPENR,#59H
MOV CHPCON,#03H
Setting Timer and enable Timer interrupt for wake-up . (15 ms for erasing operation)
Setting erase operation mode: MOV SFRCN,#22H (Erase 64KB APROM)
Start Timer and enter IDLE Mode. (Erasing...)
End of erase operation. CPU will be wakened by Timer interrupt.
PGM
PGM
End of Programming ?
Yes
No
Setting Timer and enable Timer interrupt for wake-up . (50us for program operation)
Get the parameters of new code (Address and data bytes) through I/O ports, UART or other interfaces.
Setting control registers for programming:
MOV SFRAH,#ADDRESS_H
MOV SFRAL,#ADDRESS_L
MOV SFRFD,#DATA
MOV SFRCN,#21H
Is currently in the F04KBOOT Mode ?
Yes
No
Software reset CPU and re-boot from the 64KB APROM.
MOV CHPENR,#87H
MOV CHPENR,#59H
MOV CHPCON,#83H
Hardware Reset to re-boot from new 64 KB APROM.
(S/W reset is invalid in F04KBOOT Mode)
END
Executing new code from address 00H in the 64KB APROM.

6. SECURITY

During the on-chip Flash EPROM programming mode, the Flash EPROM can be programmed and verified repeatedly. Until the code inside the Flash EPROM is confirmed OK, the code can be protected. The protection of Flash EPROM and those operations on it are described below.

The W78E516B has a Special Setting Register, the Security Register, which can not be accessed in programming mode. Those bits of the Security Register can not be changed once they have been programmed from high to low. They can only be reset through erase-all operation. The Security Register is located at the 0FFFFH of the LDROM space.



B0: Lock bit, logic 0: active

B1: MOVC inhibit,
logic 0: the MOVC instruction in external memory cannot access the code in internal memory.
logic 1: no restriction.

B2: Encryption
logic 0: the encryption logic enable
logic 1: the encryption logic disable

B07: Osillator Control
logic 0: 1/2 gain
logic 1: Full gain

Default 1 for all security bits.
Reserved bits must be kept in logic 1.

Special Setting Register

6.1 Lock Bit

This bit is used to protect the customer's program code in the W78E516B. It may be set after the programmer finishes the programming and verifies sequence. Once this bit is set to logic 0, both the Flash EPROM data and Special Setting Registers can not be accessed again.

6.2 MOVC Inhibit

This bit is used to restrict the accessible region of the MOVC instruction. It can prevent the MOVC instruction in external program memory from reading the internal program code. When this bit is set to logic 0, a MOVC instruction in external program memory space will be able to access code only in the external memory, not in the internal memory. A MOVC instruction in internal program memory space will always be able to access the ROM data in both internal and external memory. If this bit is logic 1, there are no restrictions on the MOVC instruction.

7. ELECTRICAL CHARACTERISTICS

7.1 Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
DC Power Supply	$V_{DD} - V_{SS}$	-0.3	+6.0	V
Input Voltage	V_{IN}	V_{SS} -0.3	V_{DD} +0.3	V
Operating Temperature	T_A	0	70	°C
Storage Temperature	T_{ST}	-55	+150	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

7.2 D.C. Characteristics

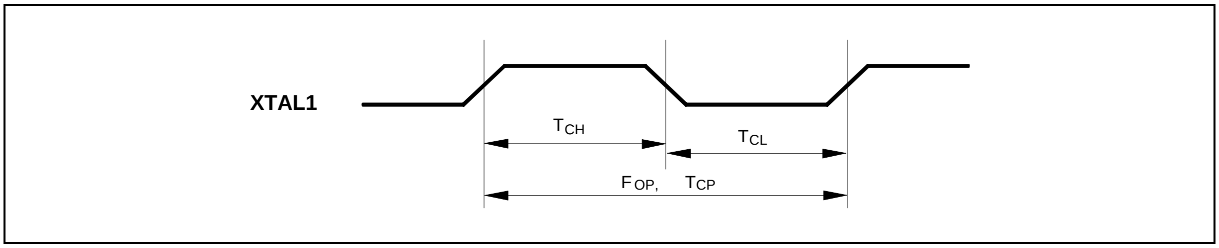
($V_{DD} - V_{SS}$ = 5V ±10%, T_A = 25°C, Fosc = 20 MHz, unless otherwise specified.)

PARAMETER	SYM.	SPECIFICATION			TEST CONDITIONS
		MIN.	MAX.	UNIT	
Operating Voltage	V_{DD}	4.5	5.5	V	RST = 1, P0 = V_{DD}
Operating Current	I_{DD}	-	20	mA	No load V_{DD} = 5.5V
Idle Current	I_{IDLE}	-	6	mA	Idle mode V_{DD} = 5.5V
Power Down Current	I_{PWDN}	-	50	μA	Power-down mode V_{DD} = 5.5V
Input Current P1, P2, P3, P4	I_{IN1}	-50	+10	μA	V_{DD} = 5.5V V_{IN} = 0V or V_{DD}
Input Current RST	I_{IN2}	-10	+300	μA	V_{DD} = 5.5V 0< V_{IN} <V_{DD}
Input Leakage Current P0, $\overline{EA}$	I_{LK}	-10	+10	μA	V_{DD} = 5.5V 0V< V_{IN} < V_{DD}
Logic 1 to 0 Transition Current P1, P2, P3, P4	I_{TL}[*4]	-500	-	μA	V_{DD} = 5.5V V_{IN} = 2.0V
Input Low Voltage P0, P1, P2, P3, P4, $\overline{EA}$	V_{IL1}	0	0.8	V	V_{DD} = 4.5V
Input Low Voltage RST	VIL2	0	0.8	V	VDD = 4.5V
Input Low Voltage XTAL1[*4]	VIL3	0	0.8	V	VDD = 4.5V

7.3 A.C. Characteristics

The AC specifications are a function of the particular process used to manufacture the part, the ratings of the I/O buffers, the capacitive load, and the internal routing capacitance. Most of the specifications can be expressed in terms of multiple input clock periods (TCP), and actual parts will usually experience less than a ±20 nS variation. The numbers below represent the performance expected from a 0.6 micron CMOS process when using 2 and 4 mA output buffers.

7.3.1 Clock Input Waveform



PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
Operating Speed	Fop	0	-	40	MHz	1
Clock Period	TCP	25	-	-	nS	2
Clock High	Tch	10	-	-	nS	3
Clock Low	Tcl	10	-	-	nS	3

Notes:

1. The clock may be stopped indefinitely in either state.
2. The TCP specification is used as a reference in other specifications.
3. There are no duty cycle requirements on the XTAL1 input.

7.3.2 Program Fetch Cycle

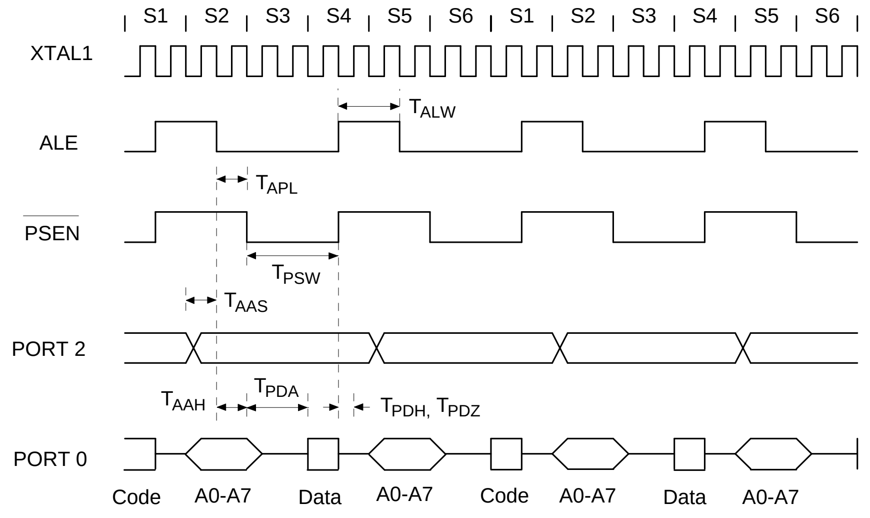
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
Address Valid to ALE Low	TAAS	1 TCP-Δ	-	-	nS	4
Address Hold from ALE Low	TAAH	1 TCP-Δ	-	-	nS	1, 4
ALE Low to $\overline{\text{PSEN}}$ Low	TAPL	1 TCP-Δ	-	-	nS	4
$\overline{\text{PSEN}}$ Low to Data Valid	TPDA	-	-	2 TCP	nS	2
Data Hold after $\overline{\text{PSEN}}$ High	TPDH	0	-	1 TCP	nS	3
Data Float after $\overline{\text{PSEN}}$ High	TPDZ	0	-	1 TCP	nS	
ALE Pulse Width	TALW	2 TCP-Δ	2 TCP	-	nS	4
$\overline{\text{PSEN}}$ Pulse Width	TPSW	3 TCP-Δ	3 TCP	-	nS	4

Notes:

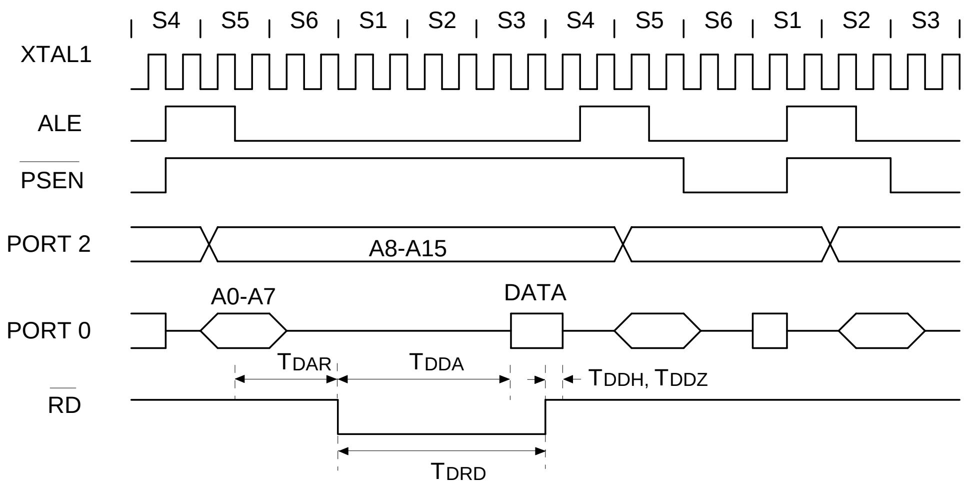
1. P0.0 – P0.7, P2.0 – P2.7 remain stable throughout entire memory cycle.
2. Memory access time is 3 TCP.
3. Data have been latched internally prior to $\overline{\text{PSEN}}$ going high.
4. "Δ" (due to buffer driving delay and wire loading) is 20 nS.

8. TIMING WAVEFORMS

8.1 Program Fetch Cycle

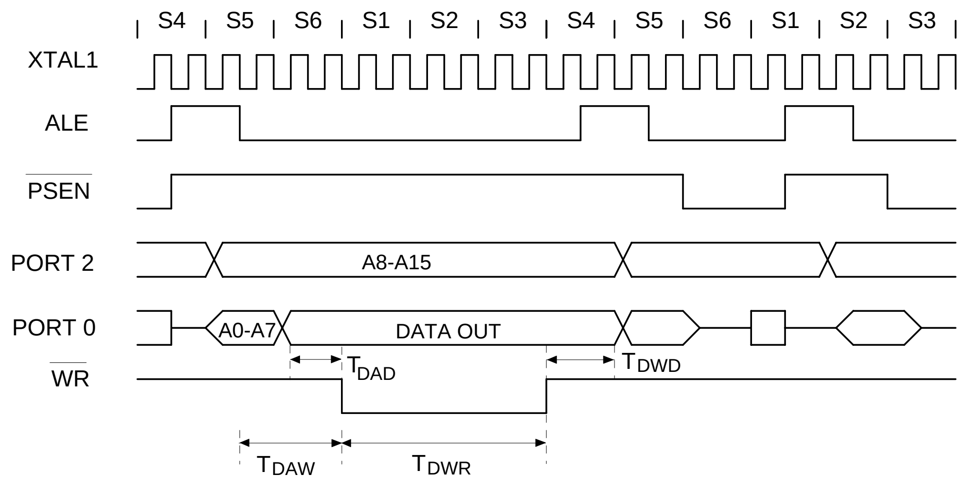


8.2 Data Read Cycle

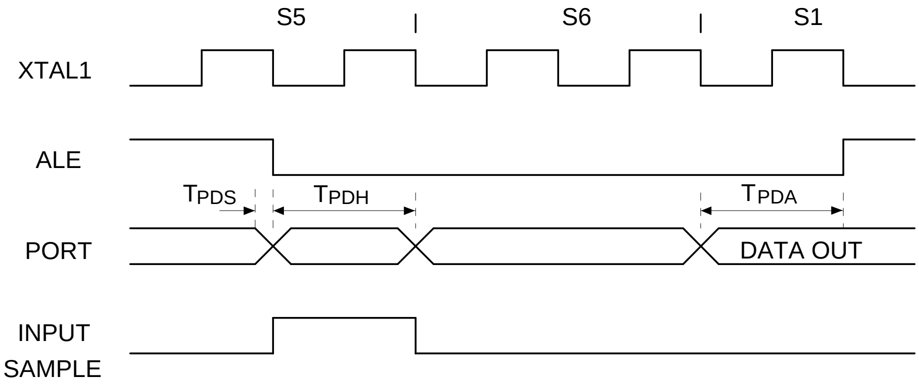


Timing Waveforms, continued

8.3 Data Write Cycle



8.4 Port Access Cycle



9. TYPICAL APPLICATION CIRCUITS

9.1 External Program Memory and Crystal

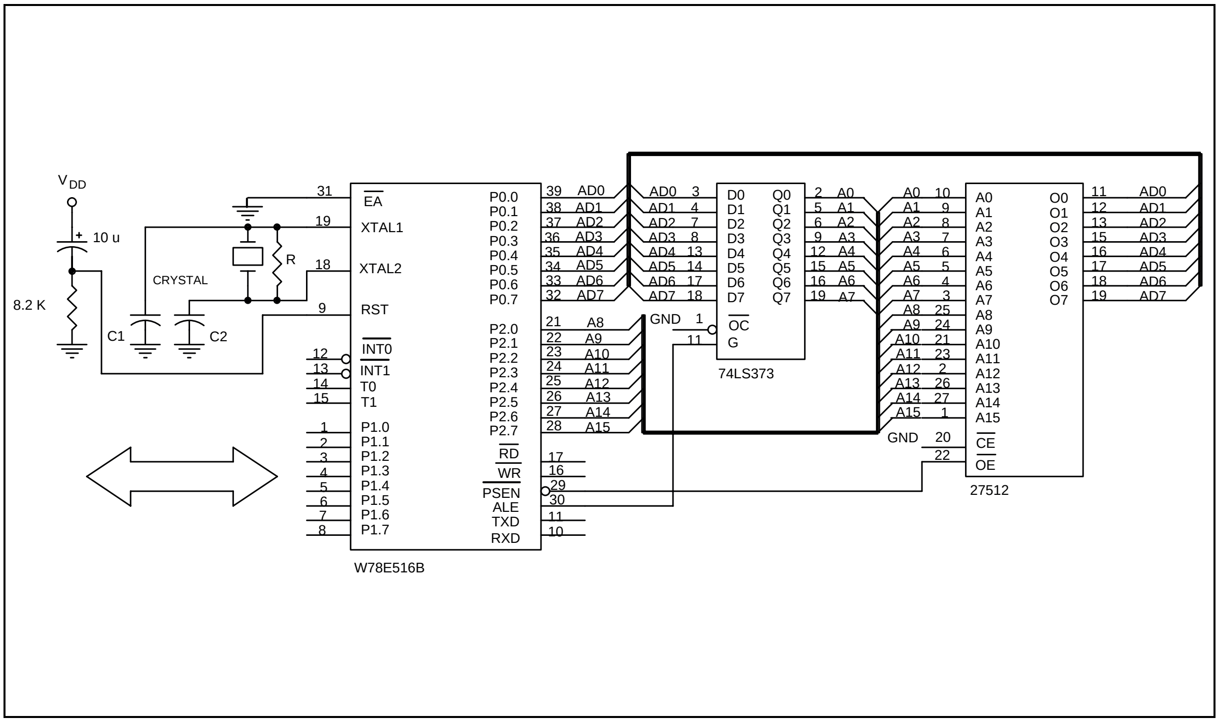


Figure A

CRYSTAL	C1	C2	R
6 MHz	47P	47P	-
16 MHz	30P	30P	-
24 MHz	15P	10P	-
32 MHz	10P	10P	6.8K
40 MHz	5P	5P	4.7K

Above table shows the reference values for crystal applications.

Notes:

1. C1, C2, R components refer to Figure A
2. Crystal layout must get close to XTAL1 and XTAL2 pins on user's application board.

Typical Application Circuits, continued

9.2 Expanded External Data Memory and Oscillator

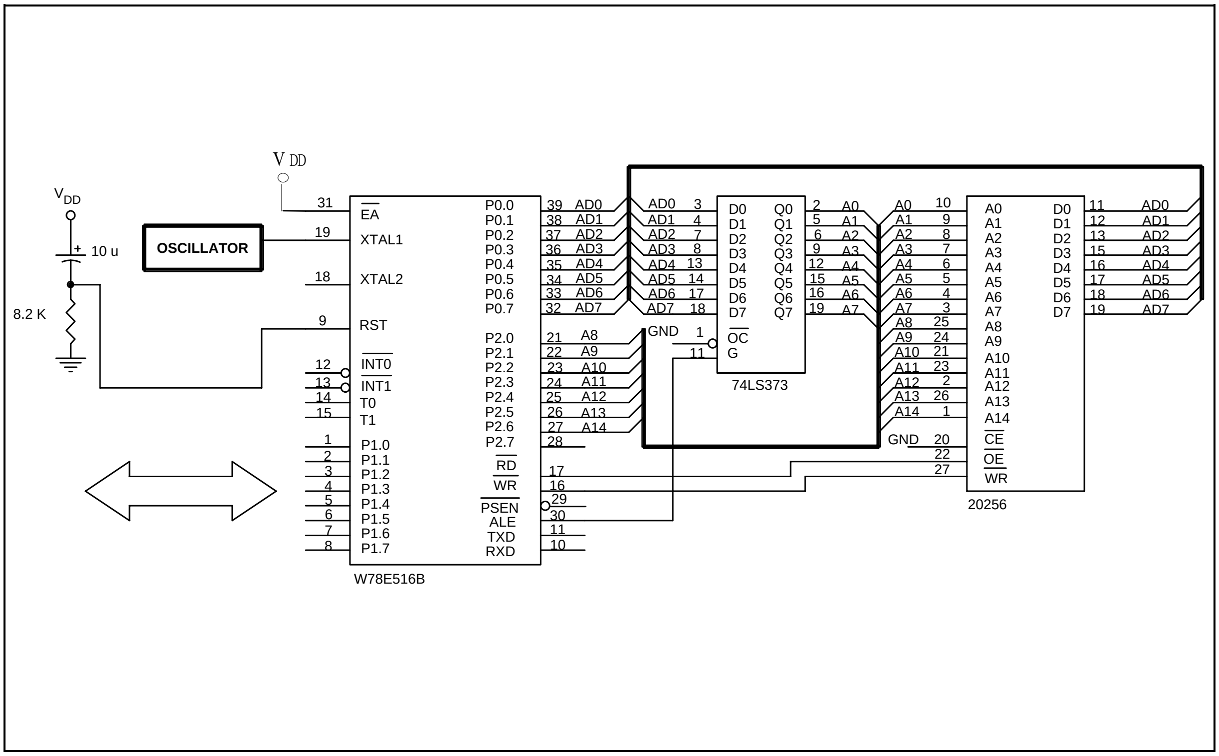
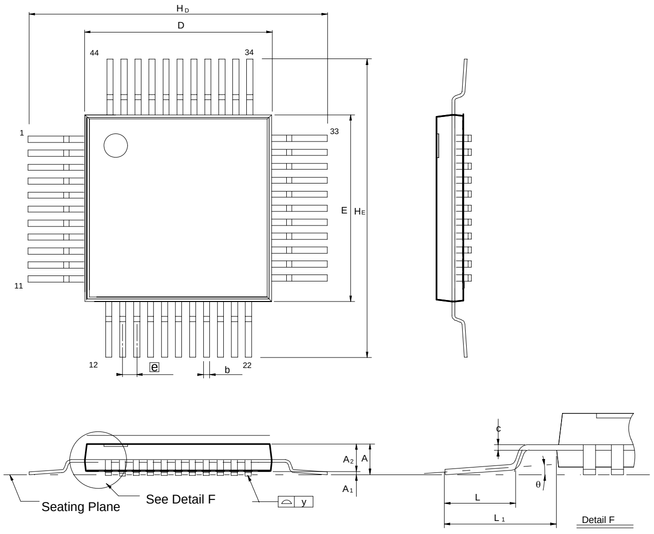


Figure B

Package Dimensions, continued.

10.3 44-pin PQFP



Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	---	---	---	---	---	---
A_1	0.002	0.01	0.02	0.05	0.25	0.5
A_2	0.075	0.081	0.087	1.90	2.05	2.20
b	0.01	0.014	0.018	0.25	0.35	0.45
c	0.004	0.006	0.010	0.101	0.152	0.254
D	0.390	0.394	0.398	9.9	10.00	10.1
E	0.390	0.394	0.398	9.9	10.00	10.1
$\boxed{e}$	0.025	0.031	0.036	0.635	0.80	0.952
H_D	0.510	0.520	0.530	12.95	13.2	13.45
H_E	0.510	0.520	0.530	12.95	13.2	13.45
L	0.025	0.031	0.037	0.65	0.8	0.95
L_1	0.051	0.063	0.075	1.295	1.6	1.905
y	—	—	0.003	—	—	0.08
θ	0°	—	7°	0°	—	7°

Notes:

1. Dimension D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion.
3. Controlling dimension: Millimeter
4. General appearance spec. should be based on final visual inspection spec.

```
MAIN_4K:
        MOV SP, #C0H            ; BE INITIAL SP REGISTER
         MOV CHPENR, #87H       ; CHPENR = 87H, CHPCON WRITE ENABLE.
        MOV CHPENR, #59H        ; CHPENR = 59H, CHPCON WRITE ENABLE.
         MOV A, CHPCON
        ANL A, #80H
        CJNE A, #80H, UPDATE_64K  ; CHECK  F04KBOOT MODE ?

        MOV CHPCON, #03H        ; CHPCON = 03H, ENABLE IN-SYSTEM PROGRAMMING.
        MOV CHPENR, #00H        ; DISABLE CHPCON WRITE ATTRIBUTE

        MOV TCON, #00H          ; TCON = 00H, TR = 0 TIMER0 STOP
         MOV TMOD, #01H         ; TMOD = 01H, SET TIMER0 A 16BIT TIMER
        MOV IP, #00H            ; IP = 00H
        MOV IE, #82H            ; IE = 82H, TIMER0 INTERRUPT ENABLED
        MOV R6, #F0H
        MOV R7, #FFH
        MOV TL0, R6
        MOV TH0, R7
        MOV TCON, #10H          ; TCON = 10H, TR0 = 1, GO
        MOV PCON, #01H          ; ENTER IDLE MODE

 UPDATE_64K:
        MOV CHPENR, #00H        ; DISABLE CHPCON WRITE-ATTRIBUTE
        MOV TCON, #00H          ; TCON = 00H, TR = 0 TIM0 STOP
        MOV IP, #00H            ; IP = 00H
        MOV IE, #82H            ; IE = 82H, TIMER0 INTERRUPT ENABLED
        MOV TMOD, #01H          ; TMOD = 01H, MODE1
        MOV R6, #3CH            ; SET WAKE-UP TIME FOR ERASE OPERATION, ABOUT 15 mS. DEPENDING
                                ; ON USER'S SYSTEM CLOCK RATE.
        MOV R7, #B0H
        MOV TL0, R6
        MOV TH0, R7

ERASE_P_4K:
        MOV SFRCN, #22H         ; SFRCN(C7H) = 22H  ERASE 64K
        MOV TCON, #10H          ; TCON = 10H, TR0 = 1,GO
        MOV PCON, #01H          ; ENTER IDLE MODE (FOR ERASE OPERATION)

;************************************************************************
;* BLANK CHECK
;************************************************************************
        MOV SFRCN, #0H          ; READ 64KB APROM MODE
        MOV SFRAH, #0H          ; START ADDRESS = 0H
        MOV SFRAL, #0H
         MOV R6, #FBH           ; SET TIMER FOR READ OPERATION, ABOUT 1.5 µS.
        MOV R7, #FFH
        MOV TL0, R6
        MOV TH0, R7

BLANK_CHECK_LOOP:
        SETB TR0                ; ENABLE TIMER 0
        MOV PCON, #01H          ; ENTER IDLE MODE
        MOV A, SFRFD            ; READ ONE BYTE
        CJNE A, #FFH, BLANK_CHECK_ERROR
```

```
        INC SFRAL                  ; NEXT ADDRESS
        MOV A, SFRAL
        JNZ BLANK_CHECK_LOOP
        INC SFRAH
        MOV A, SFRAH
        CJNE A, #0H, BLANK_CHECK_LOOP   ; END ADDRESS = FFFFH
        JMP PROGRAM_64KROM

BLANK_CHECK_ERROR:
        MOV P1, #F0H
        MOV P3, #F0H
        JMP $

;*****************************************************************************
;* RE-PROGRAMMING 64KB APROM BANK
;*****************************************************************************
PROGRAM_64KROM:
        MOV DPTR, #0H              ; THE ADDRESS OF NEW ROM CODE
         MOV R2, #00H              ; TARGET LOW BYTE ADDRESS
        MOV R1, #00H               ; TARGET HIGH BYTE ADDRESS
        MOV DPTR, #0H              ; EXTERNAL SRAM BUFFER ADDRESS
        MOV SFRAH, R1              ; SFRAH, TARGET HIGH ADDRESS
         MOV SFRCN, #21H           ; SFRCN (C7H) = 21 (PROGRAM 64K)
        MOV R6, #5AH               ; SET TIMER FOR PROGRAMMING, ABOUT 50 µS.
        MOV R7, #FFH
        MOV TL0, R6
        MOV TH0, R7

PROG_D_64K:
        MOV SFRAL, R2              ; SFRAL (C4H) = LOW BYTE ADDRESS
        MOVX A, @DPTR              ; READ DATA FROM EXTERNAL SRAM BUFFER
        MOV SFRFD, A               ; SFRFD (C6H) = DATA IN
        MOV TCON, #10H             ; TCON = 10H, TR0 = 1, GO
        MOV PCON, #01H             ; ENTER IDLE MODE (PRORGAMMING)
        INC DPTR
        INC R2
        CJNE R2, #0H, PROG_D_64K
        INC  R1
        MOV SFRAH, R1
        CJNE R1, #0H, PROG_D_64K

;***************************************************************************
; * VERIFY 64KB APROM BANK
;***************************************************************************
        MOV R4, #03H               ; ERROR COUNTER
        MOV R6, #FBH               ; SET TIMER FOR READ VERIFY, ABOUT 1.5 µS.
        MOV R7, #FFH
        MOV TL0, R6
        MOV TH0, R7
        MOV DPTR, #0H              ; The start address of sample code
        MOV R2, #0H                ; Target low byte address
        MOV R1, #0H                ; Target high byte address
        MOV SFRAH, R1              ; SFRAH, Target high address
        MOV SFRCN, #00H            ; SFRCN = 00 (Read ROM CODE)
```

12. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A5	June, 2002	-	Formerly issued
A6	June, 2004	3	Revise part number in the item of packages
A7	Aug, 2004	26	Revise title of 10.1
A8	Jan, 2005	3	Add Lead Free package
A9	April 20, 2005	35	Add Important Notice
A10	October 2, 2006		Remove block diagram
A11	December 4, 2006	3	Remove all Leaded package parts

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