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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XF

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	6
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 4x10b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	8-UDFN Exposed Pad
Supplier Device Package	8-UDFN (3x3)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic12f1822t-i-rf

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

1.0 DEVICE OVERVIEW

The PIC12(L)F1822/16(L)F1823 are described within this data sheet. They are available in 8/14 pin packages. Figure 1-1 shows a block diagram of the PIC12(L)F1822/16(L)F1823 devices. Tables 1-2 and 1-3 show the pinout descriptions.

Reference Table 1-1 for peripherals available per device.

TABLE 1-1: DEVICE PERIPHERAL SUMMARY

Peripheral		PIC12(L)F1822	PIC16(L)F1823
ADC		•	•
Capacitive Sensing (CP	S) Module	٠	•
Data EEPROM		•	•
Digital-to-Analog Conve	rter (DAC)	•	•
Digital Signal Modulator	•	•	
EUSART	٠	•	
Fixed Voltage Reference	•	•	
SR Latch	•	•	
Capture/Compare/PWM	Modules		
	ECCP1	•	•
Comparators			
	C1	٠	•
	C2		•
Master Synchronous Se	erial Ports		
	•	•	
Timers		_	
	Timer0	٠	•
	Timer1	•	•
	Timer2	•	•

TABLE 3-5: PIC12(L)F1822/16(L)F1823 MEMORY MAP, BANKS 16-23

	BANK 16		BANK 17		BANK 18		BANK 19		BANK 20		BANK 21		BANK 22		BANK 23
800h	INDF0	880h	INDF0	900h	INDF0	980h	INDF0	A00h	INDF0	A80h	INDF0	B00h	INDF0	B80h	INDF0
801h	INDF1	881h	INDF1	901h	INDF1	981h	INDF1	A01h	INDF1	A81h	INDF1	B01h	INDF1	B81h	INDF1
802h	PCL	882h	PCL	902h	PCL	982h	PCL	A02h	PCL	A82h	PCL	B02h	PCL	B82h	PCL
803h	STATUS	883h	STATUS	903h	STATUS	983h	STATUS	A03h	STATUS	A83h	STATUS	B03h	STATUS	B83h	STATUS
804h	FSR0L	884h	FSR0L	904h	FSR0L	984h	FSR0L	A04h	FSR0L	A84h	FSR0L	B04h	FSR0L	B84h	FSR0L
805h	FSR0H	885h	FSR0H	905h	FSR0H	985h	FSR0H	A05h	FSR0H	A85h	FSR0H	B05h	FSR0H	B85h	FSR0H
806h	FSR1L	886h	FSR1L	906h	FSR1L	986h	FSR1L	A06h	FSR1L	A86h	FSR1L	B06h	FSR1L	B86h	FSR1L
807h	FSR1H	887h	FSR1H	907h	FSR1H	987h	FSR1H	A07h	FSR1H	A87h	FSR1H	B07h	FSR1H	B87h	FSR1H
808h	BSR	888h	BSR	908h	BSR	988h	BSR	A08h	BSR	A88h	BSR	B08h	BSR	B88h	BSR
809h	WREG	889h	WREG	909h	WREG	989h	WREG	A09h	WREG	A89h	WREG	B09h	WREG	B89h	WREG
80Ah	PCLATH	88Ah	PCLATH	90Ah	PCLATH	98Ah	PCLATH	A0Ah	PCLATH	A8Ah	PCLATH	B0Ah	PCLATH	B8Ah	PCLATH
80Bh	INTCON	88Bh	INTCON	90Bh	INTCON	98Bh	INTCON	A0Bh	INTCON	A8Bh	INTCON	B0Bh	INTCON	B8Bh	INTCON
80Ch	_	88Ch	—	90Ch	—	98Ch		A0Ch	_	A8Ch	_	B0Ch	_	B8Ch	—
80Dh	—	88Dh		90Dh	_	98Dh	_	A0Dh		A8Dh	_	B0Dh	—	B8Dh	
80Eh	—	88Eh	—	90Eh	—	98Eh	—	A0Eh	—	A8Eh	—	B0Eh	—	B8Eh	—
80Fh	—	88Fh	—	90Fh	—	98Fh		A0Fh	—	A8Fh	_	B0Fh	—	B8Fh	—
810h	—	890h	—	910h	—	990h	_	A10h	—	A90h	_	B10h	—	B90h	—
811h	—	891h	—	911h	—	991h	_	A11h	—	A91h	_	B11h	—	B91h	—
812h	—	892h	—	912h	—	992h	—	A12h	—	A92h	—	B12h	—	B92h	—
813h	—	893h	—	913h		993h		A13h		A93h	—	B13h	—	B93h	—
814h	—	894h	—	914h	—	994h		A14h	—	A94h	_	B14h	—	B94h	—
815h	_	895h	_	915h	_	995h	_	A15h	_	A95h	_	B15h	—	B95h	—
816h	—	896h	—	916h	—	996h	_	A16h	—	A96h	_	B16h	—	B96h	—
817h	—	897h	_	917h		997h		A17h		A97h	_	B17h	—	B97h	
818h	_	898h	_	918h		998h		A18h		A98h	_	B18h	_	B98h	_
819h	_	899h	_	919h	_	999h	_	A19h	_	A99h	_	B19h	_	B99h	—
81Ah	_	89Ah	—	91Ah		99Ah		A1Ah		A9Ah	_	B1Ah	—	B9Ah	—
81Bh	_	89Bh	_	91Bh	_	99Bh	_	A1Bh	_	A9Bh	_	B1Bh	_	B9Bh	_
81Ch	_	89Ch	_	91Ch		99Ch	_	A1Ch	_	A9Ch	—	B1Ch	_	B9Ch	_
81Dh	_	89Dh	_	91Dh		99Dh	_	A1Dh	_	A9Dh	—	B1Dh	_	B9Dh	_
81Eh	_	89Eh	—	91Eh		99Eh		A1Eh		A9Eh	_	B1Eh	—	B9Eh	_
81Fh	—	89Fh	—	91Fh		99Fh	—	A1Fh		A9Fh	_	B1Fh	—	B9Fh	—
820H		6A011		92011		9A011		AZUN		AAUN		B200		BAUN	
	Unimplemented Read as '0'		Unimplemented Read as '0'		Unimplemented Read as '0'		Unimplemented Read as '0'		Unimplemented Read as '0'		Unimplemented Read as '0'		Unimplemented Read as '0'		Unimplemented Read as '0'
86Fh		8EFh		96Fh		9EFh		A6Fh		AEFh		B6Fh		BEFh	
870h		8F0h		970h		9F0h		A70h		AF0h		B70h		BF0h	
	Accesses 70h – 7Fh		Accesses 70h – 7Fh		Accesses 70h – 7Fh		Accesses 70h – 7Fh		Accesses 70h – 7Fh		Accesses 70h – 7Fh		Accesses 70h – 7Fh		Accesses 70h – 7Fh
87Fh		8FFh		97Fh		9FFh		A7Fh		AFFh		B7Fh		BFFh	

Legend: = Unimplemented data memory locations, read as '0'.

PIC12(L)F1822/16(L)F1823

			•					,			
Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
Bank 3	1										
F80h ⁽¹⁾	INDF0	Addressing to (not a physic	his location us al register)	es contents of	FSR0H/FSR0)L to address	data memor	у		xxxx xxxx	XXXX XXXX
F81h ⁽¹⁾	INDF1	Addressing to (not a physic	xxxx xxxx	xxxx xxxx							
F82h ⁽¹⁾	PCL	Program Cou	gram Counter (PC) Least Significant Byte								
F83h ⁽¹⁾	STATUS	_	_	_	TO	PD	Z	DC	С	1 1000	q quuu
F84h ⁽¹⁾	FSR0L	Indirect Data	Memory Addr	ess 0 Low Poi	nter					0000 0000	uuuu uuuu
F85h ⁽¹⁾	FSR0H	Indirect Data	Memory Addr	ess 0 High Po	inter					0000 0000	0000 0000
F86h ⁽¹⁾	FSR1L Indirect Data Memory Address 1 Low Pointer									0000 0000	uuuu uuuu
F87h ⁽¹⁾	FSR1H	Indirect Data	Memory Addr	ess 1 High Po	inter					0000 0000	0000 0000
F88h ⁽¹⁾	BSR	_	_	_			BSR<4:0>			0 0000	0 0000
F89h ⁽¹⁾	WREG	Working Reg	ister							0000 0000	uuuu uuuu
F8Ah ⁽¹⁾	PCLATH	_	Write Buffer	for the upper 7	bits of the Pro	ogram Counte	er			-000 0000	-000 0000
F8Bh ⁽¹⁾	INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	0000 000x	0000 000u
F8Ch	-	Unimplemented								-	-
FE3h											
FE4h	STATUS_ SHAD	—	_	-	-	-	Z_SHAD	DC_SHAD	C_SHAD	xxx	uuu
FE5h	WREG_ SHAD	Working Reg	ister Shadow						I	0000 0000	uuuu uuuu
FE6h	BSR_ SHAD	-	-	-	Bank Select	Register Sha	dow			x xxxx	u uuuu
FE7h	PCLATH_ SHAD	_	Program Cou	unter Latch Hig	h Register Sh	nadow				-xxx xxxx	uuuu uuuu
FE8h	FSR0L_ SHAD	Indirect Data	Memory Addr	ess 0 Low Poi	nter Shadow					xxxx xxxx	uuuu uuuu
FE9h	FSR0H_ SHAD	Indirect Data	Memory Addr	ess 0 High Po	inter Shadow					xxxx xxxx	uuuu uuuu
FEAh	FSR1L_ SHAD	Indirect Data	Memory Addr	ess 1 Low Poi	nter Shadow					xxxx xxxx	uuuu uuuu
FEBh	FSR1H_ SHAD	Indirect Data	Memory Addr	ess 1 High Po	inter Shadow					xxxx xxxx	uuuu uuuu
FECh	_	Unimplemen	ted							_	_
FEDh	STKPTR	_	_	_	Current Stac	k pointer				1 1111	1 1111
FEEh	TOSL	Top-of-Stack	Low byte		-					xxxx xxxx	uuuu uuuu
FEFh	TOSH	-	Top-of-Stack	High byte						-xxx xxxx	-uuu uuuu

TABLE 3-8 SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, r = reserved. Shaded locations are unimplemented, read as '0'. Legend:

These registers can be addressed from any bank.

1:

Note

2: PIC16(L)F1823 only.

Unimplemented. Read as '1'. 3:

PIC12(L)F1822 only. 4:

4.2 Code Protection

Code protection allows the device to be protected from unauthorized access. Program memory protection and data EEPROM protection are controlled independently. Internal access to the program memory and data EEPROM are unaffected by any code protection setting.

4.2.1 PROGRAM MEMORY PROTECTION

The entire program memory space is protected from external reads and writes by the \overline{CP} bit in Configuration Word 1. When $\overline{CP} = 0$, external reads and writes of program memory are inhibited and a read will return all '0's. The CPU can continue to read program memory, regardless of the protection bit settings. Writing the program memory is dependent upon the write protection setting. See **Section 4.3** "Write **Protection**" for more information.

4.2.2 DATA EEPROM PROTECTION

The entire data EEPROM is protected from external reads and writes by the CPD bit. When CPD = 0, external reads and writes of data EEPROM are inhibited. The CPU can continue to read and write data EEPROM regardless of the protection bit settings.

4.3 Write Protection

Write protection allows the device to be protected from unintended self-writes. Applications, such as bootloader software, can be protected while allowing other regions of the program memory to be modified.

The WRT<1:0> bits in Configuration Word 2 define the size of the program memory block that is protected.

4.4 User ID

Four memory locations (8000h-8003h) are designated as ID locations where the user can store checksum or other code identification numbers. These locations are readable and writable during normal execution. See **Section 11.5 "User ID, Device ID and Configuration Word Access"** for more information on accessing these memory locations. For more information on checksum calculation, see the "*PIC16F/LF1826/27/PIC12F/LF1822 Memory Programming Specification*" (DS41390).

5.2.1.5 TIMER1 Oscillator

The Timer1 Oscillator is a separate crystal oscillator that is associated with the Timer1 peripheral. It is optimized for timekeeping operations with a 32.768 kHz crystal connected between the T1OSO and T1OSI device pins.

The Timer1 Oscillator can be used as an alternate system clock source and can be selected during run-time using clock switching. Refer to **Section 5.3** "**Clock Switching**" for more information.

FIGURE 5-5: QUARTZ CRYSTAL OPERATION (TIMER1 OSCILLATOR)



- Note 1: Quartz crystal characteristics vary according to type, package and manufacturer. The user should consult the manufacturer data sheets for specifications and recommended application.
 - 2: Always verify oscillator performance over the VDD and temperature range that is expected for the application.
 - **3:** For oscillator design assistance, reference the following Microchip Applications Notes:
 - AN826, "Crystal Oscillator Basics and Crystal Selection for rfPIC[®] and PIC[®] Devices" (DS00826)
 - AN849, "Basic PIC[®] Oscillator Design" (DS00849)
 - AN943, "Practical PIC[®] Oscillator Analysis and Design" (DS00943)
 - AN949, "Making Your Oscillator Work" (DS00949)
 - TB097, "Interfacing a Micro Crystal MS1V-T1K 32.768 kHz Tuning Fork Crystal to a PIC16F690/SS" (DS91097)
 - AN1288, "Design Practices for Low-Power External Oscillators" (DS01288)

5.2.1.6 External RC Mode

The external Resistor-Capacitor (RC) modes support the use of an external RC circuit. This allows the designer maximum flexibility in frequency choice while keeping costs to a minimum when clock accuracy is not required.

The RC circuit connects to OSC1. OSC2/CLKOUT is available for general purpose I/O or CLKOUT. The function of the OSC2/CLKOUT pin is determined by the state of the CLKOUTEN bit in Configuration Word 1.

Figure 5-6 shows the external RC mode connections.





The RC oscillator frequency is a function of the supply voltage, the resistor (REXT) and capacitor (CEXT) values and the operating temperature. Other factors affecting the oscillator frequency are:

- threshold voltage variation
- component tolerances
- · packaging variations in capacitance

The user also needs to take into account variation due to tolerance of external RC components used.

6.0 REFERENCE CLOCK MODULE

The reference clock module provides the ability to send a divided clock to the clock output pin of the device (CLKR) and provide a secondary internal clock source to the modulator module. This module is available in all oscillator configurations and allows the user to select a greater range of clock sub-multiples to drive external devices in the application. The reference clock module includes the following features:

- System clock is the source
- Available in all oscillator configurations
- Programmable clock divider
- Output enable to a port pin
- Selectable duty cycle
- Slew rate control

The reference clock module is controlled by the CLKRCON register (Register 6-1) and is enabled when setting the CLKREN bit. To output the divided clock signal to the CLKR port pin, the CLKROE bit must be set. The CLKRDIV<2:0> bits enable the selection of eight different clock divider options. The CLKRDC<1:0> bits can be used to modify the duty cycle of the output clock⁽¹⁾. The CLKRSLR bit controls slew rate limiting.

Note 1: If the base clock rate is selected without a divider, the output clock will always have a duty cycle equal to that of the source clock, unless a 0% duty cycle is selected. If the clock divider is set to base clock/2, then 25% and 75% duty cycle accuracy will be dependent upon the source clock.

For information on using the reference clock output with the modulator module, see **Section 23.0 "Data Signal Modulator"**.

6.1 Slew Rate

The slew rate limitation on the output port pin can be disabled. The Slew Rate limitation can be removed by clearing the CLKRSLR bit in the CLKRCON register.

6.2 Effects of a Reset

Upon any device Reset, the reference clock module is disabled. The user's firmware is responsible for initializing the module before enabling the output. The registers are reset to their default values.

6.3 Conflicts with the CLKR pin

There are two cases when the reference clock output signal cannot be output to the CLKR pin, if:

- LP, XT or HS oscillator mode is selected.
- CLKOUT function is enabled.

Even if either of these cases are true, the module can still be enabled and the reference clock signal may be used in conjunction with the modulator module.

6.3.1 OSCILLATOR MODES

If LP, XT or HS oscillator modes are selected, the OSC2/CLKR pin must be used as an oscillator input pin and the CLKR output cannot be enabled. See **Section 5.2 "Clock Source Types"** for more information on different oscillator modes.

6.3.2 CLKOUT FUNCTION

The CLKOUT function has a higher priority than the reference clock module. <u>Therefore</u>, if the CLKOUT function is enabled by the CLKOUTEN bit in Configuration Word 1, FOSC/4 will always be output on the port pin. Reference **Section 4.0** "**Device Configuration**" for more information.

6.4 Operation During Sleep

As the reference clock module relies on the system clock as its source, and the system clock is disabled in Sleep, the module does not function in Sleep, even if an external clock source or the Timer1 clock source is configured as the system clock. The module outputs will remain in their current state until the device exits Sleep.

7.1 Power-on Reset (POR)

The POR circuit holds the device in Reset until VDD has reached an acceptable level for minimum operation. Slow rising VDD, fast operating speeds or analog performance may require greater than minimum VDD. The PWRT, BOR or MCLR features can be used to extend the start-up period until all device operation conditions have been met.

7.1.1 POWER-UP TIMER (PWRT)

The Power-up Timer provides a nominal 64 ms timeout on POR or Brown-out Reset.

The device is held in Reset as long as PWRT is active. The PWRT delay allows additional time for the VDD to rise to an acceptable level. The Power-up Timer is enabled by clearing the PWRTE bit in Configuration Word 1.

The Power-up Timer starts after the release of the POR and BOR.

For additional information, refer to Application Note AN607, *"Power-up Trouble Shooting"* (DS00607).

7.2 Brown-Out Reset (BOR)

The BOR circuit holds the device in Reset when VDD reaches a selectable minimum level. Between the POR and BOR, complete voltage range coverage for execution protection can be implemented.

The Brown-out Reset module has four operating modes controlled by the BOREN<1:0> bits in Configuration Word 1. The four operating modes are:

- · BOR is always on
- · BOR is off when in Sleep
- · BOR is controlled by software
- · BOR is always off

Refer to Table 7-1 for more information.

The Brown-out Reset voltage level is selectable by configuring the BORV bit in Configuration Word 2.

A VDD noise rejection filter prevents the BOR from triggering on small events. If VDD falls below VBOR for a duration greater than parameter TBORDC, the device will reset. See Figure 7-3 for more information.

BOREN Config bits	SBOREN	Device Mode	BOR Mode	Device Operation upon release of POR	Device Operation upon wake- up from Sleep
BOR_ON (11)	х	Х	Active	Waits for B	OR ready ⁽¹⁾
BOR_NSLEEP (10)	х	Awake	Active		
BOR_NSLEEP (10)	Х	Sleep	Disabled	vvaits for i	BOR ready
BOR_SBOREN (01)	1	х	Active	Begins in	nmediately
BOR_SBOREN (01)	0	х	Disabled	Begins in	nmediately
BOR_OFF (00)	х	Х	Disabled	Begins in	nmediately

TABLE 7-1:BOR OPERATING MODES

Note 1: In these specific cases, "Release of POR" and "Wake-up from Sleep", there is no delay in start-up. The BOR ready flag, (BORRDY = 1), will be set before the CPU is ready to execute instructions because the BOR circuit is forced on by the BOREN<1:0> bits.

7.2.1 BOR IS ALWAYS ON

When the BOREN bits of Configuration Word 1 are set to '11', the BOR is always on. The device start-up will be delayed until the BOR is ready and VDD is higher than the BOR threshold.

BOR protection is active during Sleep. The BOR does not delay wake-up from Sleep.

7.2.2 BOR IS OFF IN SLEEP

When the BOREN bits of Configuration Word 1 are set to '10', the BOR is on, except in Sleep. The device start-up will be delayed until the BOR is ready and VDD is higher than the BOR threshold.

BOR protection is not active during Sleep. The device wake-up will be delayed until the BOR is ready.

12.2.2 PORTA FUNCTIONS AND OUTPUT PRIORITIES

Each PORTA pin is multiplexed with other functions. The pins, their combined functions and their output priorities are briefly described here. For additional information, refer to the appropriate section in this data sheet.

When multiple outputs are enabled, the actual pin control goes to the peripheral with the lowest number in the following lists.

Analog input functions, such as ADC, comparator and CapSense inputs, are not shown in the priority lists. These inputs are active when the I/O pin is set for Analog mode using the ANSELx registers. Digital output functions may control the pin when it is in Analog mode with the priority shown below.

<u>RA0</u>

- 1. ICSPDAT
- 2. ICDDAT
- 3. DACOUT (DAC)
- 4. MDOUT (PIC12(L)F1822 only)
- 5. TX/CK (EUSART)
- 6. SDO (PIC12(L)F1822 only)
- 7. P1B (PIC12(L)F1822 only)

<u>RA1</u>

- 1. ICSPCLK
- 2. ICDCLK
- 3. SCL (PIC12(L)F1822 only)
- 4. RX/DT (EUSART)
- 5. SCK (PIC12(L)F1822 only)

<u>RA2</u>

- 1. SRQ
- 2. C1OUT (Comparator)
- 3. SDA (PIC12(L)F1822 only)
- 4. CCP1/P1A (PIC12(L)F1822 only)

<u>RA3</u>

No output priorities. Input only pin.

<u>RA4</u>

- 1. OSC2
- 2. CLKOUT
- 3. T1OSO (Timer1 Oscillator)
- 4. CLKR
- 5. TX/CK (PIC12(L)F1822 only)
- 6. SDO
- 7. P1B (PIC12(L)F1822 only)

<u>RA5</u>

1. OSC1

- 2. T1OSI (Timer1 Oscillator)
- 3. SRNQ (PIC12(L)F1822 only)
- 4. RX/DT (PIC12(L)F1822 only)
- 5. CCP1/P1A (PIC12(L)F1822 only)

21.7 **Timer1 Interrupt**

The Timer1 register pair (TMR1H:TMR1L) increments to FFFFh and rolls over to 0000h. When Timer1 rolls over, the Timer1 interrupt flag bit of the PIR1 register is set. To enable the interrupt on rollover, you must set these bits:

- TMR1ON bit of the T1CON register
- TMR1IE bit of the PIE1 register
- · PEIE bit of the INTCON register
- · GIE bit of the INTCON register

The interrupt is cleared by clearing the TMR1IF bit in the Interrupt Service Routine.

The TMR1H:TMR1L register pair and the Note: TMR1IF bit should be cleared before enabling interrupts.

21.8 **Timer1 Operation During Sleep**

Timer1 can only operate during Sleep when setup in Asynchronous Counter mode. In this mode, an external crystal or clock source can be used to increment the counter. To set up the timer to wake the device:

- TMR1ON bit of the T1CON register must be set
- TMR1IE bit of the PIE1 register must be set
- PEIE bit of the INTCON register must be set
- T1SYNC bit of the T1CON register must be set
- TMR1CS bits of the T1CON register must be configured
- T1OSCEN bit of the T1CON register must be configured

The device will wake-up on an overflow and execute the next instructions. If the GIE bit of the INTCON register is set, the device will call the Interrupt Service Routine.

Timer1 oscillator will continue to operate in Sleep regardless of the $\overline{\text{T1SYNC}}$ bit setting.

21.9 ECCP/CCP Capture/Compare Time Base

The CCP1 module uses the TMR1H:TMR1L register pair as the time base when operating in Capture or Compare mode.

In Capture mode, the value in the TMR1H:TMR1L register pair is copied into the CCPR1H:CCPR1L register pair on a configured event.

In Compare mode, an event is triggered when the value CCPR1H:CCPR1L register pair matches the value in the TMR1H:TMR1L register pair. This event can be a Special Event Trigger.

For more information, see Section 24.0 "Capture/Compare/PWM Modules".

21.10 ECCP/CCP Special Event Trigger

When any of the CCP's are configured to trigger a special event, the trigger will clear the TMR1H:TMR1L register pair. This special event does not cause a Timer1 interrupt. The CCP module may still be configured to generate a CCP interrupt.

In this mode of operation, the CCPR1H:CCPR1L register pair becomes the period register for Timer1.

Timer1 should be synchronized and Fosc/4 should be selected as the clock source in order to utilize the Special Event Trigger. Asynchronous operation of Timer1 can cause a Special Event Trigger to be missed.

In the event that a write to TMR1H or TMR1L coincides with a Special Event Trigger from the CCP, the write will take precedence.

For more information, see Section 16.2.5 "Special Event Trigger".



FIGURE 21-2: TIMER1 INCREMENTING EDGE

PIC12(L)F1822/16(L)F1823

R/W-0/0	R/W-0/0	R/W-1/1	R/W-0/0	R-0/0	U-0	U-0	R/W-0/0
MDEN	MDOE	MDSLR	MDOPOL	MDOUT		_	MDBIT
bit 7							bit 0
Legend:							
R = Readab	le bit	W = Writable	bit	U = Unimplei	mented bit, read	1 as '0'	
u = Bit is un	changed	x = Bit is unki	nown	-n/n = Value	at POR and BO	R/Value at all	other Resets
'1' = Bit is se	et	'0' = Bit is cle	ared				
bit 7	MDEN: Modu	llator Module E	nable bit				
	1 = Modulato	or module is en	abled and mix	ing input signa	als		
		or module is dis					
bit 6	MDOE: Modu	Ilator Module F	'in Output Ena	ible bit			
	1 = Modulato	or pin output er	abled				
bit 5		N IT Pin Slew	Rate Limiting	hit			
DIL J		nin slew rate li	miting enabled	1			
	0 = MDOUT	pin slew rate li	miting disable	d			
bit 4	MDOPOL: M	odulator Outpu	t Polarity Sele	ct bit			
	1 = Modulato	or output signal	is inverted				
	0 = Modulato	or output signal	is not invertee	b			
bit 3	MDOUT: Mod	lulator Output I	oit				
	Displays the o	current output	alue of the M	odulator modu	le. ⁽¹⁾		
bit 2-1	Unimplemen	ted: Read as '	0'				
bit 0	MDBIT: Allow	vs software to r	nanually set m	odulation sou	rce input to mod	dule ⁽²⁾	
	1 = Modulato	or uses High Ca	arrier source				
	0 = Modulato	or uses Low Ca	Irrier source				
Note 1: T	he modulated our egister bit, the bit	tput frequency value may not	can be greate be valid for hi	r and asynchro gher speed mo	onous from the odulator or carri	clock that upd er signals.	ates this

REGISTER 23-1: MDCON: MODULATION CONTROL REGISTER

2: MDBIT must be selected as the modulation source in the MDSRC register for this operation.

24.4.2.1 Direction Change in Full-Bridge Mode

In the Full-Bridge mode, the P1M1 bit in the CCP1CON register allows users to control the forward/reverse direction. When the application firmware changes this direction control bit, the module will change to the new direction on the next PWM cycle.

A direction change is initiated in software by changing the P1M1 bit of the CCP1CON register. The following sequence occurs four Timer cycles prior to the end of the current PWM period:

- The modulated outputs (P1B and P1D) are placed in their inactive state.
- The associated unmodulated outputs (P1A and P1C) are switched to drive in the opposite direction.
- PWM modulation resumes at the beginning of the next period.

See Figure 24-12 for an illustration of this sequence.

The Full-Bridge mode does not provide dead-band delay. As one output is modulated at a time, dead-band delay is generally not required. There is a situation where dead-band delay is required. This situation occurs when both of the following conditions are true:

- 1. The direction of the PWM output changes when the duty cycle of the output is at or near 100%.
- 2. The turn-off time of the power switch, including the power device and driver circuit, is greater than the turn-on time.

Figure 24-13 shows an example of the PWM direction changing from forward to reverse, at a near 100% duty cycle. In this example, at time t1, the output P1A and P1D become inactive, while output P1C becomes active. Since the turn off time of the power devices is longer than the turn on time, a shoot-through current will flow through power devices QC and QD (see Figure 24-10) for the duration of 't'. The same phenomenon will occur to power devices QA and QB for PWM direction change from reverse to forward.

If changing PWM direction at high duty cycle is required for an application, two possible solutions for eliminating the shoot-through current are:

- 1. Reduce PWM duty cycle for one PWM period before changing directions.
- 2. Use switch drivers that can drive the switches off faster than they can drive them on.

Other options to prevent shoot-through current may exist.

FIGURE 24-12: EXAMPLE OF PWM DIRECTION CHANGE



2: When changing directions, the P1A and P1C signals switch before the end of the current PWM cycle. The modulated P1B and P1D signals are inactive at this time. The length of this time is four Timer counts.

24.4.3 ENHANCED PWM AUTO-SHUTDOWN MODE

The PWM mode supports an Auto-Shutdown mode that will disable the PWM outputs when an external shutdown event occurs. Auto-Shutdown mode places the PWM output pins into a predetermined state. This mode is used to help prevent the PWM from damaging the application.

The auto-shutdown sources are selected using the CCP1AS<2:0> bits of the CCP1AS register. A shutdown event may be generated by:

- A logic '0' on the FLT0 pin
- A logic '1' on a Comparator (C1) output

A shutdown condition is indicated by the CCP1ASE (Auto-Shutdown Event Status) bit of the CCP1AS register. If the bit is a '0', the PWM pins are operating normally. If the bit is a '1', the PWM outputs are in the shutdown state.

When a shutdown event occurs, two things happen:

The CCP1ASE bit is set to '1'. The CCP1ASE will remain set until cleared in firmware or an auto-restart occurs (see **Section 24.4.4 "Auto-Restart Mode"**).

The enabled PWM pins are asynchronously placed in their shutdown states. The PWM output pins are grouped into pairs [P1A/P1C] and [P1B/P1D]. The state of each pin pair is determined by the PSS1AC and PSS1BD bits of the CCP1AS register. Each pin pair may be placed into one of three states:

- Drive logic '1'
- Drive logic '0'
- Tri-state (high-impedance)

- Note 1: The auto-shutdown condition is a levelbased signal, not an edge-based signal. As long as the level is present, the autoshutdown will persist.
 - 2: Writing to the CCP1ASE bit is disabled while an auto-shutdown condition persists.
 - 3: Once the auto-shutdown condition has been removed and the PWM restarted (either through firmware or auto-restart) the PWM signal will always restart at the beginning of the next PWM period.
 - 4: Prior to an auto-shutdown event caused by a comparator output or FLT0 pin event, a software shutdown can be triggered in firmware by setting the CCP1ASE bit of the CCP1AS register to '1'. The autorestart feature tracks the active status of a shutdown caused by a comparator output or FLT0 pin event only. If it is enabled at this time, it will immediately clear this bit and restart the ECCP module at the beginning of the next PWM period.

FIGURE 24-14: PWM AUTO-SHUTDOWN WITH	I FIRMWARE RESTART (P1RSEN = 0)
FIGURE 24-14: PWM AUTO-SHUTDOWN WITH	$\mathbf{FIRMWARE\ RESTART\ (P1RSEN=0)}$



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The MSSP1 consists of a transmit/receive shift register (SSP1SR) and a buffer register (SSP1BUF). The SSP1SR shifts the data in and out of the device. MSb first. The SSP1BUF holds the data that was written to the SSP1SR until the received data is ready. Once the eight bits of data have been received, that byte is moved to the SSP1BUF register. Then, the Buffer Full Detect bit, BF of the SSP1STAT register, and the interrupt flag bit, SSP1IF, are set. This double-buffering of the received data (SSP1BUF) allows the next byte to start reception before reading the data that was just received. Any write to the SSP1BUF register during transmission/reception of data will be ignored and the write collision detect bit, WCOL, of the SSP1CON1 register, will be set. User software must clear the WCOL bit to allow the following write(s) to the SSP1BUF register to complete successfully.

When the application software is expecting to receive valid data, the SSP1BUF should be read before the next byte of data to transfer is written to the SSP1BUF. The Buffer Full bit, BF of the SSP1STAT register, indicates when SSP1BUF has been loaded with the received data (transmission is complete). When the SSP1BUF is read, the BF bit is cleared. This data may be irrelevant if the SP1 is only a transmitter. Generally, the MSSP1 interrupt is used to determine when the transmission/reception has completed. If the interrupt method is not going to be used, then software polling can be done to ensure that a write collision does not occur.

The SSP1SR is not directly readable or writable and can only be accessed by addressing the SSP1BUF register. Additionally, the SSP1STAT register indicates the various Status conditions.



FIGURE 25-5: SPI MASTER/SLAVE CONNECTION

PIC12(L)F1822/16(L)F1823

25.6.13.1 Bus Collision During a Start Condition

During a Start condition, a bus collision occurs if:

- a) SDA or SCL are sampled low at the beginning of the Start condition (Figure 25-33).
- b) SCL is sampled low before SDA is asserted low (Figure 25-34).

During a Start condition, both the SDA and the SCL pins are monitored.

If the SDA pin is already low, or the SCL pin is already low, then all of the following occur:

- · the Start condition is aborted,
- the BCL1IF flag is set and
- the MSSP1 module is reset to its Idle state (Figure 25-33).

The Start condition begins with the SDA and SCL pins deasserted. When the SDA pin is sampled high, the Baud Rate Generator is loaded and counts down. If the SCL pin is sampled low while SDA is high, a bus collision occurs because it is assumed that another master is attempting to drive a data '1' during the Start condition.

If the SDA pin is sampled low during this count, the BRG is reset and the SDA line is asserted early (Figure 25-35). If, however, a '1' is sampled on the SDA pin, the SDA pin is asserted low at the end of the BRG count. The Baud Rate Generator is then reloaded and counts down to zero; if the SCL pin is sampled as '0' during this time, a bus collision does not occur. At the end of the BRG count, the SCL pin is asserted low.

Note: The reason that bus collision is not a factor during a Start condition is that no two bus masters can assert a Start condition at the exact same time. Therefore, one master will always assert SDA before the other. This condition does not cause a bus collision because the two masters must be allowed to arbitrate the first address following the Start condition. If the address is the same, arbitration must be allowed to continue into the data portion, Repeated Start or Stop conditions.





25.7 BAUD RATE GENERATOR

The MSSP1 module has a Baud Rate Generator available for clock generation in both I²C and SPI Master modes. The Baud Rate Generator (BRG) reload value is placed in the SSP1ADD register (Register 25-6). When a write occurs to SSP1BUF, the Baud Rate Generator will automatically begin counting down.

Once the given operation is complete, the internal clock will automatically stop counting and the clock pin will remain in its last state.

An internal signal "Reload" in Figure 25-40 triggers the value from SSP1ADD to be loaded into the BRG counter. This occurs twice for each oscillation of the

module clock line. The logic dictating when the reload signal is asserted depends on the mode the MSSP1 is being operated in.

Table 25-4 demonstrates clock rates based on instruction cycles and the BRG value loaded into SSP1ADD.

EQUATION 25-1:

$$FCLOCK = \frac{FOSC}{(SSPxADD + 1)(4)}$$

FIGURE 25-40: BAUD RATE GENERATOR BLOCK DIAGRAM



Note: Values of 0x00, 0x01 and 0x02 are not valid for SSP1ADD when used as a Baud Rate Generator for I²C. This is an implementation limitation.

TABLE 25-4: MSSP1 CLOCK RATE W/BRG

Fosc	Fcy	BRG Value	FcLock (2 Rollovers of BRG)
32 MHz	8 MHz	13h	400 kHz
32 MHz	8 MHz	19h	308 kHz
32 MHz	8 MHz	4Fh	100 kHz
16 MHz	4 MHz	09h	400 kHz
16 MHz	4 MHz	0Ch	308 kHz
16 MHz	4 MHz	27h	100 kHz
4 MHz	1 MHz	09h	100 kHz

Note 1: Refer to the I/O port electrical and timing specifications in Table 30-4 and Figure 30-7 to ensure the system is designed to support the I/O requirements.

26.1 EUSART Asynchronous Mode

The EUSART transmits and receives data using the standard non-return-to-zero (NRZ) format. NRZ is implemented with two levels: a VOH mark state which represents a '1' data bit, and a VOL space state which represents a '0' data bit. NRZ refers to the fact that consecutively transmitted data bits of the same value stay at the output level of that bit without returning to a neutral level between each bit transmission. An NRZ transmission port idles in the mark state. Each character transmission consists of one Start bit followed by eight or nine data bits and is always terminated by one or more Stop bits. The Start bit is always a space and the Stop bits are always marks. The most common data format is eight bits. Each transmitted bit persists for a period of 1/(Baud Rate). An on-chip dedicated 8-bit/16-bit Baud Rate Generator is used to derive standard baud rate frequencies from the system oscillator. See Table 26-5 for examples of baud rate configurations.

The EUSART transmits and receives the LSb first. The EUSART's transmitter and receiver are functionally independent, but share the same data format and baud rate. Parity is not supported by the hardware, but can be implemented in software and stored as the ninth data bit.

26.1.1 EUSART ASYNCHRONOUS TRANSMITTER

The EUSART transmitter block diagram is shown in Figure 26-1. The heart of the transmitter is the serial Transmit Shift Register (TSR), which is not directly accessible by software. The TSR obtains its data from the transmit buffer, which is the TXREG register.

26.1.1.1 Enabling the Transmitter

The EUSART transmitter is enabled for asynchronous operations by configuring the following three control bits:

- TXEN = 1
- SYNC = 0
- SPEN = 1

All other EUSART control bits are assumed to be in their default state.

Setting the TXEN bit of the TXSTA register enables the transmitter circuitry of the EUSART. Clearing the SYNC bit of the TXSTA register configures the EUSART for asynchronous operation. Setting the SPEN bit of the RCSTA register enables the EUSART and automatically configures the TX/CK I/O pin as an output. If the TX/CK pin is shared with an analog peripheral, the analog I/O function must be disabled by clearing the corresponding ANSEL bit.

Note 1: The TXIF Transmitter Interrupt flag is set when the TXEN enable bit is set.

26.1.1.2 Transmitting Data

A transmission is initiated by writing a character to the TXREG register. If this is the first character, or the previous character has been completely flushed from the TSR, the data in the TXREG is immediately transferred to the TSR register. If the TSR still contains all or part of a previous character, the new character data is held in the TXREG until the Stop bit of the previous character has been transmitted. The pending character in the TXREG is then transferred to the TSR in one TCY immediately following the Stop bit sequence commences immediately following the transfer of the data to the TSR from the TXREG.

26.1.1.3 Transmit Interrupt Flag

The TXIF interrupt flag bit of the PIR1 register is set whenever the EUSART transmitter is enabled and no character is being held for transmission in the TXREG. In other words, the TXIF bit is only clear when the TSR is busy with a character and a new character has been queued for transmission in the TXREG. The TXIF flag bit is not cleared immediately upon writing TXREG. TXIF becomes valid in the second instruction cycle following the write execution. Polling TXIF immediately following the TXREG write will return invalid results. The TXIF bit is read-only, it cannot be set or cleared by software.

The TXIF interrupt can be enabled by setting the TXIE interrupt enable bit of the PIE1 register. However, the TXIF flag bit will be set whenever the TXREG is empty, regardless of the state of TXIE enable bit.

To use interrupts when transmitting data, set the TXIE bit only when there is more data to send. Clear the TXIE interrupt enable bit upon writing the last character of the transmission to the TXREG.

26.3.2 AUTO-BAUD OVERFLOW

During the course of automatic baud detection, the ABDOVF bit of the BAUDCON register will be set if the baud rate counter overflows before the fifth rising edge is detected on the RX pin. The ABDOVF bit indicates that the counter has exceeded the maximum count that can fit in the 16 bits of the SPBRGH:SPBRGL register pair. After the ABDOVF has been set, the counter continues to count until the fifth rising edge is detected on the RX pin. Upon detecting the fifth RX edge, the hardware will set the RCIF interrupt flag and clear the ABDEN bit of the BAUDCON register. The RCIF flag can be subsequently cleared by reading the RCREG register. The ABDOVF flag of the BAUDCON register can be cleared by software directly.

To terminate the auto-baud process before the RCIF flag is set, clear the ABDEN bit then clear the ABDOVF bit of the BAUDCON register. The ABDOVF bit will remain set if the ABDEN bit is not cleared first.

26.3.3 AUTO-WAKE-UP ON BREAK

During Sleep mode, all clocks to the EUSART are suspended. Because of this, the Baud Rate Generator is inactive and a proper character reception cannot be performed. The Auto-Wake-up feature allows the controller to wake-up due to activity on the RX/DT line. This feature is available only in Asynchronous mode.

The Auto-Wake-up feature is enabled by setting the WUE bit of the BAUDCON register. Once set, the normal receive sequence on RX/DT is disabled, and the EUSART remains in an Idle state, monitoring for a wake-up event independent of the CPU mode. A wake-up event consists of a high-to-low transition on the RX/DT line. (This coincides with the start of a Sync Break or a wake-up signal character for the LIN protocol.)

The EUSART module generates an RCIF interrupt coincident with the wake-up event. The interrupt is generated synchronously to the Q clocks in normal CPU operating modes (Figure 26-7), and asynchronously if the device is in Sleep mode (Figure 26-8). The interrupt condition is cleared by reading the RCREG register.

The WUE bit is automatically cleared by the low-to-high transition on the RX line at the end of the Break. This signals to the user that the Break event is over. At this point, the EUSART module is in Idle mode waiting to receive the next character.

26.3.3.1 Special Considerations

Break Character

To avoid character errors or character fragments during a wake-up event, the wake-up character must be all zeros.

When the wake-up is enabled the function works independent of the low time on the data stream. If the WUE bit is set and a valid non-zero character is received, the low time from the Start bit to the first rising edge will be interpreted as the wake-up event. The remaining bits in the character will be received as a fragmented character and subsequent characters can result in framing or overrun errors.

Therefore, the initial character in the transmission must be all '0's. This must be 10 or more bit times, 13-bit times recommended for LIN bus, or any number of bit times for standard RS-232 devices.

Oscillator Start-up Time

Oscillator start-up time must be considered, especially in applications using oscillators with longer start-up intervals (i.e., LP, XT or HS/PLL mode). The Sync Break (or wake-up signal) character must be of sufficient length, and be followed by a sufficient interval, to allow enough time for the selected oscillator to start and provide proper initialization of the EUSART.

WUE Bit

The wake-up event causes a receive interrupt by setting the RCIF bit. The WUE bit is cleared in hardware by a rising edge on RX/DT. The interrupt condition is then cleared in software by reading the RCREG register and discarding its contents.

To ensure that no actual data is lost, check the RCIDL bit to verify that a receive operation is not in process before setting the WUE bit. If a receive operation is not occurring, the WUE bit may then be set just prior to entering the Sleep mode.

26.3.4 BREAK CHARACTER SEQUENCE

The EUSART module has the capability of sending the special Break character sequences that are required by the LIN bus standard. A Break character consists of a Start bit, followed by 12 '0' bits and a Stop bit.

To send a Break character, set the SENDB and TXEN bits of the TXSTA register. The Break character transmission is then initiated by a write to the TXREG. The value of data written to TXREG will be ignored and all '0's will be transmitted.

The SENDB bit is automatically reset by hardware after the corresponding Stop bit is sent. This allows the user to preload the transmit FIFO with the next transmit byte following the Break character (typically, the Sync character in the LIN specification).

The TRMT bit of the TXSTA register indicates when the transmit operation is active or Idle, just as it does during normal transmission. See Figure 26-9 for the timing of the Break character sequence.

Break and Sync Transmit Sequence 26.3.4.1

The following sequence will start a message frame header made up of a Break, followed by an auto-baud Sync byte. This sequence is typical of a LIN bus master.

- 1. Configure the EUSART for the desired mode.
- 2. Set the TXEN and SENDB bits to enable the Break sequence.
- Load the TXREG with a dummy character to 3. initiate transmission (the value is ignored).
- Write '55h' to TXREG to load the Sync character 4 into the transmit FIFO buffer.
- After the Break has been sent, the SENDB bit is 5. reset by hardware and the Sync character is then transmitted.

When the TXREG becomes empty, as indicated by the TXIF, the next data byte can be written to TXREG.

Write to TXREG Dummy Write **BRG** Output (Shift Clock) TX (pin) Start bit bit 0 bit 1 Stop bit Break TXIF bit (Transmit Interrupt Flag) TRMT bit (Transmit Shift Empty Flag) SENDB Sampled Here Auto Cleared SENDB (send Break control bit)

FIGURE 26-9: SEND BREAK CHARACTER SEQUENCE

RECEIVING A BREAK CHARACTER 26.3.5

The Enhanced EUSART module can receive a Break character in two ways.

The first method to detect a Break character uses the FERR bit of the RCSTA register and the Received data as indicated by RCREG. The Baud Rate Generator is assumed to have been initialized to the expected baud rate.

A Break character has been received when;

- RCIF bit is set
- · FERR bit is set
- RCREG = 00h

The second method uses the Auto-Wake-up feature described in Section 26.3.3 "Auto-Wake-up on Break". By enabling this feature, the EUSART will sample the next two transitions on RX/DT, cause an RCIF interrupt, and receive the next data byte followed by another interrupt.

Note that following a Break character, the user will typically want to enable the Auto-Baud Detect feature. For both methods, the user can set the ABDEN bit of the BAUDCON register before placing the EUSART in Sleep mode.

TABLE 30-19: DC CHARACTERISTICS FOR PIC12F1822/16F1823-H (High Temp.)

PIC12F1822/16F1823				Standard Operating Conditions: (unless otherwise stated) Operating Temperature: -40°C \leq TA \leq +150°C for High Temperature					
Param No.	Sym.	Characteristics	Min.	Тур.	Max.	Units	Condition		
D001	Vdd	Supply Voltage	2.5	—	5.5	V	Fosc ≤ 32 MHz (Note 1)		
D002*	Vdr	RAM Data Retention Voltage	2.1	—	5.5	V	Device in Sleep mode		
D003	VADFVR	Fixed Voltage Reference Voltage for ADC	-10	_	8	%	$\begin{array}{l} 1.024V, \ VDD \geq 2.5V \\ 2.048V, \ VDD \geq 2.5V \\ 4.096V, \ VDD \geq 4.75V \end{array}$		
D003A	VCDAFV R	Fixed Voltage Reference Voltage for ADC	-13		9	%	$\begin{array}{l} 1.024 \text{V}, \ \text{VDD} \geq 2.5 \text{V} \\ 2.048 \text{V}, \ \text{VDD} \geq 2.5 \text{V} \\ 4.096 \text{V}, \ \text{VDD} \geq 4.75 \text{V} \end{array}$		

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: PLL required for 32 MHz operation.

8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	MILLIMETERS					
Dimension	MIN	NOM	MAX			
Contact Pitch	E	1.27 BSC				
Contact Pad Spacing	С		5.40			
Contact Pad Width (X8)	X1			0.60		
Contact Pad Length (X8)	Y1			1.55		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A