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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	12
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	14-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	14-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f1823t-i-st

PIC12(L)F1822/16(L)F1823

FIGURE 1: 8-PIN DIAGRAM FOR PIC12(L)F1822

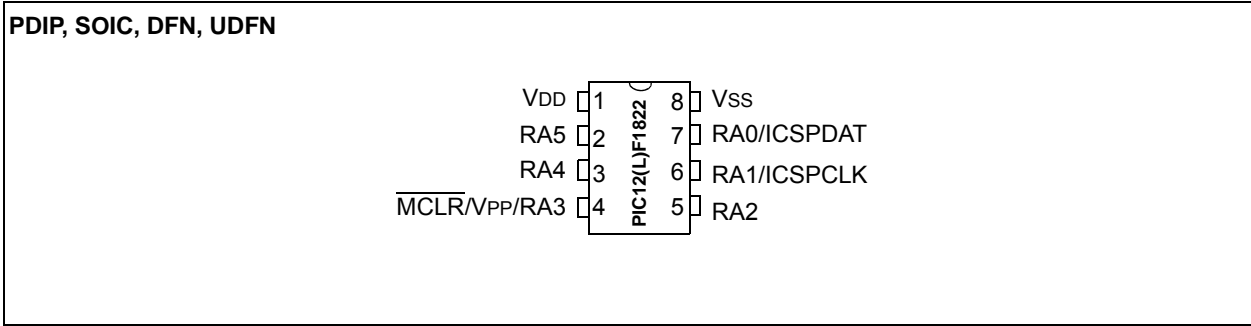


TABLE 2: 8-PIN ALLOCATION TABLE (PIC12(L)F1822)

I/O	8-Pin PDIP/SOIC/DFN/UDFN	A/D	Reference	Cap Sense	Comparator	SR Latch	Timers	ECCP	EUSART	MSSP	Interrupt	Modulator	Pull-up	Basic
RA0	7	AN0	DACOUT	CPS0	C1IN+	—	—	P1B ⁽¹⁾	TX ⁽¹⁾ CK ⁽¹⁾	SDO ⁽¹⁾ SS ⁽¹⁾	IOC	MDOUT	Y	ICSPDAT ICDDAT
RA1	6	AN1	VREF+	CPS1	C1IN0-	SRI	—	—	RX ⁽¹⁾ DT ⁽¹⁾	SCL SCK	IOC	MDMIN	Y	ICSPCLK ICPCLK
RA2	5	AN2	—	CPS2	C1OUT	SRQ	T0CKI	CCP1 ⁽¹⁾ P1A ⁽¹⁾ FLT0	—	SDA SDI	INT/ IOC	MDCIN1	Y	—
RA3	4	—	—	—	—	—	T1G ⁽¹⁾	—	—	SS ⁽¹⁾	IOC	—	Y	MCLR VPP
RA4	3	AN3	—	CPS3	C1IN1-	—	T1G ⁽¹⁾ T1OSO	P1B ⁽¹⁾	TX ⁽¹⁾ CK ⁽¹⁾	SDO ⁽¹⁾	IOC	MDCIN2	Y	OSC2 CLKOUT CLKR
RA5	2	—	—	—	—	SRNQ	T1CKI T1OSI	CCP1 ⁽¹⁾ P1A ⁽¹⁾	RX ⁽¹⁾ DT ⁽¹⁾	—	IOC	—	Y	OSC1 CLKIN
VDD	1	—	—	—	—	—	—	—	—	—	—	—	—	VDD
VSS	8	—	—	—	—	—	—	—	—	—	—	—	—	VSS

Note 1: Pin function is selectable via the APFCON register.

FIGURE 3-7: ACCESSING THE STACK EXAMPLE 4



3.4.2 OVERFLOW/UNDERFLOW RESET

If the `STVREN` bit in Configuration Word 2 is programmed to '1', the device will be reset if the stack is PUSHed beyond the sixteenth level or POPed beyond the first level, setting the appropriate bits (`STKOVF` or `STKUNF`, respectively) in the `PCON` register.

3.5 Indirect Addressing

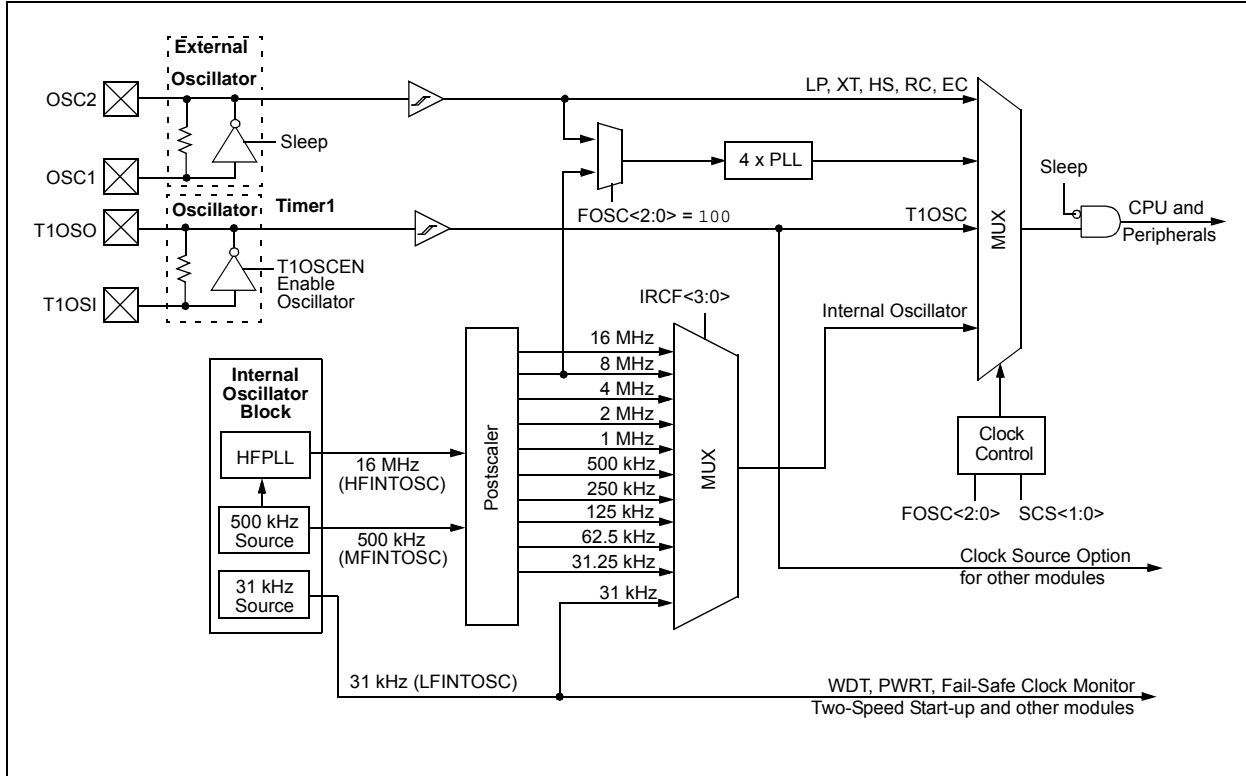
The `INDFn` registers are not physical registers. Any instruction that accesses an `INDFn` register actually accesses the register at the address specified by the File Select Registers (`FSR`). If the `FSRn` address specifies one of the two `INDFn` registers, the read will return '0' and the write will not occur (though Status bits may be affected). The `FSRn` register value is created by the pair `FSRnH` and `FSRnL`.

The `FSR` registers form a 16-bit address that allows an addressing space with 65536 locations. These locations are divided into three memory regions:

- Traditional Data Memory
- Linear Data Memory
- Program Flash Memory

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FIGURE 5-1: SIMPLIFIED PIC® MCU CLOCK SOURCE BLOCK DIAGRAM



PIC12(L)F1822/16(L)F1823

REGISTER 6-1: CLKRCON: REFERENCE CLOCK CONTROL REGISTER

R/W-0/0	R/W-0/0	R/W-1/1	R/W-1/1	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
CLKREN	CLKROE	CLKRSLR	CLKRDC<1:0>	CLKRDIV<2:0>			
bit 7							bit 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7	CLKREN: Reference Clock Module Enable bit 1 = Reference clock module is enabled 0 = Reference clock module is disabled
bit 6	CLKROE: Reference Clock Output Enable bit ⁽³⁾ 1 = Reference clock output is enabled on CLKR pin 0 = Reference clock output disabled on CLKR pin
bit 5	CLKRSLR: Reference Clock Slew Rate Control limiting enable bit 1 = Slew rate limiting is enabled 0 = Slew rate limiting is disabled
bit 4-3	CLKRDC<1:0>: Reference Clock Duty Cycle bits 11 = Clock outputs duty cycle of 75% 10 = Clock outputs duty cycle of 50% 01 = Clock outputs duty cycle of 25% 00 = Clock outputs duty cycle of 0%
bit 2-0	CLKRDIV<2:0> Reference Clock Divider bits 111 = Base clock value divided by 128 110 = Base clock value divided by 64 101 = Base clock value divided by 32 100 = Base clock value divided by 16 011 = Base clock value divided by 8 010 = Base clock value divided by 4 001 = Base clock value divided by 2 ⁽¹⁾ 000 = Base clock value ⁽²⁾

Note 1: In this mode, the 25% and 75% duty cycle accuracy will be dependent on the source clock duty cycle.

2: In this mode, the duty cycle will always be equal to the source clock duty cycle, unless a duty cycle of 0% is selected.

3: To route CLKR to pin, $\overline{\text{CLKOUTEN}}$ of Configuration Word 1 = 1 is required. $\overline{\text{CLKOUTEN}}$ of Configuration Word 1 = 0 will result in $F_{\text{OSC}}/4$. See **Section 6.3 "Conflicts with the CLKR pin"** for details.

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7.1 Power-on Reset (POR)

The POR circuit holds the device in Reset until VDD has reached an acceptable level for minimum operation. Slow rising VDD, fast operating speeds or analog performance may require greater than minimum VDD. The PWRT, BOR or MCLR features can be used to extend the start-up period until all device operation conditions have been met.

7.1.1 POWER-UP TIMER (PWRT)

The Power-up Timer provides a nominal 64 ms time-out on POR or Brown-out Reset.

The device is held in Reset as long as PWRT is active. The PWRT delay allows additional time for the VDD to rise to an acceptable level. The Power-up Timer is enabled by clearing the PWRTE bit in Configuration Word 1.

The Power-up Timer starts after the release of the POR and BOR.

For additional information, refer to Application Note AN607, "Power-up Trouble Shooting" (DS00607).

7.2 Brown-Out Reset (BOR)

The BOR circuit holds the device in Reset when VDD reaches a selectable minimum level. Between the POR and BOR, complete voltage range coverage for execution protection can be implemented.

The Brown-out Reset module has four operating modes controlled by the BOREN<1:0> bits in Configuration Word 1. The four operating modes are:

- BOR is always on
- BOR is off when in Sleep
- BOR is controlled by software
- BOR is always off

Refer to Table 7-1 for more information.

The Brown-out Reset voltage level is selectable by configuring the BORV bit in Configuration Word 2.

A VDD noise rejection filter prevents the BOR from triggering on small events. If VDD falls below VBOR for a duration greater than parameter TBORDC, the device will reset. See Figure 7-3 for more information.

TABLE 7-1: BOR OPERATING MODES

BOREN Config bits	SBOREN	Device Mode	BOR Mode	Device Operation upon release of POR	Device Operation upon wake-up from Sleep
BOR_ON (11)	X	X	Active	Waits for BOR ready ⁽¹⁾	
BOR_NSLEEP (10)	X	Awake	Active	Waits for BOR ready	
BOR_NSLEEP (10)	X	Sleep	Disabled		
BOR_SBOREN (01)	1	X	Active	Begins immediately	
BOR_SBOREN (01)	0	X	Disabled	Begins immediately	
BOR_OFF (00)	X	X	Disabled	Begins immediately	

Note 1: In these specific cases, "Release of POR" and "Wake-up from Sleep", there is no delay in start-up. The BOR ready flag, (BORRDY = 1), will be set before the CPU is ready to execute instructions because the BOR circuit is forced on by the BOREN<1:0> bits.

7.2.1 BOR IS ALWAYS ON

When the BOREN bits of Configuration Word 1 are set to '11', the BOR is always on. The device start-up will be delayed until the BOR is ready and VDD is higher than the BOR threshold.

BOR protection is active during Sleep. The BOR does not delay wake-up from Sleep.

7.2.2 BOR IS OFF IN SLEEP

When the BOREN bits of Configuration Word 1 are set to '10', the BOR is on, except in Sleep. The device start-up will be delayed until the BOR is ready and VDD is higher than the BOR threshold.

BOR protection is not active during Sleep. The device wake-up will be delayed until the BOR is ready.

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REGISTER 12-10: ANSELC: PORTC ANALOG SELECT REGISTER

U-0	U-0	U-0	U-0	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1
—	—	—	—	ANSC3	ANSC2	ANSC1	ANSC0
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
u = Bit is unchanged x = Bit is unknown -n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set '0' = Bit is cleared

bit 7-4 **Unimplemented:** Read as '0'

bit 3-0 **ANSC<3:0>:** Analog Select between Analog or Digital Function on pins RC<3:0>, respectively
0 = Digital I/O. Pin is assigned to port or digital special function.
1 = Analog input. Pin is assigned as analog input⁽¹⁾. Digital input buffer disabled.

Note 1: When setting a pin to an analog input, the corresponding TRIS bit must be set to Input mode in order to allow external control of the voltage on the pin.

REGISTER 12-11: WPUC: WEAK PULL-UP PORTC REGISTER

U-0	U-0	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1
—	—	WPUC5	WPUC4	WPUC3	WPUC2	WPUC1	WPUC0
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
u = Bit is unchanged x = Bit is unknown -n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set '0' = Bit is cleared

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **WPUC<5:0>:** Weak Pull-up Register bits^(1, 2)
1 = Pull-up enabled
0 = Pull-up disabled

Note 1: Global WPUEN bit of the OPTION register must be cleared for individual pull-ups to be enabled.

2: The weak pull-up device is automatically disabled if the pin is in configured as an output.

TABLE 12-4: SUMMARY OF REGISTERS ASSOCIATED WITH PORTC⁽¹⁾

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ANSELC	—	—	—	—	ANSC3	ANSC2	ANSC1	ANSC0	122
LATC	—	—	LATC5	LATC4	LATC3	LATC2	LATC1	LATC0	121
OPTION_REG	WPUEN	INTEDG	TMR0CS	TMR0SE	PSA	PS<2:0>			164
PORTC	—	—	RC5	RC4	RC3	RC2	RC1	RC0	121
TRISC	—	—	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	121
WPUC	—	—	WPUC5	WPUC4	WPUC3	WPUC2	WPUC1	WPUC0	122

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by PORTC.

Note 1: PIC16(L)F1823 only.

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REGISTER 18-2: SRCON1: SR LATCH CONTROL 1 REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
SRSPE	SRSCKE	SRSC2E ⁽¹⁾	SRSC1E	SRRPE	SRRCKE	SRRC2E ⁽¹⁾	SRRC1E
bit 7							bit 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

- bit 7 **SRSPE:** SR Latch Peripheral Set Enable bit
1 = SR latch is set when the SRI pin is high
0 = SRI pin has no effect on the set input of the SR latch
- bit 6 **SRSCKE:** SR Latch Set Clock Enable bit
1 = Set input of SR latch is pulsed with SRCLK
0 = SRCLK has no effect on the set input of the SR latch
- bit 5 **SRSC2E:** SR Latch C2 Set Enable bit⁽¹⁾
1 = SR latch is set when the C2 Comparator output is high
0 = C2 Comparator output has no effect on the set input of the SR latch
- bit 4 **SRSC1E:** SR Latch C1 Set Enable bit
1 = SR latch is set when the C1 Comparator output is high
0 = C1 Comparator output has no effect on the set input of the SR latch
- bit 3 **SRRPE:** SR Latch Peripheral Reset Enable bit
1 = SR latch is reset when the SRI pin is high
0 = SRI pin has no effect on the reset input of the SR latch
- bit 2 **SRRCKE:** SR Latch Reset Clock Enable bit
1 = Reset input of SR latch is pulsed with SRCLK
0 = SRCLK has no effect on the reset input of the SR latch
- bit 1 **SRRC2E:** SR Latch C2 Reset Enable bit⁽¹⁾
1 = SR latch is reset when the C2 Comparator output is high
0 = C2 Comparator output has no effect on the reset input of the SR latch
- bit 0 **SRRC1E:** SR Latch C1 Reset Enable bit
1 = SR latch is reset when the C1 Comparator output is high
0 = C1 Comparator output has no effect on the reset input of the SR latch

Note 1: PIC16(L)F1823 only.

21.3 Timer1 Prescaler

Timer1 has four prescaler options allowing 1, 2, 4 or 8 divisions of the clock input. The T1CKPS bits of the T1CON register control the prescale counter. The prescale counter is not directly readable or writable; however, the prescaler counter is cleared upon a write to TMR1H or TMR1L.

21.4 Timer1 Oscillator

A dedicated low-power 32.768 kHz oscillator circuit is built-in between pins T1OSI (input) and T1OSO (amplifier output). This internal circuit is to be used in conjunction with an external 32.768 kHz crystal.

The oscillator circuit is enabled by setting the T1OSCEN bit of the T1CON register. The oscillator will continue to run during Sleep.

Note: The oscillator requires a start-up and stabilization time before use. Thus, T1OSCEN should be set and a suitable delay observed prior to enabling Timer1.

21.5 Timer1 Operation in Asynchronous Counter Mode

If control bit $\overline{T1SYNC}$ of the T1CON register is set, the external clock input is not synchronized. The timer increments asynchronously to the internal phase clocks. If external clock source is selected then the timer will continue to run during Sleep and can generate an interrupt on overflow, which will wake-up the processor. However, special precautions in software are needed to read/write the timer (see Section 21.5.1 “Reading and Writing Timer1 in Asynchronous Counter Mode”).

Note: When switching from synchronous to asynchronous operation, it is possible to skip an increment. When switching from asynchronous to synchronous operation, it is possible to produce an additional increment.

21.5.1 READING AND WRITING TIMER1 IN ASYNCHRONOUS COUNTER MODE

Reading TMR1H or TMR1L while the timer is running from an external asynchronous clock will ensure a valid read (taken care of in hardware). However, the user should keep in mind that reading the 16-bit timer in two 8-bit values itself, poses certain problems, since the timer may overflow between the reads.

For writes, it is recommended that the user simply stop the timer and write the desired values. A write contention may occur by writing to the timer registers, while the register is incrementing. This may produce an unpredictable value in the TMR1H:TMR1L register pair.

21.6 Timer1 Gate

Timer1 can be configured to count freely or the count can be enabled and disabled using Timer1 Gate circuitry. This is also referred to as Timer1 Gate Enable.

Timer1 Gate can also be driven by multiple selectable sources.

21.6.1 TIMER1 GATE ENABLE

The Timer1 Gate Enable mode is enabled by setting the TMR1GE bit of the T1GCON register. The polarity of the Timer1 Gate Enable mode is configured using the T1GPOL bit of the T1GCON register.

When Timer1 Gate Enable mode is enabled, Timer1 will increment on the rising edge of the Timer1 clock source. When Timer1 Gate Enable mode is disabled, no incrementing will occur and Timer1 will hold the current count. See Figure 21-3 for timing details.

TABLE 21-3: TIMER1 GATE ENABLE SELECTIONS

T1CLK	T1GPOL	T1G	Timer1 Operation
↑	0	0	Counts
↑	0	1	Holds Count
↑	1	0	Holds Count
↑	1	1	Counts

21.6.2 TIMER1 GATE SOURCE SELECTION

The Timer1 Gate source can be selected from one of four different sources. Source selection is controlled by the T1GSS bits of the T1GCON register. The polarity for each available source is also selectable. Polarity selection is controlled by the T1GPOL bit of the T1GCON register.

TABLE 21-4: TIMER1 GATE SOURCES

T1GSS	Timer1 Gate Source
00	Timer1 Gate Pin
01	Overflow of Timer0 (TMR0 increments from FFh to 00h)
10	Comparator 1 Output sync_C1OUT (optionally Timer1 synchronized output)
11	Comparator 2 Output sync_C2OUT (optionally Timer1 synchronized output)

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23.5 Carrier Source Polarity Select

The signal provided from any selected input source for the carrier high and carrier low signals can be inverted. Inverting the signal for the carrier high source is enabled by setting the MDCHPOL bit of the MDCARH register. Inverting the signal for the carrier low source is enabled by setting the MDCLPOL bit of the MDCARL register.

23.6 Carrier Source Pin Disable

Some peripherals assert control over their corresponding output pin when they are enabled. For example, when the CCP1 module is enabled, the output of CCP1 is connected to the CCP1 pin.

This default connection to a pin can be disabled by setting the MDCHODIS bit in the MDCARH register for the carrier high source and the MDCLDIS bit in the MDCARL register for the carrier low source.

23.7 Programmable Modulator Data

The MDBIT of the MDCON register can be selected as the source for the modulator signal. This gives the user the ability to program the value used for modulation.

23.8 Modulator Source Pin Disable

The modulator source default connection to a pin can be disabled by setting the MDMSODIS bit in the MDSRC register.

23.9 Modulated Output Polarity

The modulated output signal provided on the MDOUT pin can also be inverted. Inverting the modulated output signal is enabled by setting the MDOPOL bit of the MDCON register.

23.10 Slew Rate Control

The slew rate limitation on the output port pin can be disabled. The slew rate limitation can be removed by clearing the MDSLR bit in the MDCON register.

23.11 Operation in Sleep Mode

The DSM module is not affected by Sleep mode. The DSM can still operate during Sleep, if the Carrier and Modulator input sources are also still operable during Sleep.

23.12 Effects of a Reset

Upon any device Reset, the Data Signal Modulator module is disabled. The user's firmware is responsible for initializing the module before enabling the output. The registers are reset to their default values.

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REGISTER 23-2: MDSRC: MODULATION SOURCE CONTROL REGISTER

R/W-x/u	U-0	U-0	U-0	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
MDMSODIS	—	—	—	MDMS<3:0>			
bit 7							bit 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

- bit 7 **MDMSODIS:** Modulation Source Output Disable bit
1 = Output signal driving the peripheral output pin (selected by MDMS<3:0>) is disabled
0 = Output signal driving the peripheral output pin (selected by MDMS<3:0>) is enabled
- bit 6-4 **Unimplemented:** Read as '0'
- bit 3-0 **MDMS<3:0>** Modulation Source Selection bits
1111 = Reserved. No channel connected.
1110 = Reserved. No channel connected.
1101 = Reserved. No channel connected.
1100 = Reserved. No channel connected.
1011 = Reserved. No channel connected.
1010 = EUSART TX output
1001 = Reserved. No channel selected.
1000 = MSSP1 SDO1 output
0111 = Comparator 2 output (PIC16(L)F1823 only. PIC12(L)F1822; Reserved, no channel connected.)
0110 = Comparator 1 output
0101 = Reserved. No channel connected.
0100 = Reserved. No channel connected.
0011 = Reserved. No channel connected.
0010 = CCP1 output (PWM Output mode only)
0001 = MDMIN port pin
0000 = MDBIT bit of MDCON register is modulation source

Note 1: Narrowed carrier pulse widths or spurs may occur in the signal stream if the carrier is not synchronized.

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REGISTER 23-3: MDCARH: MODULATION HIGH CARRIER CONTROL REGISTER

R/W-x/u	R/W-x/u	R/W-x/u	U-0	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
MDCHODIS	MDCHPOL	MDCHSYNC	—	MDCH<3:0>			
bit 7							bit 0

Legend:

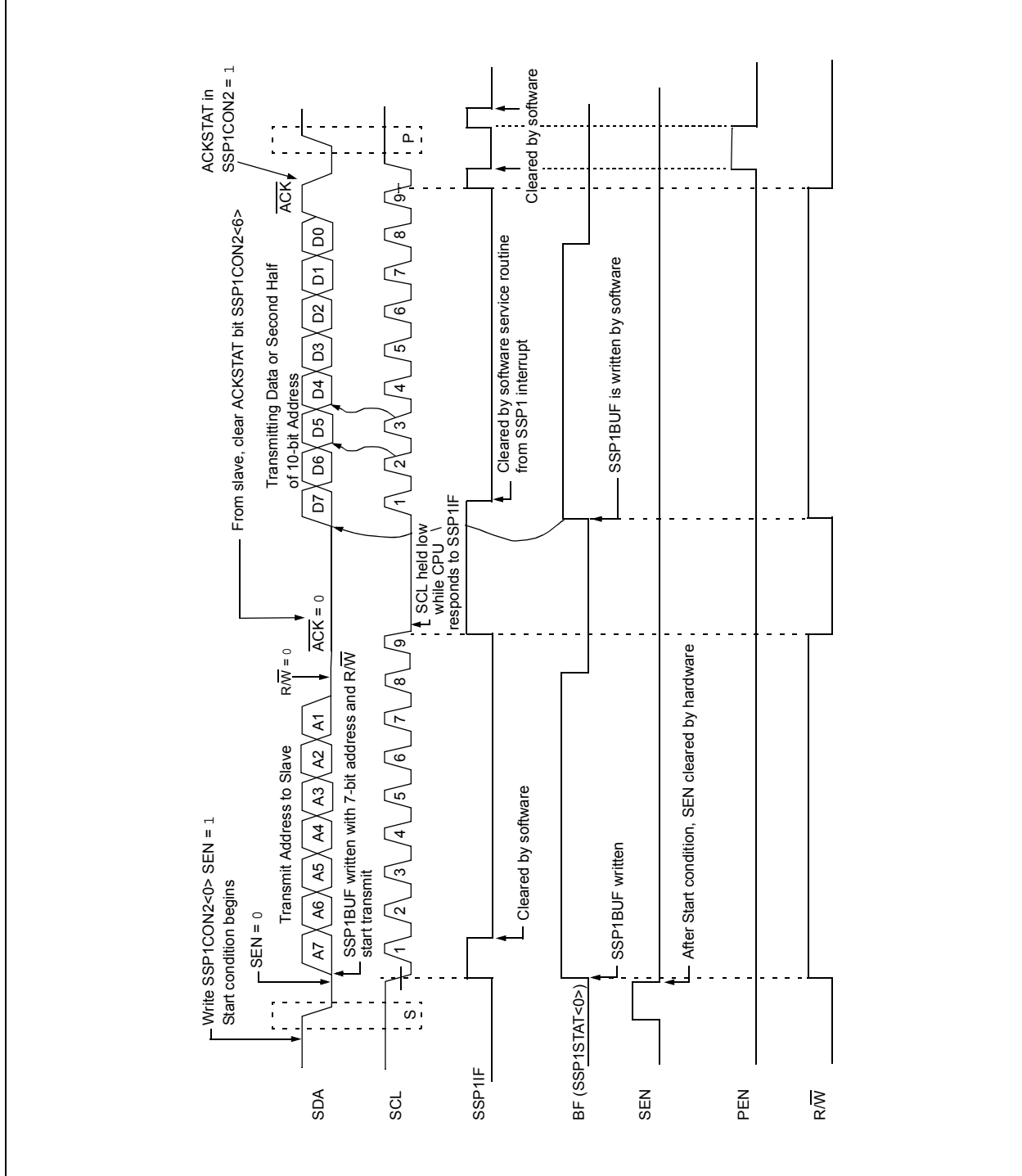
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

- bit 7 **MDCHODIS:** Modulator High Carrier Output Disable bit
 1 = Output signal driving the peripheral output pin (selected by MDCH<3:0>) is disabled
 0 = Output signal driving the peripheral output pin (selected by MDCH<3:0>) is enabled
- bit 6 **MDCHPOL:** Modulator High Carrier Polarity Select bit
 1 = Selected high carrier signal is inverted
 0 = Selected high carrier signal is not inverted
- bit 5 **MDCHSYNC:** Modulator High Carrier Synchronization Enable bit
 1 = Modulator waits for a falling edge on the high time carrier signal before allowing a switch to the low time carrier
 0 = Modulator Output is not synchronized to the high time carrier signal⁽¹⁾
- bit 4 **Unimplemented:** Read as '0'
- bit 3-0 **MDCH<3:0>** Modulator Data High Carrier Selection bits ⁽¹⁾
 1111 = Reserved. No channel connected.
 •
 •
 •
 0101 = Reserved. No channel connected.
 0100 = CCP1 output (PWM Output mode only)
 0011 = Reference Clock module signal (CLKR)
 0010 = MDCIN2 port pin
 0001 = MDCIN1 port pin
 0000 = VSS

Note 1: Narrowed carrier pulse widths or spurs may occur in the signal stream if the carrier is not synchronized.

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FIGURE 25-28: I²C MASTER MODE WAVEFORM (TRANSMISSION, 7 OR 10-BIT ADDRESS)



PIC12(L)F1822/16(L)F1823

25.6.13.3 Bus Collision During a Stop Condition

Bus collision occurs during a Stop condition if:

- a) After the SDA pin has been deasserted and allowed to float high, SDA is sampled low after the BRG has timed out (Case 1).
- b) After the SCL pin is deasserted, SCL is sampled low before SDA goes high (Case 2).

The Stop condition begins with SDA asserted low. When SDA is sampled low, the SCL pin is allowed to float. When the pin is sampled high (clock arbitration), the Baud Rate Generator is loaded with SSP1ADD and counts down to 0. After the BRG times out, SDA is sampled. If SDA is sampled low, a bus collision has occurred. This is due to another master attempting to drive a data '0' (Figure 25-38). If the SCL pin is sampled low before SDA is allowed to float high, a bus collision occurs. This is another case of another master attempting to drive a data '0' (Figure 25-39).

FIGURE 25-38: BUS COLLISION DURING A STOP CONDITION (CASE 1)

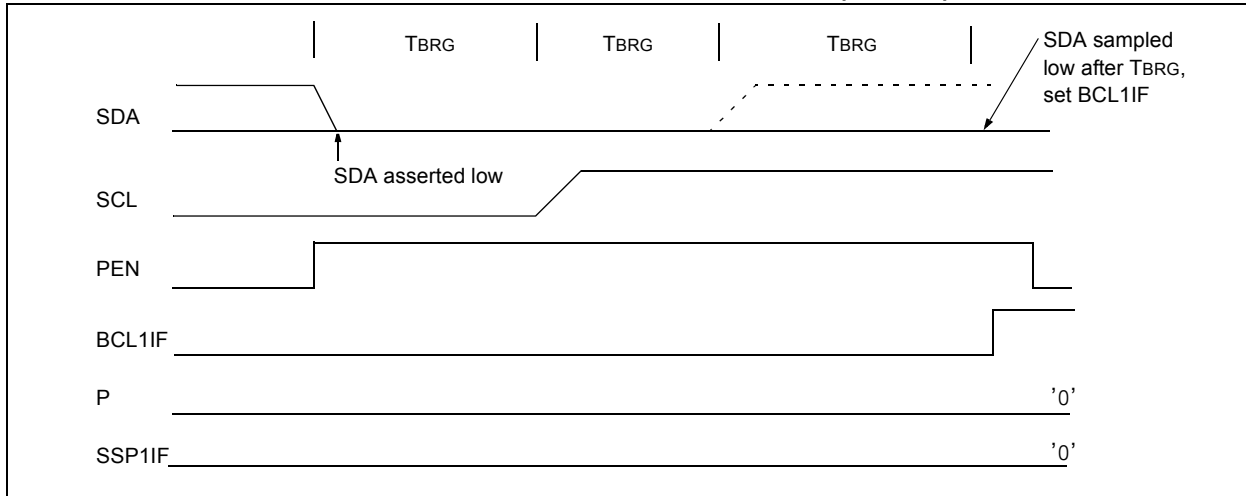
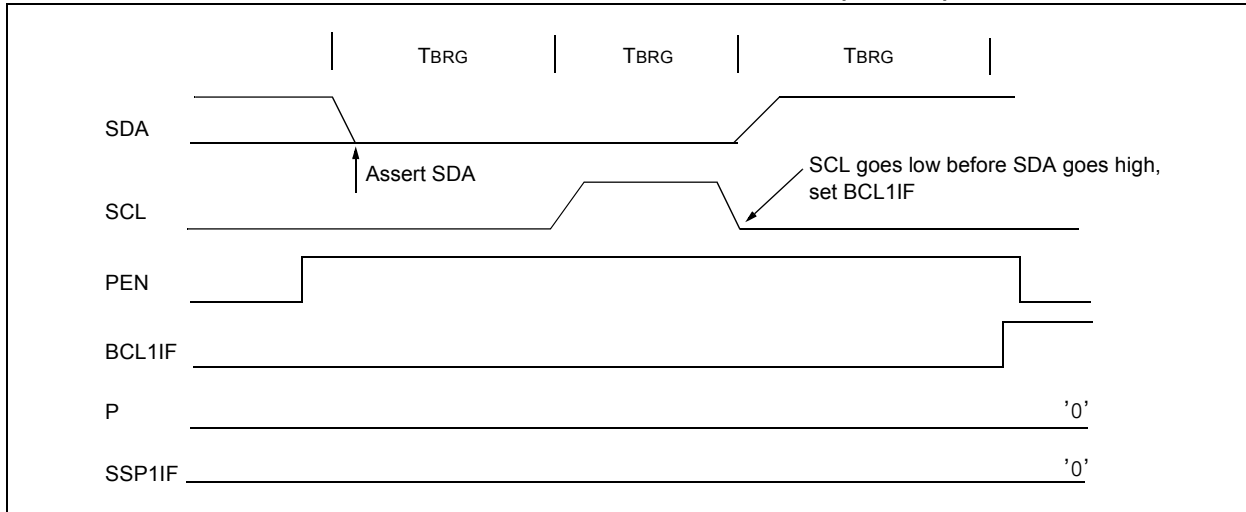


FIGURE 25-39: BUS COLLISION DURING A STOP CONDITION (CASE 2)



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26.1.2.4 Receive Framing Error

Each character in the receive FIFO buffer has a corresponding framing error Status bit. A framing error indicates that a Stop bit was not seen at the expected time. The framing error status is accessed via the FERR bit of the RCSTA register. The FERR bit represents the status of the top unread character in the receive FIFO. Therefore, the FERR bit must be read before reading the RCREG.

The FERR bit is read-only and only applies to the top unread character in the receive FIFO. A framing error (FERR = 1) does not preclude reception of additional characters. It is not necessary to clear the FERR bit. Reading the next character from the FIFO buffer will advance the FIFO to the next character and the next corresponding framing error.

The FERR bit can be forced clear by clearing the SPEN bit of the RCSTA register which resets the EUSART. Clearing the CREN bit of the RCSTA register does not affect the FERR bit. A framing error by itself does not generate an interrupt.

Note: If all receive characters in the receive FIFO have framing errors, repeated reads of the RCREG will not clear the FERR bit.
--

26.1.2.5 Receive Overrun Error

The receive FIFO buffer can hold two characters. An overrun error will be generated if a third character, in its entirety, is received before the FIFO is accessed. When this happens the OERR bit of the RCSTA register is set. The characters already in the FIFO buffer can be read but no additional characters will be received until the error is cleared. The error must be cleared by either clearing the CREN bit of the RCSTA register or by resetting the EUSART by clearing the SPEN bit of the RCSTA register.

26.1.2.6 Receiving 9-bit Characters

The EUSART supports 9-bit character reception. When the RX9 bit of the RCSTA register is set the EUSART will shift nine bits into the RSR for each character received. The RX9D bit of the RCSTA register is the ninth and Most Significant data bit of the top unread character in the receive FIFO. When reading 9-bit data from the receive FIFO buffer, the RX9D data bit must be read before reading the eight Least Significant bits from the RCREG.

26.1.2.7 Address Detection

A special Address Detection mode is available for use when multiple receivers share the same transmission line, such as in RS-485 systems. Address detection is enabled by setting the ADDEN bit of the RCSTA register.

Address detection requires 9-bit character reception. When address detection is enabled, only characters with the ninth data bit set will be transferred to the receive FIFO buffer, thereby setting the RCIF interrupt bit. All other characters will be ignored.

Upon receiving an address character, user software determines if the address matches its own. Upon address match, user software must disable address detection by clearing the ADDEN bit before the next Stop bit occurs. When user software detects the end of the message, determined by the message protocol used, software places the receiver back into the Address Detection mode by setting the ADDEN bit.

PIC12(L)F1822/16(L)F1823

FIGURE 31-44: POR RELEASE VOLTAGE

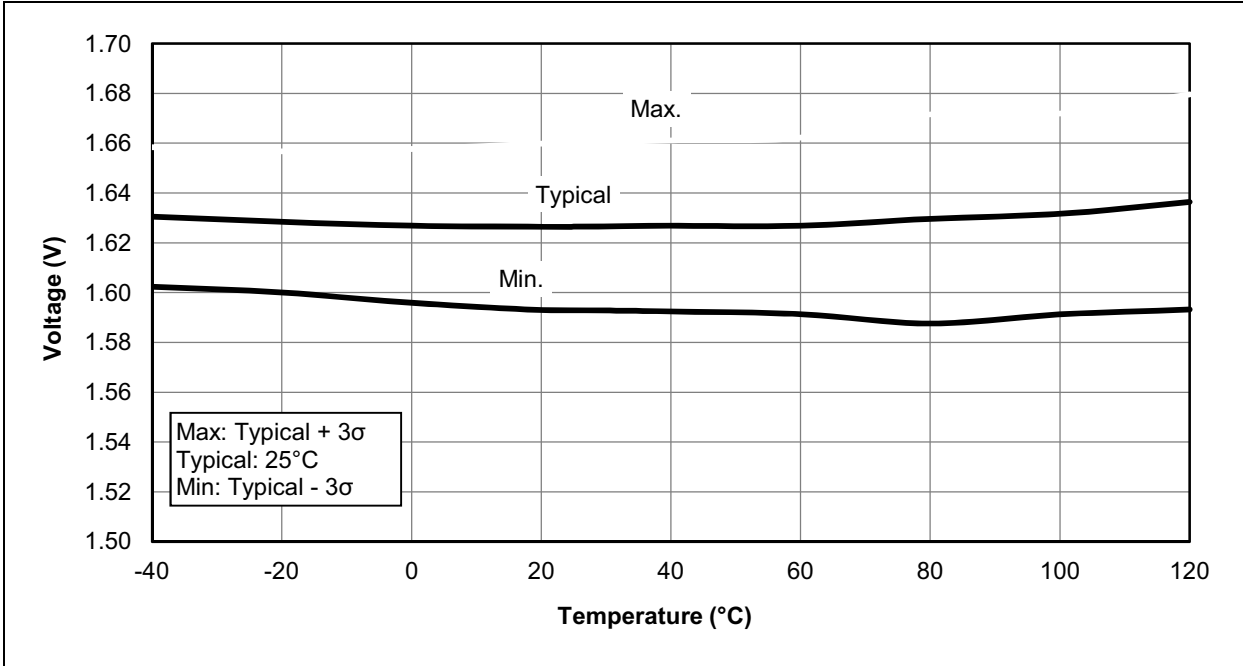
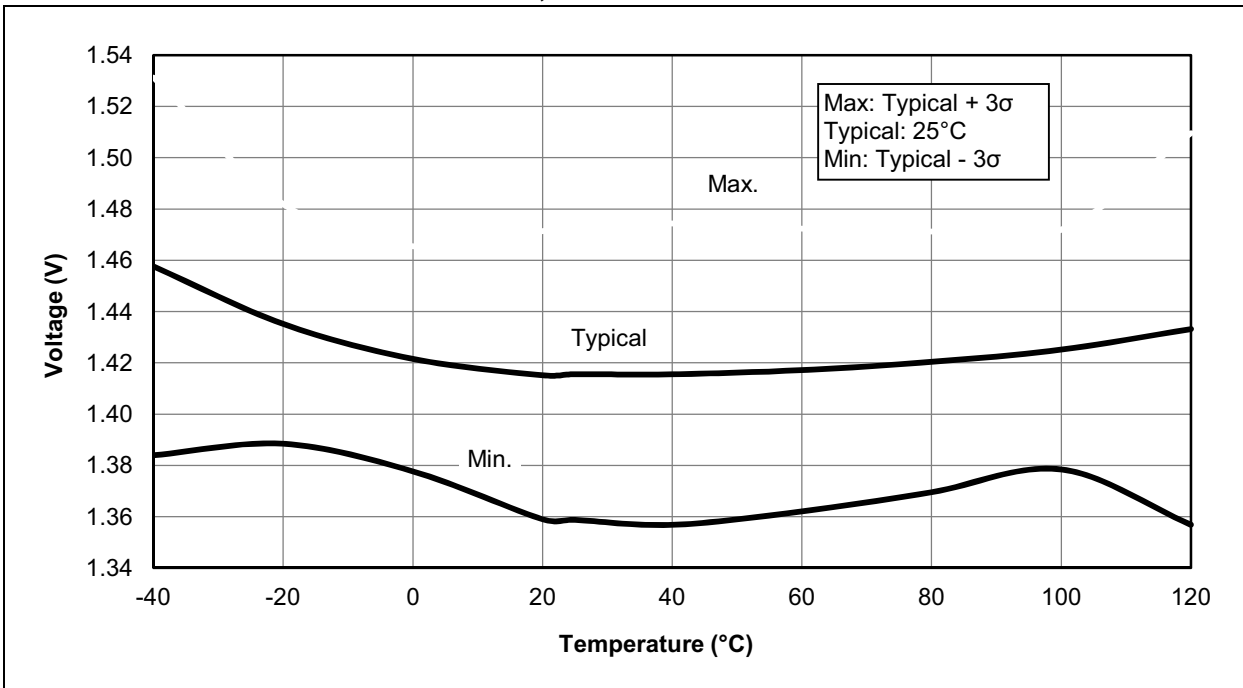


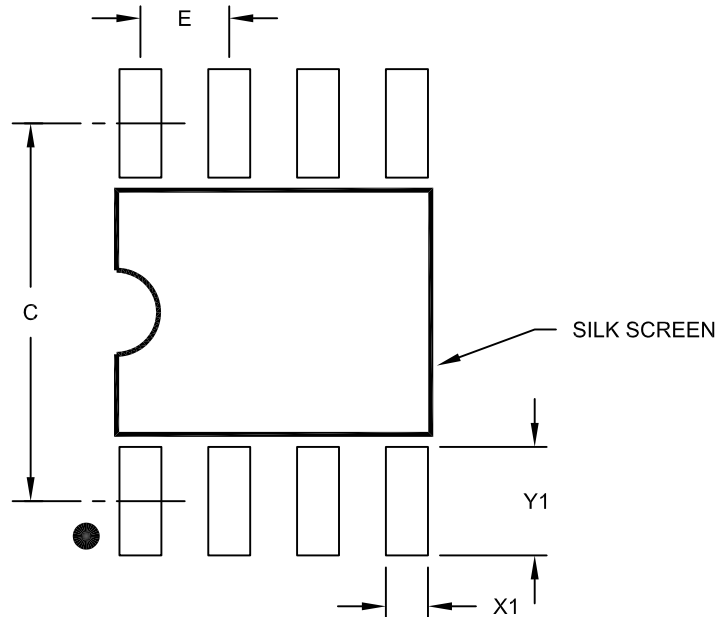
FIGURE 31-45: POR REARM VOLTAGE, PIC12F1822 AND PIC16F1823 ONLY



PIC12(L)F1822/16(L)F1823

8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

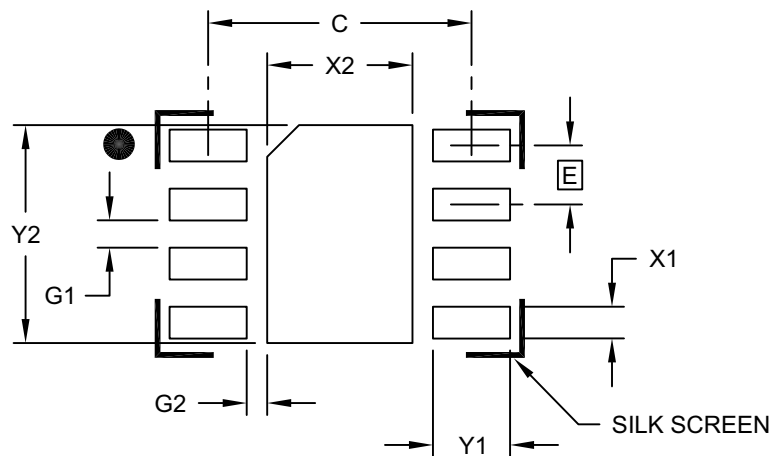
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A

PIC12(L)F1822/16(L)F1823

8-Lead Ultra Thin Plastic Dual Flat, No Lead Package (RF) - 3x3x0.50 mm Body [UDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Optional Center Pad Width	X2			1.60
Optional Center Pad Length	Y2			2.40
Contact Pad Spacing	C		2.90	
Contact Pad Width (X8)	X1			0.35
Contact Pad Length (X8)	Y1			0.85
Contact Pad to Contact Pad (X6)	G1	0.20		
Contact Pad to Center Pad (X8)	G2	0.30		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

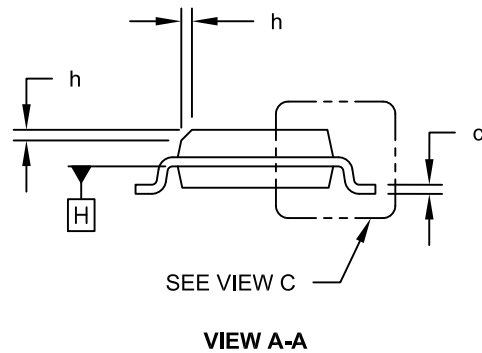
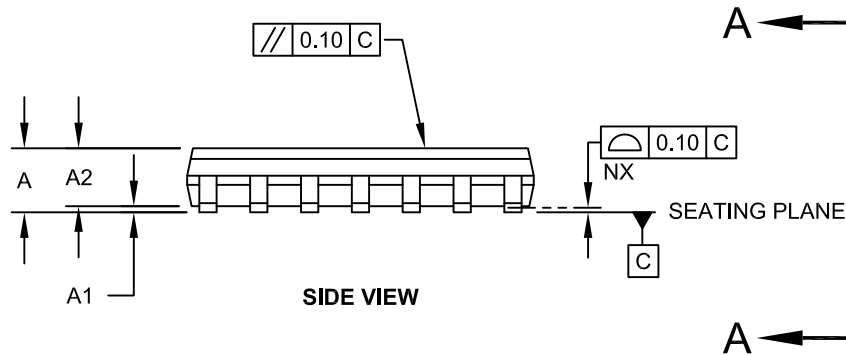
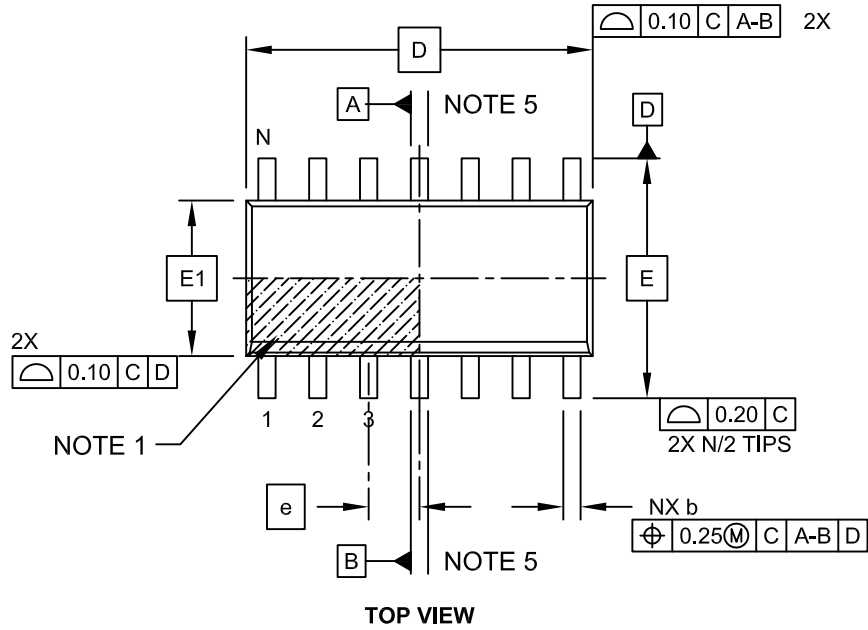
Microchip Technology Drawing C04-2254A

14-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

PIC12(L)F1822/16(L)F1823

14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

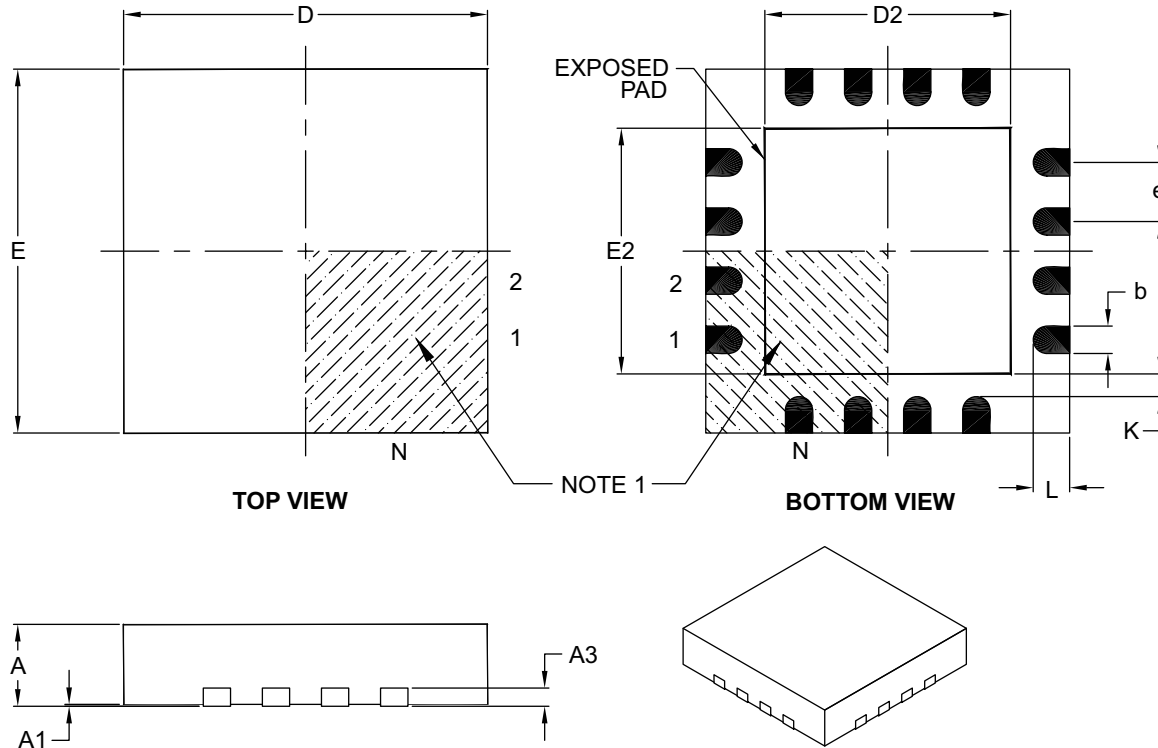


Microchip Technology Drawing No. C04-065C Sheet 1 of 2

PIC12(L)F1822/16(L)F1823

16-Lead Plastic Quad Flat, No Lead Package (ML) – 4x4x0.9 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Pins	N	16		
Pitch	e	0.65 BSC		
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3	0.20 REF		
Overall Width	E	4.00 BSC		
Exposed Pad Width	E2	2.50	2.65	2.80
Overall Length	D	4.00 BSC		
Exposed Pad Length	D2	2.50	2.65	2.80
Contact Width	b	0.25	0.30	0.35
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package is saw singulated.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

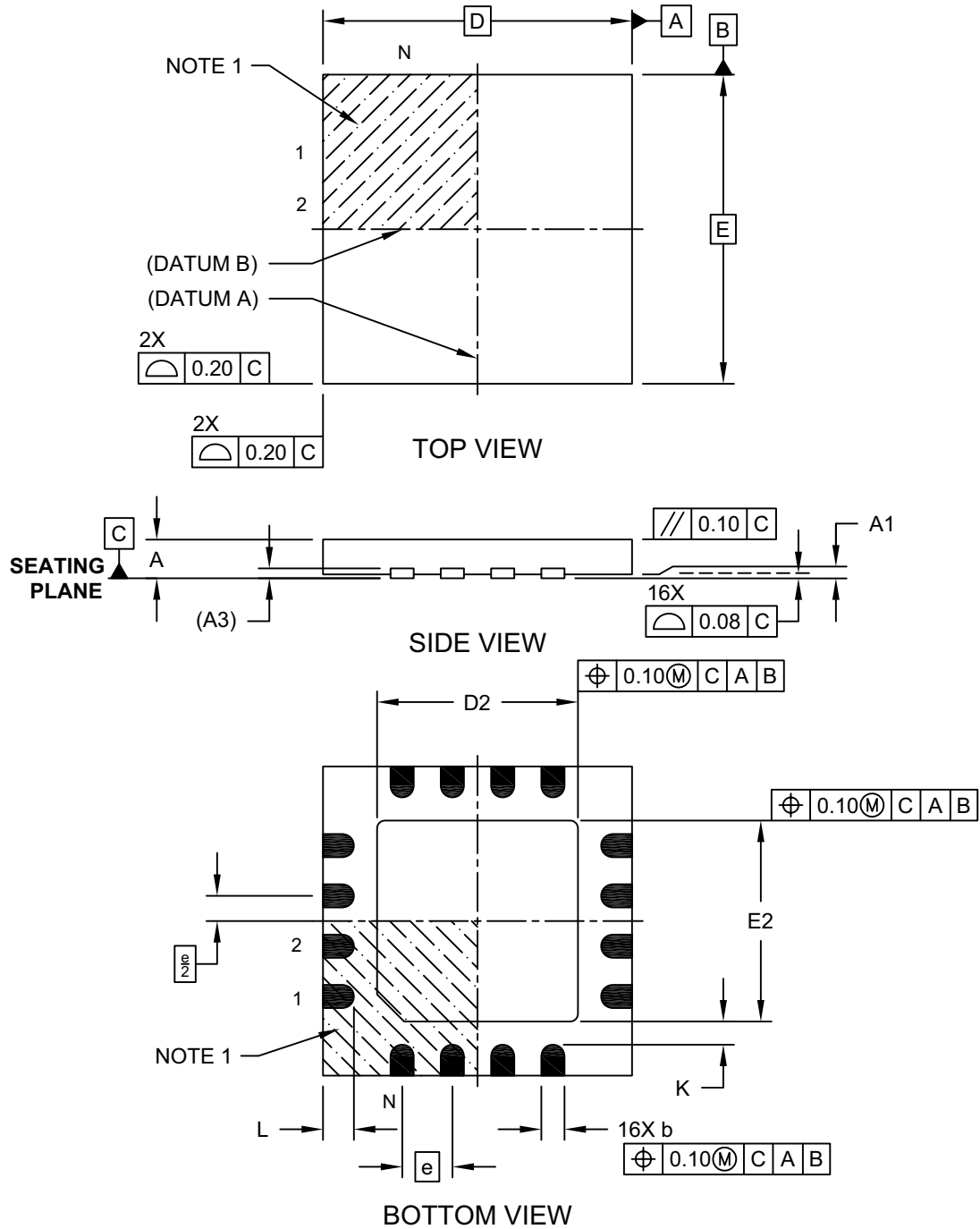
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-127B

PIC12(L)F1822/16(L)F1823

16-Lead Ultra Thin Plastic Quad Flat, No Lead Package (JQ) - 4x4x0.5 mm Body [UQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing C04-257A Sheet 1 of 2