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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Obsolete
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	55MHz
Connectivity	EBI/EMI, I ² C, SPI, SSC, UART/USART, USB
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	88
Program Memory Size	256КВ (256К х 8)
Program Memory Type	FLASH
EEPROM Size	·
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 1.95V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LFBGA
Supplier Device Package	144-BGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/atmel/at91sam7se256-cu

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



2. Block Diagram

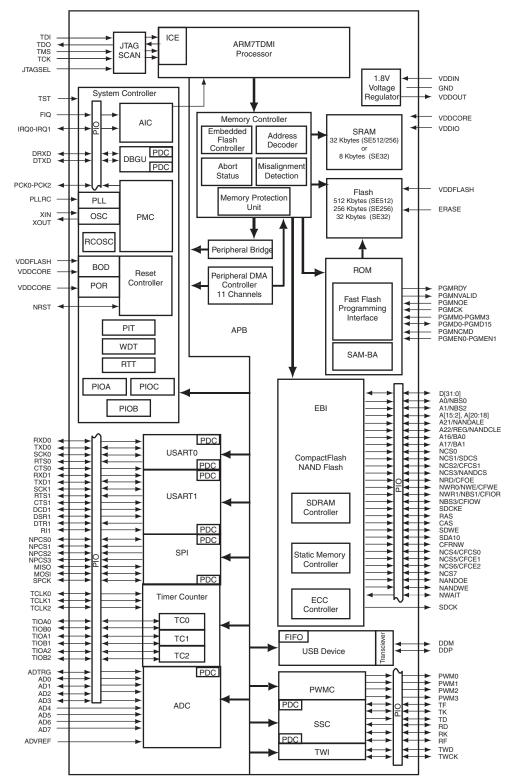






Table 3-1. Signal Description List (Continued)

Function	Туре	Active Level	Comments				
PIO							
Parallel IO Controller A	I/O		Pulled-up input at reset				
Parallel IO Controller B	I/O		Pulled-up input at reset				
Parallel IO Controller C	I/O		Pulled-up input at reset				
USB Device Port							
USB Device Port Data -	Analog						
USB Device Port Data +	Analog						
US	ART						
Serial Clock	I/O						
Transmit Data	I/O						
Receive Data	Input						
Request To Send	Output						
Clear To Send	Input						
Data Carrier Detect	Input						
Data Terminal Ready	Output						
Data Set Ready	Input						
Ring Indicator	Input						
Synchronous S	Serial Controlle	r					
Transmit Data	Output						
Receive Data	Input						
Transmit Clock	I/O						
Receive Clock	I/O						
Transmit Frame Sync	I/O						
Receive Frame Sync	I/O						
Timer/0	Counter						
External Clock Inputs	Input						
Timer Counter I/O Line A	I/O						
Timer Counter I/O Line B	I/O						
PWM C	ontroller						
PWM Channels	Output						
Serial Periph	eral Interface						
Master In Slave Out	I/O						
Master Out Slave In	I/O						
SPI Serial Clock	I/O						
SPI Peripheral Chip Select 0	I/O	Low					
SPI Peripheral Chip Select 1 to 3	Output	Low					
	Parallel IO Controller A Parallel IO Controller B Parallel IO Controller C USB Device Port Data - USB Device Port Data + USB Device Port Data + Serial Clock Transmit Data Receive Data Request To Send Clear To Send Data Carrier Detect Data Set Ready Ring Indicator Synchronous S Transmit Data Receive Data Receive Clock Transmit Data Receive Clock Transmit Clock Receive Clock Transmit Frame Sync Receive Frame Sync External Clock Inputs Timer Counter I/O Line A Timer Counter I/O Line B PWM Channels PWM Channels Serial Peripheral Clock SPI Serial Clock SPI Peripheral Chip Select 0	PIO Parallel IO Controller A I/O Parallel IO Controller B I/O Parallel IO Controller C I/O Parallel IO Controller C I/O USB Device Port Data - Analog USB Device Port Data + Analog USB Device Port Data + Analog Serial Clock I/O Transmit Data I/O Receive Data Input Request To Send Output Data Carrier Detect Input Data Carrier Detect Input Data Set Ready Input Receive Data Output Transmit Data Output Transmit Data Output Receive Data Input Receive Clock I/O Transmit Clock I/O Receive Clock I/O Receive Clock I/O Receive Prame Sync I/O Receive Frame Sync I/O Timer Counter I/O Line A I/O Timer Counter I/O Line A I/O Timer Counter I/O Line B I/O <td< td=""><td>FunctionTypeLevelParallel IO Controller AI/OI/OParallel IO Controller BI/OI/OParallel IO Controller CI/OI/OParallel IO Controller CI/OI/OUSB Device Port Data -AnalogI/OUSB Device Port Data +AnalogI/OSerial ClockI/OI/OTransmit DataI/OI/OReceive DataInputIRequest To SendOutputIData Carrier DetectInputIData Set ReadyInputIIng IndicatorInputIReceive DataOutputIData Set ReadyInputIReceive DataInputITransmit DataOutputIReceive DataInputIReceive DataInputIReceive DataInputIReceive DataInputIReceive DataInputIReceive DataInputIReceive ClockI/OIReceive Frame SyncI/OITimer Counter I/O Line AI/OITimer Counter I/O Line BIn/OIPWM ChannelsOutputInputMaster In Slave OutI/OIMaster In Slave InI/OISerial Peripheral ClockI/OISerial Peripheral ClockI/OISerial Peripheral ClockI/OISerial Peripheral ClockI/O<</td></td<>	FunctionTypeLevelParallel IO Controller AI/OI/OParallel IO Controller BI/OI/OParallel IO Controller CI/OI/OParallel IO Controller CI/OI/OUSB Device Port Data -AnalogI/OUSB Device Port Data +AnalogI/OSerial ClockI/OI/OTransmit DataI/OI/OReceive DataInputIRequest To SendOutputIData Carrier DetectInputIData Set ReadyInputIIng IndicatorInputIReceive DataOutputIData Set ReadyInputIReceive DataInputITransmit DataOutputIReceive DataInputIReceive DataInputIReceive DataInputIReceive DataInputIReceive DataInputIReceive DataInputIReceive ClockI/OIReceive Frame SyncI/OITimer Counter I/O Line AI/OITimer Counter I/O Line BIn/OIPWM ChannelsOutputInputMaster In Slave OutI/OIMaster In Slave InI/OISerial Peripheral ClockI/OISerial Peripheral ClockI/OISerial Peripheral ClockI/OISerial Peripheral ClockI/O<				

4. Package

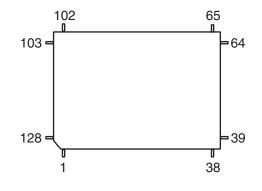
The SAM7SE512/256/32 is available in:

- 20 x 14 mm 128-lead LQFP package with a 0.5 mm lead pitch.
- 10x 10 x 1.4 mm 144-ball LFBGA package with a 0.8 mm lead pitch

4.1 128-lead LQFP Package Outline

Figure 4-1 shows the orientation of the 128-lead LQFP package and a detailed mechanical description is given in the Mechanical Characteristics section of the full datasheet.

Figure 4-1. 128-lead LQFP Package Outline (Top View)







4.2 128-lead LQFP Pinout

Table 4-1.Pinout in 128-lead LQFP Package

1	ADVREF	
2	GND	
3	AD7	
4	AD6	
5	AD5	
6	AD4	
7	VDDOUT	
8	VDDIN	
9	PA20/PGMD8/AD3	
10	PA19/PGMD7/AD2	
11	PA18/PGMD6/AD1	
12	PA17/PGMD5/AD0	
13	PA16/PGMD4	
14	PA15/PGMD3	
15	PA14/PGMD2	
16	PA13/PGMD1	
17	PA12/PGMD0	
18	PA11/PGMM3	
19	PA10/PGMM2	
20	PA9/PGMM1	
21	VDDIO	
22	GND	
23	VDDCORE	
24	PA8/PGMM0	
25	PA7/PGMNVALID	
26	PA6/PGMNOE	
27	PA5/PGMRDY	
28	PA4/PGMNCMD	
29	PA3	
30	PA2/PGMEN2	
31	PA1/PGMEN1	
32	PA0/PGMEN0	

	ППаскауе			
33	PB31			
34	PB30			
35	PB29			
36	PB28			
37	PB27			
38	PB26			
39	PB25			
40	PB24			
41	PB23			
42	PB22			
43	PB21			
44	PB20			
45	GND			
46	VDDIO			
47	VDDCORE			
48	PB19			
49	PB18			
50	PB17			
51	PB16			
52	PB15			
53	PB14			
54	PB13			
55	PB12			
56	PB11			
57	PB10			
58	PB9			
59	PB8			
60	PB7			
61	PB6			
62	PB5			
63	PB4			
64	PB3			

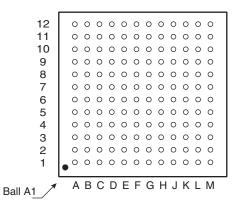
65	TDI
66	TDO
67	PB2
68	PB1
69	PB0
70	GND
71	VDDIO
72	VDDCORE
73	NRST
74	TST
75	ERASE
76	ТСК
77	TMS
78	JTAGSEL
79	PC23
80	PC22
81	PC21
82	PC20
83	PC19
84	PC18
85	PC17
86	PC16
87	PC15
88	PC14
89	PC13
90	PC12
91	PC11
92	PC10
93	PC9
94	GND
95	VDDIO
96	VDDCORE
	•

97	SDCK
98	PC8
99	PC7
100	PC6
101	PC5
102	PC4
103	PC3
104	PC2
105	PC1
106	PC0
107	PA31
108	PA30
109	PA29
110	PA28
111	PA27/PGMD15
112	PA26/PGMD14
113	PA25/PGMD13
114	PA24/PGMD12
115	PA23/PGMD11
116	PA22/PGMD10
117	PA21/PGMD9
118	VDDCORE
119	GND
120	VDDIO
121	DM
122	DP
123	VDDFLASH
124	GND
125	XIN/PGMCK
126	XOUT
127	PLLRC
128	VDDPLL

4.3 144-ball LFBGA Package Outline

Figure 4-2 shows the orientation of the 144-ball LFBGA package and a detailed mechanical description is given in the Mechanical Characteristics section.









- One external 2.2 μF (or 3.3 $\mu F)$ X7R capacitor should be connected between VDDOUT and GND.

Adequate input supply decoupling is mandatory for VDDIN in order to improve startup stability and reduce source voltage drop. The input decoupling capacitor should be placed close to the chip. For example, two capacitors can be used in parallel: 100 nF NPO and 4.7 μ F X7R.

5.4 Typical Powering Schematics

The SAM7SE512/256/32 supports a 3.3V single supply mode. The internal regulator input connected to the 3.3V source and its output feeds VDDCORE and the VDDPLL. Figure 5-1 shows the power schematics to be used for USB bus-powered systems.

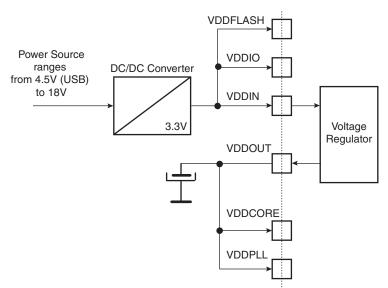


Figure 5-1. 3.3V System Single Power Supply Schematic



6.5 SDCK Pin

The SDCK pin is dedicated to the SDRAM Clock and is an output-only without pull-up. Maximum Output Frequency of this pad is 48 MHz at 3.0V and 25 MHz at 1.65V with a maximum load of 30 pF.

6.6 PIO Controller lines

All the I/O lines PA0 to PA31, PB0 to PB31, PC0 to PC23 integrate a programmable pull-up resistor. Programming of this pull-up resistor is performed independently for each I/O line through the PIO controllers.

Typical pull-up value is 100 k $\!\Omega$

All the I/O lines have schmitt trigger inputs.

6.7 I/O Lines Current Drawing

The PIO lines PA0 to PA3 are high-drive current capable. Each of these I/O lines can drive up to 16 mA permanently.

The remaining I/O lines can draw only 8 mA.

However, the total current drawn by all the I/O lines cannot exceed 300 mA.

SAM7SE512/256/32 Summary

7. Processor and Architecture

7.1 ARM7TDMI Processor

- RISC processor based on ARMv4T Von Neumann architecture
 - Runs at up to 55 MHz, providing 0.9 MIPS/MHz (core supplied with 1.8V)
- Two instruction sets
 - ARM® high-performance 32-bit instruction set
 - Thumb[®] high code density 16-bit instruction set
- Three-stage pipeline architecture
 - Instruction Fetch (F)
 - Instruction Decode (D)
 - Execute (E)

7.2 Debug and Test Features

- EmbeddedICE[™] (Integrated embedded in-circuit emulator)
 - Two watchpoint units
 - Test access port accessible through a JTAG protocol
 - Debug communication channel
- Debug Unit
 - Two-pin UART
 - Debug communication channel interrupt handling
 - Chip ID Register
- IEEE1149.1 JTAG Boundary-scan on all digital pins

7.3 Memory Controller

- Programmable Bus Arbiter
 - Handles requests from the ARM7TDMI and the Peripheral DMA Controller
- · Address decoder provides selection signals for
 - Four internal 1 Mbyte memory areas
 - One 256-Mbyte embedded peripheral area
 - Eight external 256-Mbyte memory areas
- Abort Status Registers
 - Source, Type and all parameters of the access leading to an abort are saved
 - Facilitates debug by detection of bad pointers
- Misalignment Detector
 - Alignment checking of all data accesses
 - Abort generation in case of misalignment
- Remap Command
 - Remaps the SRAM in place of the embedded non-volatile memory
 - Allows handling of dynamic exception vectors
- 16-area Memory Protection Unit (Internal Memory and peripheral protection only)



SAM7SE512/256/32 Summary

- Multiple device adaptability
 - Compliant with LCD Module
 - Compliant with PSRAM in synchronous operations
 - Programmable Setup Time Read/Write
 - Programmable Hold Time Read/Write
- Multiple Wait State Management
 - Programmable Wait State Generation
 - External Wait Request
 - Programmable Data Float Time

7.6 SDRAM Controller

- Numerous configurations supported
 - 2K, 4K, 8K Row Address Memory Parts
 - SDRAM with two or four Internal Banks
 - SDRAM with 16- or 32-bit Data Path
- Programming facilities
 - Word, half-word, byte access
 - Automatic page break when Memory Boundary has been reached
 - Multibank Ping-pong Access
 - Timing parameters specified by software
 - Automatic refresh operation, refresh rate is programmable
- Energy-saving capabilities
 - Self-refresh, and Low-power Modes supported
- Error detection
 - Refresh Error Interrupt
- SDRAM Power-up Initialization by software
- Latency is set to two clocks (CAS Latency of 1, 3 Not Supported)
- Auto Precharge Command not used
- Mobile SDRAM supported (except for low-power extended mode and deep power-down mode)

7.7 Error Corrected Code Controller

- Tracking the accesses to a NAND Flash device by triggering on the corresponding chip select
- Single bit error correction and 2-bit Random detection.
- Automatic Hamming Code Calculation while writing
 - ECC value available in a register
- Automatic Hamming Code Calculation while reading
 - Error Report, including error flag, correctable error flag and word address being detected erroneous
 - Supports 8- or 16-bit NAND Flash devices with 512-, 1024-, 2048- or 4096-byte pages





7.8 Peripheral DMA Controller

- Handles data transfer between peripherals and memories
- Eleven channels
 - Two for each USART
 - Two for the Debug Unit
 - Two for the Serial Synchronous Controller
 - Two for the Serial Peripheral Interface
 - One for the Analog-to-digital Converter
- · Low bus arbitration overhead
 - One Master Clock cycle needed for a transfer from memory to peripheral
 - Two Master Clock cycles needed for a transfer from peripheral to memory
- Next Pointer management for reducing interrupt latency requirements
- Peripheral DMA Controller (PDC) priority is as follows (from the highest priority to the lowest):

Receive	DBGU
Receive	USART0
Receive	USART1
Receive	SSC
Receive	ADC
Receive	SPI
Transmit	DBGU
Transmit	USART0
Transmit	USART1
Transmit	SSC
Transmit	SPI

SAM7SE512/256/32 Summary

8. Memories

- 512 Kbytes of Flash Memory (SAM7SE512)
 - dual plane
 - two contiguous banks of 1024 pages of 256 bytes
 - Fast access time, 30 MHz single-cycle access in Worst Case conditions
 - Page programming time: 6 ms, including page auto-erase
 - Page programming without auto-erase: 3 ms
 - Full chip erase time: 15 ms
 - 10,000 write cycles, 10-year data retention capability
 - 32 lock bits, each protecting 32 lock regions of 64 pages
 - Protection Mode to secure contents of the Flash
- 256 Kbytes of Flash Memory (SAM7SE256)
 - single plane
 - one bank of 1024 pages of 256 bytes
 - Fast access time, 30 MHz single-cycle access in Worst Case conditions
 - Page programming time: 6 ms, including page auto-erase
 - Page programming without auto-erase: 3 ms
 - Full chip erase time: 15 ms
 - 10,000 cycles, 10-year data retention capability
 - 16 lock bits, each protecting 16 lock regions of 64 pages
 - Protection Mode to secure contents of the Flash
- 32 Kbytes of Flash Memory (SAM7SE32)
 - single plane
 - one bank of 256 pages of 128 bytes
 - Fast access time, 30 MHz single-cycle access in Worst Case conditions
 - Page programming time: 6 ms, including page auto-erase
 - Page programming without auto-erase: 3 ms
 - Full chip erase time: 15 ms
 - 10,000 cycles, 10-year data retention capability
 - 8 lock bits, each protecting 8 lock regions of 32 pages
 - Protection Mode to secure contents of the Flash
- 32 Kbytes of Fast SRAM (SAM7SE512/256)
 - Single-cycle access at full speed
- 8 Kbytes of Fast SRAM (SAM7SE32)
 - Single-cycle access at full speed





256 Bytes/64 registers

SAM7SE512/256/32 Summary

256 MBytes

A	Address Memory Space	Э		Internal Me	emory Mappir	ng	Note:		
0x0000 0000			 0x0000 0000	0 0000 Boot Memory (1)		(1) Can be ROM, Flash or SRAM depending on GPNVM2 and REMAP			
	Internal Memories	256 MBytes		Flash be	efore Remap after Remap	1 MBytes			
0x0FFF FFFF 0x1000 0000	EBI		0x000F FFFF 0x0010 0000						
	Chip Select 0 SMC	256 MBytes		Interr	nal Flash	1 MBytes			
0x1FFF FFFF 0x2000 0000	300		0x001F FFFF 0x0020 0000						
	EBI Chip Select 1/	256 MBytes		Interr	al SRAM	1 MBytes			
0x2FFF FFFF	SMC or SDRAMC	,	0x002F FFFF 0x0030 0000						
0x3000 0000	EBI			Inter	nal ROM	1 MBytes			
	Chip Select 2 SMC	256 MBytes	0x003F FFFF 0x0040 0000						
0x3FFF FFFF 0x4000 0000	EBI								
	Chip Select 3 SMC/NANDFlash/	256 MBytes		Re	served	252 MBytes	3		
0x4FFF FFFF 0x5000 0000	SmartMedia		0x0FFF FFFF				Syste	em Controller Ma	pping
0,5000 0000	EBI Chip Select 4	256 MButoo					0xFFFF F000		
	SMC Compact Flash	256 MBytes						AIC	512 Bytes/128 registers
0x5FFF FFFF 0x6000 0000	EBI						0xFFFF F1FF		
	Chip Select 5 SMC	256 MBytes					0xFFFF F200		
0x6FFF FFFF 0x7000 0000	Compact Flash							DBGU	512 Bytes/128 registers
	EBI Chip Select 6	256 MBytes					0xFFFF F3FF 0xFFFF F400		
0x7FFF FFFF	Only Select 0	,	Periph 0xF000 0000	eral Mappin	g			PIOA	512 Bytes/128 registers
0x8000 0000	EBI	050 MD: too	R	eserved				FIOA	STZ Dytes/TZO registers
0x8FFF FFFF	Chip Select 7	256 MBytes		, TC1, TC2	16 Kbytes		0xFFFF F5FF 0xFFFF F600		
0x9000 0000			0xFFFA 3FFF 0xFFFA 4000	eserved				PIOB	512 Bytes/128 registers
			0xFFFA FFFF 0xFFFB 0000				0xFFFF F7FF		
			0xFFFB 3FFF 0xFFFB 4000	UDP	16 Kbytes		0xFFFF F800		
			R	eserved				PIOC	512 Bytes/128 registers
			0xFFFB 7FFF 0xFFFB 8000	TWI	16 Kbytes		0xFFFF F9FF 0xFFFF FA00		
			0xFFFB BFFF 0xFFFB C000	eserved			UXFFFF FAUU	Reserved	
			0xFFFB FFFF 0xFFFC 0000	ISART0	16 Kbytes		0xFFFF FBFF		
		6 x 256 MBytes	0xFFFC 3FFF				0xFFFF FC00	PMC	256 Bytes/64 registers
	Undefined (Abort)	1,536 MBytes	0xFFFC 7FFF	ISART1 eserved	16 Kbytes		0xFFFF FCFF 0xFFFF FD00	RSTC	16 Bytes/4 registers
			0xFFFC BFFF 0xFFFC C000	PWMC	16 Kbytes		0xFFFF FD0F		
			0xFFFC FFFF		101109100		0xFFFF FD20	Reserved	16 Dutoo/4 registers
			0xFFFD 3FFF 0xFFFD 4000	eserved			0xFFFF FC2F 0xFFFF FD30	RTT	16 Bytes/4 registers
			0xFFFD 7FFF	SSC	16 Kbytes		0xFFFF FC3F 0xFFFF FD40	PIT	16 Bytes/4 registers
			0xFFFD 8000 0xFFFD BFFF 0xFFFD C000	ADC	16 Kbytes		0xFFFF FD4F	WDT	16 Bytes/4 registers
			0xFFFD C000 0xFFFD FFFF	eserved			0xFFFF FD60	Reserved	
			0xFFFE 0000	SPI	16 Kbytes		0xFFFF FC6F	VREG	4 Bytes/1 register

Reserved

SYSC

0xFFFE 3FFF 0xFFFE 4000

0xFFFF EFFF

0xFFFF F000

0xFFFF FFFF

0xFFFF FD70

0xFFFF FEFF

0xFFFF FF00

0xFFFF FFFF

Reserved

MC

Internal Memory Mapping

Note:

Figure 8-1. SAM7SE Memory Mapping

Address Memory Space

22

0xEFFF FFFF 0xF000 0000

0xFFFF FFFF

Internal Peripherals

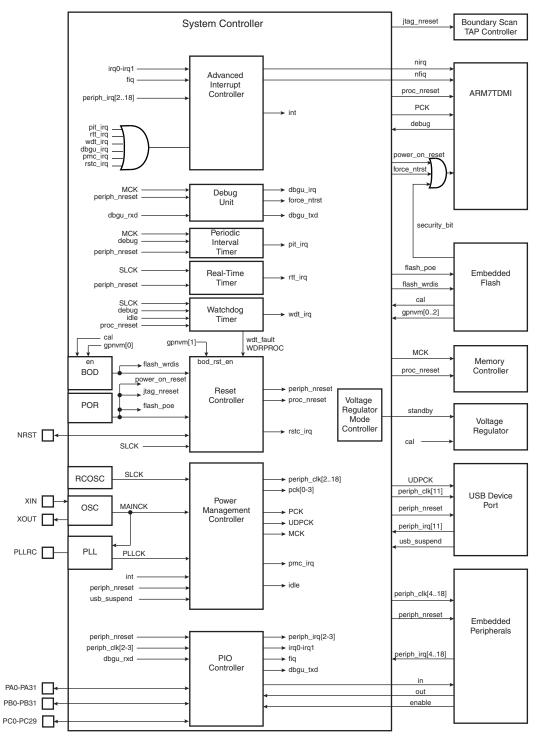


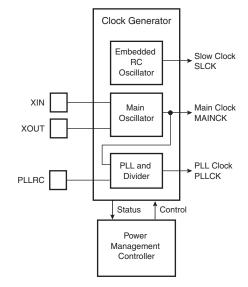
Figure 9-1. System Controller Block Diagram



- Main Oscillator frequency ranges between 3 and 20 MHz
- Main Oscillator can be bypassed
- PLL output ranges between 80 and 220 MHz

It provides SLCK, MAINCK and PLLCK.

Figure 9-2. Clock Generator Block Diagram



9.3 Power Management Controller

The Power Management Controller uses the Clock Generator outputs to provide:

- the Processor Clock PCK
- the Master Clock MCK
- the USB Clock UDPCK
- all the peripheral clocks, independently controllable
- three programmable clock outputs

The Master Clock (MCK) is programmable from a few hundred Hz to the maximum operating frequency of the device.

The Processor Clock (PCK) switches off when entering processor idle mode, thus allowing reduced power consumption while waiting for an interrupt.





• Synchronous output, provides Set and Clear of several I/O lines in a single write

9.10 Voltage Regulator Controller

The purpose of this controller is to select the Power Mode of the Voltage Regulator between Normal Mode (bit 0 is cleared) or Standby Mode (bit 0 is set).

10. Peripherals

10.1 User Interface

The User Peripherals are mapped in the 256 MBytes of the address space between 0xF000 0000 and 0xFFFF EFFF. Each peripheral is allocated 16 Kbytes of address space.

A complete memory map is presented in Figure 8-1 on page 22.

10.2 Peripheral Identifiers

The SAM7SE512/256/32 embeds a wide range of peripherals. Table 10-1 defines the Peripheral Identifiers of the SAM7SE512/256/32. Unique peripheral identifiers are defined for both the Advanced Interrupt Controller and the Power Management Controller.

Peripheral ID	Peripheral Mnemonic	Peripheral Name	External Interrupt
0	AIC	Advanced Interrupt Controller	FIQ
1	SYSC ⁽¹⁾		
2	PIOA	Parallel I/O Controller A	
3	PIOB	Parallel I/O Controller B	
4	PIOC	Parallel I/O Controller C	
5	SPI	Serial Peripheral Interface 0	
6	US0	USART 0	
7	US1	USART 1	
8	SSC	Synchronous Serial Controller	
9	тwi	Two-wire Interface	
10	PWMC	PWM Controller	
11	UDP	USB Device Port	
12	TC0	Timer/Counter 0	
13	TC1	Timer/Counter 1	
14	TC2	Timer/Counter 2	
15	ADC ⁽¹⁾	Analog-to Digital Converter	
16-28	reserved		
29	AIC	Advanced Interrupt Controller	IRQ0
30	AIC	Advanced Interrupt Controller	IRQ1

Table 10-1. Peripheral Identifiers

Note: 1. Setting SYSC and ADC bits in the clock set/clear registers of the PMC has no effect. The System Controller is continuously clocked. The ADC clock is automatically started for the first conversion. In Sleep Mode the ADC clock is automatically stopped after each conversion.





- 8- to 16-bit programmable data length per chip select
- Programmable phase and polarity per chip select
- Programmable transfer delays per chip select, between consecutive transfers and between clock and data
- Programmable delay between consecutive transfers
- Selectable mode fault detection
- Maximum frequency at up to Master Clock

10.8 Two Wire Interface

- Master, Multi-Master and Slave Mode Operation
- · Compatibility with standard two-wire serial memories
- One, two or three bytes for slave address
- · Sequential read/write operations
- Bit Rate: Up to 400 Kbit/s
- General Call Supported in Slave Mode

10.9 USART

- Programmable Baud Rate Generator
- 5- to 9-bit full-duplex synchronous or asynchronous serial communications
 - 1, 1.5 or 2 stop bits in Asynchronous Mode
 - 1 or 2 stop bits in Synchronous Mode
 - Parity generation and error detection
 - Framing error detection, overrun error detection
 - MSB or LSB first
 - Optional break generation and detection
 - By 8 or by 16 over-sampling receiver frequency
 - Hardware handshaking RTS CTS
 - Modem Signals Management DTR-DSR-DCD-RI on USART1
 - Receiver time-out and transmitter timeguard
 - Multi-drop Mode with address generation and detection
- RS485 with driver control signal
- ISO7816, T = 0 or T = 1 Protocols for interfacing with smart cards
 - NACK handling, error counter with repetition and iteration limit
- IrDA[®] modulation and demodulation
 - Communication at up to 115.2 Kbps
- Test Modes
 - Remote Loopback, Local Loopback, Automatic Echo

10.10 Serial Synchronous Controller

- Provides serial synchronous communication links used in audio and telecom applications
- · Contains an independent receiver and transmitter and a common clock divider

40 SAM7SE512/256/32 Summary

- Offers a configurable frame sync and data length
- Receiver and transmitter can be programmed to start automatically or on detection of different event on the frame sync signal
- Receiver and transmitter include a data signal, a clock signal and a frame synchronization signal

10.11 Timer Counter

- Three 16-bit Timer Counter Channels
 - Two output compare or one input capture per channel
- Wide range of functions including:
 - Frequency measurement
 - Event counting
 - Interval measurement
 - Pulse generation
 - Delay timing
 - Pulse Width Modulation
 - Up/down capabilities
- Each channel is user-configurable and contains:
 - Three external clock inputs
 - Five internal clock inputs, as defined in Table 10-4

Table 10-4. Timer Counter Clocks Assignment

TC Clock input	Clock
TIMER_CLOCK1	MCK/2
TIMER_CLOCK2	MCK/8
TIMER_CLOCK3	MCK/32
TIMER_CLOCK4	MCK/128
TIMER_CLOCK5	MCK/1024

- Two multi-purpose input/output signals
- Two global registers that act on all three TC channels

10.12 PWM Controller

- Four channels, one 16-bit counter per channel
- · Common clock generator, providing thirteen different clocks
 - One Modulo n counter providing eleven clocks
 - Two independent linear dividers working on modulo n counter outputs
- Independent channel programming
 - Independent enable/disable commands
 - Independent clock selection
 - Independent period and duty cycle, with double buffering
 - Programmable selection of the output waveform polarity
 - Programmable center or left aligned output waveform





10.13 USB Device Port

- USB V2.0 full-speed compliant,12 Mbits per second.
- Embedded USB V2.0 full-speed transceiver
- Embedded 2688-byte dual-port RAM for endpoints
- Eight endpoints
 - Endpoint 0: 64bytes
 - Endpoint 1 and 2: 64 bytes ping-pong
 - Endpoint 3: 64 bytes
 - Endpoint 4 and 5: 512 bytes ping-pong
 - Endpoint 6 and 7: 64 bytes ping-pong
 - Ping-pong Mode (two memory banks) for Isochronous and bulk endpoints
- Suspend/resume logic
- Integrated Pull-up on DDP

10.14 Analog-to-Digital Converter

- 8-channel ADC
- 10-bit 384 Ksamples/sec. or 8-bit 583 Ksamples/sec. Successive Approximation Register ADC
- ±2 LSB Integral Non Linearity, ±1 LSB Differential Non Linearity
- Integrated 8-to-1 multiplexer, offering eight independent 3.3V analog inputs
- External voltage reference for better accuracy on low voltage inputs
- Individual enable and disable of each channel
- Multiple trigger sources
 - Hardware or software trigger
 - External trigger pin
 - Timer Counter 0 to 2 outputs TIOA0 to TIOA2 trigger
- Sleep Mode and conversion sequencer
 - Automatic wakeup on trigger and back to sleep mode after conversions of all enabled channels
- Each analog input shared with digital signals



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