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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	55MHz
Connectivity	EBI/EMI, I²C, SPI, SSC, UART/USART, USB
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	88
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 1.95V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	128-LQFP
Supplier Device Package	128-LQFP (20x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at91sam7se256b-au

2. Block Diagram

Figure 2-1. SAM7SE512/256/32 Block Diagram Signal Description

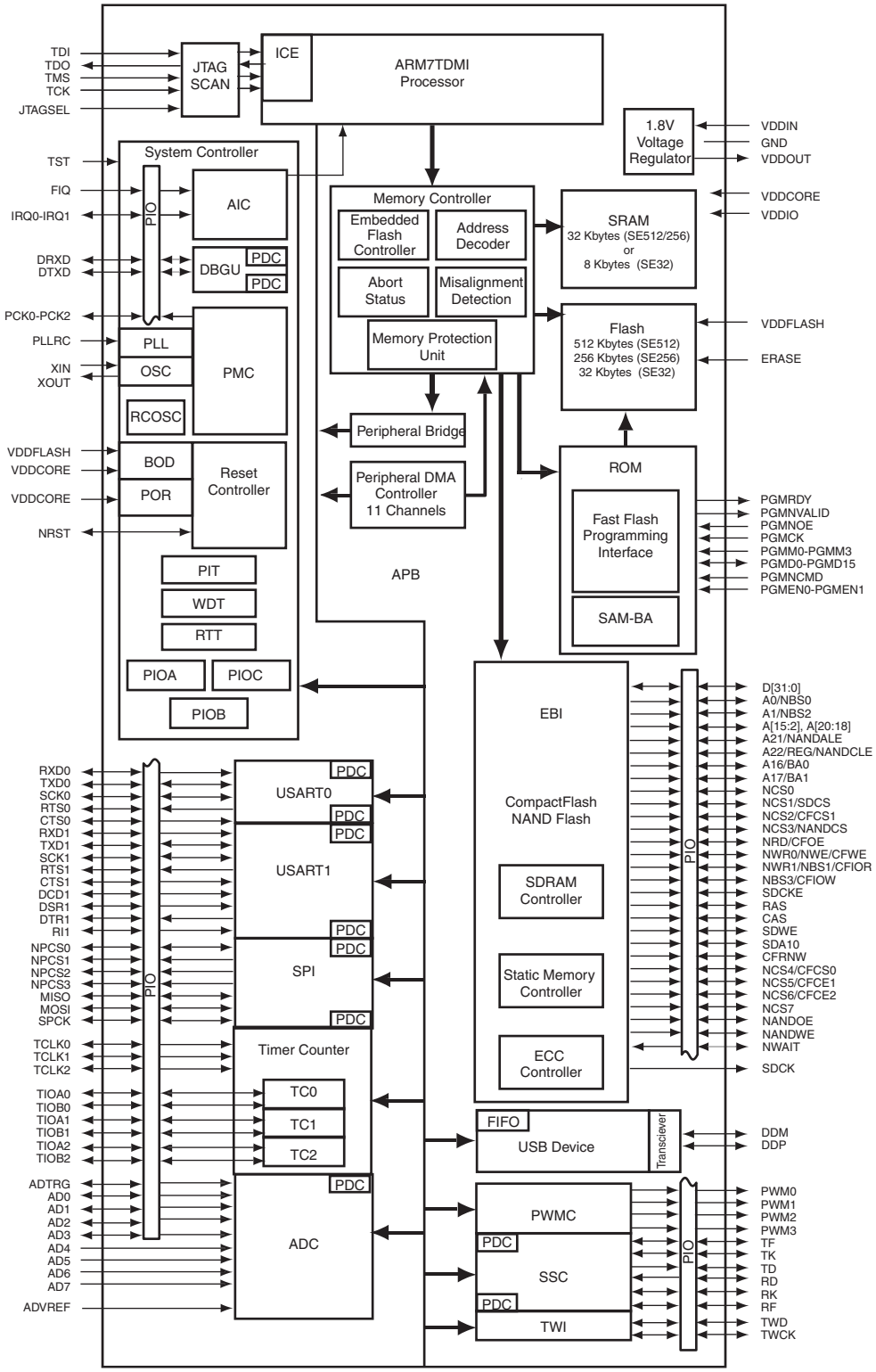


Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Comments
EBI for NAND Flash Support				
NANDCS	NAND Flash Chip Select Line	Output	Low	
NANDOE	NAND Flash Output Enable	Output	Low	
NANDWE	NAND Flash Write Enable	Output	Low	
NANDCLE	NAND Flash Command Line Enable	Output	Low	
NANDALE	NAND Flash Address Line Enable	Output	Low	
SDRAM Controller				
SDCK	SDRAM Clock	Output		Tied low after reset
SDCKE	SDRAM Clock Enable	Output	High	
SDCS	SDRAM Controller Chip Select Line	Output	Low	
BA[1:0]	Bank Select	Output		
SDWE	SDRAM Write Enable	Output	Low	
RAS - CAS	Row and Column Signal	Output	Low	
NBS[3:0]	Byte Mask Signals	Output	Low	
SDA10	SDRAM Address 10 Line	Output		

Note: 1. Refer to Section 6. “/O Lines Considerations” on page 15.

4. Package

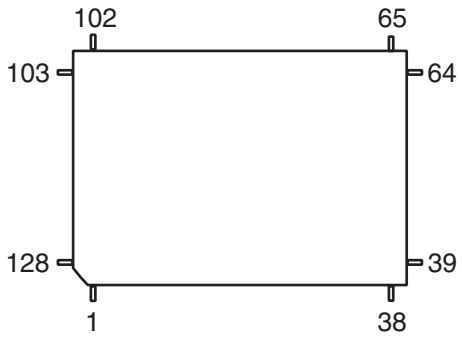
The SAM7SE512/256/32 is available in:

- 20 x 14 mm 128-lead LQFP package with a 0.5 mm lead pitch.
- 10x 10 x 1.4 mm 144-ball LFBGA package with a 0.8 mm lead pitch

4.1 128-lead LQFP Package Outline

Figure 4-1 shows the orientation of the 128-lead LQFP package and a detailed mechanical description is given in the Mechanical Characteristics section of the full datasheet.

Figure 4-1. 128-lead LQFP Package Outline (Top View)



4.2 128-lead LQFP Pinout

Table 4-1. Pinout in 128-lead LQFP Package

1	ADVREF	33	PB31	65	TDI	97	SDCK
2	GND	34	PB30	66	TDO	98	PC8
3	AD7	35	PB29	67	PB2	99	PC7
4	AD6	36	PB28	68	PB1	100	PC6
5	AD5	37	PB27	69	PB0	101	PC5
6	AD4	38	PB26	70	GND	102	PC4
7	VDDOUT	39	PB25	71	VDDIO	103	PC3
8	VDDIN	40	PB24	72	VDDCORE	104	PC2
9	PA20/PGMD8/AD3	41	PB23	73	NRST	105	PC1
10	PA19/PGMD7/AD2	42	PB22	74	TST	106	PC0
11	PA18/PGMD6/AD1	43	PB21	75	ERASE	107	PA31
12	PA17/PGMD5/AD0	44	PB20	76	TCK	108	PA30
13	PA16/PGMD4	45	GND	77	TMS	109	PA29
14	PA15/PGMD3	46	VDDIO	78	JTAGSEL	110	PA28
15	PA14/PGMD2	47	VDDCORE	79	PC23	111	PA27/PGMD15
16	PA13/PGMD1	48	PB19	80	PC22	112	PA26/PGMD14
17	PA12/PGMD0	49	PB18	81	PC21	113	PA25/PGMD13
18	PA11/PGMM3	50	PB17	82	PC20	114	PA24/PGMD12
19	PA10/PGMM2	51	PB16	83	PC19	115	PA23/PGMD11
20	PA9/PGMM1	52	PB15	84	PC18	116	PA22/PGMD10
21	VDDIO	53	PB14	85	PC17	117	PA21/PGMD9
22	GND	54	PB13	86	PC16	118	VDDCORE
23	VDDCORE	55	PB12	87	PC15	119	GND
24	PA8/PGMM0	56	PB11	88	PC14	120	VDDIO
25	PA7/PGMNVALID	57	PB10	89	PC13	121	DM
26	PA6/PGMNOE	58	PB9	90	PC12	122	DP
27	PA5/PGMRDY	59	PB8	91	PC11	123	VDDFLASH
28	PA4/PGMNCMD	60	PB7	92	PC10	124	GND
29	PA3	61	PB6	93	PC9	125	XIN/PGMCK
30	PA2/PGMEN2	62	PB5	94	GND	126	XOUT
31	PA1/PGMEN1	63	PB4	95	VDDIO	127	PLLRC
32	PA0/PGMEN0	64	PB3	96	VDDCORE	128	VDDPLL

4.4 144-ball LFBGA Pinout

Table 4-2. SAM7SE512/256/32 Pinout for 144-ball LFBGA Package

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
A1	PB7	D1	VDDCORE	G1	PC18	K1	PC11
A2	PB8	D2	VDDCORE	G2	PC16	K2	PC6
A3	PB9	D3	PB2	G3	PC17	K3	PC2
A4	PB12	D4	TDO	G4	PC9	K4	PC0
A5	PB13	D5	TDI	G5	VDDIO	K5	PA27/PGMD15
A6	PB16	D6	PB17	G6	GND	K6	PA26/PGMD14
A7	PB22	D7	PB26	G7	GND	K7	GND
A8	PB23	D8	PA14/PGMD2	G8	GND	K8	VDDCORE
A9	PB25	D9	PA12/PGMD0	G9	GND	K9	VDDFLASH
A10	PB29	D10	PA11/PGMM3	G10	AD4	K10	VDDIO
A11	PB30	D11	PA8/PGMM0	G11	VDDIN	K11	VDDIO
A12	PB31	D12	PA7/PGMNVALID	G12	VDDOUT	K12	PA18/PGMD6/AD1
B1	PB6	E1	PC22	H1	PC15	L1	SDCK
B2	PB3	E2	PC23	H2	PC14	L2	PC7
B3	PB4	E3	NRST	H3	PC13	L3	PC4
B4	PB10	E4	TCK	H4	VDDCORE	L4	PC1
B5	PB14	E5	ERASE	H5	VDDCORE	L5	PA29
B6	PB18	E6	TEST	H6	GND	L6	PA24/PGMD12
B7	PB20	E7	VDDCORE	H7	GND	L7	PA21/PGMD9
B8	PB24	E8	VDDCORE	H8	GND	L8	ADVREF
B9	PB28	E9	GND	H9	GND	L9	VDDFLASH
B10	PA4/PGMNCMD	E10	PA9/PGMM1	H10	PA19/PGMD7/AD2	L10	VDDFLASH
B11	PA0/PGMEN0	E11	PA10/PGMM2	H11	PA20/PGMD8/AD3	L11	PA17/PGMD5/AD0
B12	PA1/PGMEN1	E12	PA13/PGMD1	H12	VDDIO	L12	GND
C1	PB0	F1	PC21	J1	PC12	M1	PC8
C2	PB1	F2	PC20	J2	PC10	M2	PC5
C3	PB5	F3	PC19	J3	PA30	M3	PC3
C4	PB11	F4	JTAGSEL	J4	PA28	M4	PA31
C5	PB15	F5	TMS	J5	PA23/PGMD11	M5	PA25/PGMD13
C6	PB19	F6	VDDIO	J6	PA22/PGMD10	M6	DM
C7	PB21	F7	GND	J7	AD6	M7	DP
C8	PB27	F8	GND	J8	AD7	M8	GND
C9	PA6/PGMNOE	F9	GND	J9	VDDCORE	M9	XIN/PGMCK
C10	PA5/PGMRDY	F10	AD5	J10	VDDCORE	M10	XOUT
C11	PA2/PGMEN2	F11	PA15/PGMD3	J11	VDDCORE	M11	PLLRC
C12	PA3	F12	PA16/PGMD4	J12	VDDIO	M12	VDDPLL

6. /O Lines Considerations

6.1 JTAG Port Pins

TMS, TDI and TCK are Schmitt trigger inputs. TMS, TDI and TCK do not integrate a pull-up resistor.

TDO is an output, driven at up to VDDIO, and has no pull-up resistor.

The JTAGSEL pin is used to select the JTAG boundary scan when asserted at a high level. The JTAGSEL pin integrates a permanent pull-down resistor of about 15 kΩ.

To eliminate any risk of spuriously entering the JTAG boundary scan mode due to noise on JTAGSEL, it should be tied externally to GND if boundary scan is not used, or put in place an external low value resistor (such as 1 kΩ).

6.2 Test Pin

The TST pin is used for manufacturing test or fast programming mode of the SAM7SE512/256/32 when asserted high. The TST pin integrates a permanent pull-down resistor of about 15 kΩ to GND.

To eliminate any risk of entering the test mode due to noise on the TST pin, it should be tied to GND if the FFPI is not used, or put in place an external low value resistor (such as 1 kΩ).

To enter fast programming mode, the TST pin and the PA0 and PA1 pins should be tied high and PA2 tied low.

Driving the TST pin at a high level while PA0 or PA1 is driven at 0 leads to unpredictable results.

6.3 Reset Pin

The NRST pin is bidirectional with an open-drain output buffer. It is handled by the on-chip reset controller and can be driven low to provide a reset signal to the external components or asserted low externally to reset the microcontroller. There is no constraint on the length of the reset pulse, and the reset controller can guarantee a minimum pulse length. This allows connection of a simple push-button on the NRST pin as system user reset, and the use of the NRST signal to reset all the components of the system.

An external power-on reset can drive this pin during the start-up instead of using the internal power-on reset circuit.

The NRST pin integrates a permanent pull-up of about 100 kΩ resistor to VDDIO.

This pin has Schmitt trigger input.

6.4 ERASE Pin

The ERASE pin is used to re-initialize the Flash content and some of its NVM bits. It integrates a permanent pull-down resistor of about 15 kΩ to GND.

To eliminate any risk of erasing the Flash due to noise on the ERASE pin, it should be tied externally to GND, which prevents erasing the Flash from the application, or put in place an external low value resistor (such as 1 kΩ).

This pin is debounced by the RC oscillator to improve the glitch tolerance. When the pin is tied to high during less than 100 ms, ERASE pin is not taken into account. The pin must be tied high during more than 220 ms to perform the re-initialization of the Flash.

6.5 SDCK Pin

The SDCK pin is dedicated to the SDRAM Clock and is an output-only without pull-up. Maximum Output Frequency of this pad is 48 MHz at 3.0V and 25 MHz at 1.65V with a maximum load of 30 pF.

6.6 PIO Controller lines

All the I/O lines PA0 to PA31, PB0 to PB31, PC0 to PC23 integrate a programmable pull-up resistor. Programming of this pull-up resistor is performed independently for each I/O line through the PIO controllers.

Typical pull-up value is 100 kΩ

All the I/O lines have schmitt trigger inputs.

6.7 I/O Lines Current Drawing

The PIO lines PA0 to PA3 are high-drive current capable. Each of these I/O lines can drive up to 16 mA permanently.

The remaining I/O lines can draw only 8 mA.

However, the total current drawn by all the I/O lines cannot exceed 300 mA.

7. Processor and Architecture

7.1 ARM7TDMI Processor

- RISC processor based on ARMv4T Von Neumann architecture
  - Runs at up to 55 MHz, providing 0.9 MIPS/MHz (core supplied with 1.8V)
- Two instruction sets
  - ARM® high-performance 32-bit instruction set
  - Thumb® high code density 16-bit instruction set
- Three-stage pipeline architecture
  - Instruction Fetch (F)
  - Instruction Decode (D)
  - Execute (E)

7.2 Debug and Test Features

- EmbeddedICE™ (Integrated embedded in-circuit emulator)
  - Two watchpoint units
  - Test access port accessible through a JTAG protocol
  - Debug communication channel
- Debug Unit
  - Two-pin UART
  - Debug communication channel interrupt handling
  - Chip ID Register
- IEEE1149.1 JTAG Boundary-scan on all digital pins

7.3 Memory Controller

- Programmable Bus Arbiter
  - Handles requests from the ARM7TDMI and the Peripheral DMA Controller
- Address decoder provides selection signals for
  - Four internal 1 Mbyte memory areas
  - One 256-Mbyte embedded peripheral area
  - Eight external 256-Mbyte memory areas
- Abort Status Registers
  - Source, Type and all parameters of the access leading to an abort are saved
  - Facilitates debug by detection of bad pointers
- Misalignment Detector
  - Alignment checking of all data accesses
  - Abort generation in case of misalignment
- Remap Command
  - Remaps the SRAM in place of the embedded non-volatile memory
  - Allows handling of dynamic exception vectors
- 16-area Memory Protection Unit (Internal Memory and peripheral protection only)

- Multiple device adaptability
  - Compliant with LCD Module
  - Compliant with PSRAM in synchronous operations
  - Programmable Setup Time Read/Write
  - Programmable Hold Time Read/Write
- Multiple Wait State Management
  - Programmable Wait State Generation
  - External Wait Request
  - Programmable Data Float Time

7.6 SDRAM Controller

- Numerous configurations supported
  - **2K, 4K, 8K Row Address Memory Parts**
  - **SDRAM with two or four Internal Banks**
  - **SDRAM with 16- or 32-bit Data Path**
- Programming facilities
  - **Word, half-word, byte access**
  - **Automatic page break when Memory Boundary has been reached**
  - **Multibank Ping-pong Access**
  - **Timing parameters specified by software**
  - **Automatic refresh operation, refresh rate is programmable**
- **Energy-saving capabilities**
  - **Self-refresh, and Low-power Modes supported**
- Error detection
  - **Refresh Error Interrupt**
- **SDRAM Power-up Initialization by software**
- **Latency is set to two clocks (CAS Latency of 1, 3 Not Supported)**
- **Auto Precharge Command not used**
- Mobile SDRAM supported (except for low-power extended mode and deep power-down mode)

7.7 Error Corrected Code Controller

- Tracking the accesses to a NAND Flash device by triggering on the corresponding chip select
- Single bit error correction and 2-bit Random detection.
- Automatic Hamming Code Calculation while writing
  - ECC value available in a register
- Automatic Hamming Code Calculation while reading
  - Error Report, including error flag, correctable error flag and word address being detected erroneous
  - Supports 8- or 16-bit NAND Flash devices with 512-, 1024-, 2048- or 4096-byte pages

A first level of address decoding is performed by the Memory Controller, i.e., by the implementation of the Advanced System Bus (ASB) with additional features.

Decoding splits the 4G bytes of address space into 16 areas of 256M bytes. The areas 1 to 8 are directed to the EBI that associates these areas to the external chip selects NC0 to NCS7. The area 0 is reserved for the addressing of the internal memories, and a second level of decoding provides 1M byte of internal memory area. The area 15 is reserved for the peripherals and provides access to the Advanced Peripheral Bus (APB).

Other areas are unused and performing an access within them provides an abort to the master requesting such an access.

8.1 Embedded Memories

8.1.1 Internal Memories

8.1.1.1 Internal SRAM

The SAM7SE512/256 embeds a high-speed 32-Kbyte SRAM bank. The SAM7SE32 embeds a high-speed 8-Kbyte SRAM bank. After reset and until the Remap Command is performed, the SRAM is only accessible at address 0x0020 0000. After Remap, the SRAM also becomes available at address 0x0.

8.1.1.2 Internal ROM

The SAM7SE512/256/32 embeds an Internal ROM. At any time, the ROM is mapped at address 0x30 0000. The ROM contains the FFPI and the SAM-BA boot program.

8.1.1.3 Internal Flash

- The SAM7SE512 features two banks of 256 Kbytes of Flash.
- The SAM7SE256 features one bank of 256 Kbytes of Flash.
- The SAM7SE32 features one bank of 32 Kbytes of Flash.

At any time, the Flash is mapped to address 0x0010 0000.

A general purpose NVM (GPNVM) bit is used to boot either on the ROM (default) or from the Flash.

This GPNVM bit can be cleared or set respectively through the commands “Clear General-purpose NVM Bit” and “Set General-purpose NVM Bit” of the EFC User Interface.

Setting the GPNVM bit 2 selects the boot from the Flash, clearing it selects the boot from the ROM. Asserting ERASE clears the GPNVM bit 2 and thus selects the boot from the ROM by default.

The Flash benefits from the integration of a power reset cell and from the brownout detector. This prevents code corruption during power supply changes, even in the worst conditions.

8.1.2.2 *Embedded Flash Controller*

The Embedded Flash Controller (EFC) manages accesses performed by the masters of the system. It enables reading the Flash and writing the write buffer. It also contains a User Interface, mapped within the Memory Controller on the APB. The User Interface allows:

- programming of the access parameters of the Flash (number of wait states, timings, etc.)
- starting commands such as full erase, page erase, page program, NVM bit set, NVM bit clear, etc.
- getting the end status of the last command
- getting error status
- programming interrupts on the end of the last commands or on errors

The Embedded Flash Controller also provides a dual 32-bit Prefetch Buffer that optimizes 16-bit access to the Flash. This is particularly efficient when the processor is running in Thumb mode.

- Two EFCs (EFC0 and EFC1) are embedded in the SAM7SE512 to control each plane of 256 KBytes. Dual plane organization allows concurrent Read and Program.
- One EFC (EFC0) is embedded in the SAM7SE256 to control the single plane 256 KBytes.
- One EFC (EFC0) is embedded in the SAM7SE32 to control the single plane 32 KBytes.

8.1.2.3 *Lock Regions*

The SAM7SE512 Embedded Flash Controller manages 32 lock bits to protect 32 regions of the flash against inadvertent flash erasing or programming commands. The SAM7SE512 contains 32 lock regions and each lock region contains 64 pages of 256 bytes. Each lock region has a size of 16 Kbytes.

The SAM7SE256 Embedded Flash Controller manages 16 lock bits to protect 16 regions of the flash against inadvertent flash erasing or programming commands. The SAM7SE256 contains 16 lock regions and each lock region contains 64 pages of 256 bytes. Each lock region has a size of 16 Kbytes.

The SAM7SE32 Embedded Flash Controller manages 8 lock bits to protect 8 regions of the flash against inadvertent flash erasing or programming commands. The SAM7SE32 contains 8 lock regions and each lock region contains 32 pages of 128 bytes. Each lock region has a size of 4 Kbytes.

If a locked-region's erase or program command occurs, the command is aborted and the EFC triggers an interrupt.

The 32 (SAM7SE512), 16 (SAM7SE256) or 8 (SAM7SE32) NVM bits are software programmable through the EFC User Interface. The command "Set Lock Bit" enables the protection. The command "Clear Lock Bit" unlocks the lock region.

Asserting the ERASE pin clears the lock bits, thus unlocking the entire Flash.

8.1.2.4 *Security Bit Feature*

The SAM7SE512/256/32 features a security bit, based on a specific NVM-bit. When the security is enabled, any access to the Flash, either through the ICE interface or through the Fast Flash Programming Interface, is forbidden.

9. System Controller

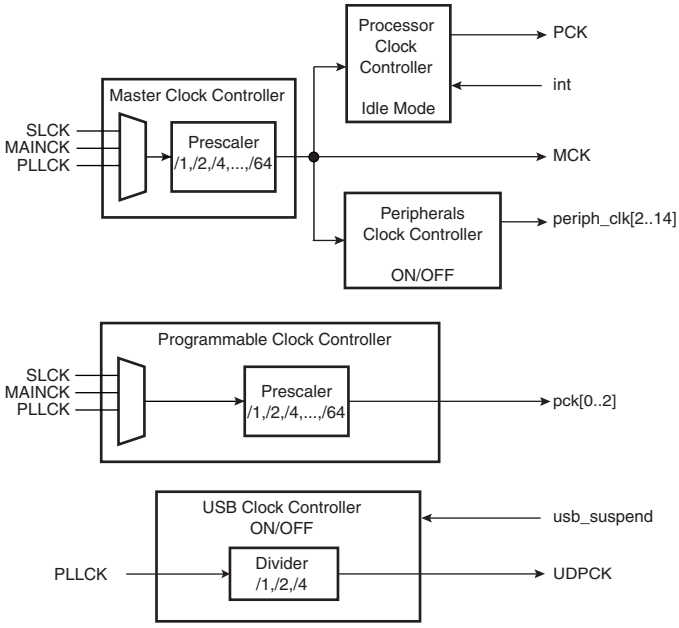
The System Controller manages all vital blocks of the microcontroller: interrupts, clocks, power, time, debug and reset.

The System Controller peripherals are all mapped to the highest 4 Kbytes of address space, between addresses 0xFFFF F000 and 0xFFFF FFFF.

Figure 9-1 on page 29 shows the System Controller Block Diagram.

Figure 8-1 on page 22 shows the mapping of the User Interface of the System Controller peripherals. Note that the Memory Controller configuration user interface is also mapped within this address space.

Figure 9-3. Power Management Controller Block Diagram



9.4 Advanced Interrupt Controller

- Controls the interrupt lines (nIRQ and nFIQ) of an ARM Processor
- Individually maskable and vectored interrupt sources
  - Source 0 is reserved for the Fast Interrupt Input (FIQ)
  - Source 1 is reserved for system peripherals (RTT, PIT, EFC, PMC, DBGU, etc.)
  - Other sources control the peripheral interrupts or external interrupts
  - Programmable edge-triggered or level-sensitive internal sources
  - Programmable positive/negative edge-triggered or high/low level-sensitive external sources
- 8-level Priority Controller
  - Drives the normal interrupt nIRQ of the processor
  - Handles priority of the interrupt sources
  - Higher priority interrupts can be served during service of lower priority interrupt
- Vectoring
  - Optimizes interrupt service routine branch and execution
  - One 32-bit vector register per interrupt source
  - Interrupt vector register reads the corresponding current interrupt vector
- Protect Mode
  - Easy debugging by preventing automatic operations
- Fast Forcing
  - Permits redirecting any interrupt source on the fast interrupt
- General Interrupt Mask
  - Provides processor synchronization on events without triggering an interrupt

9.5 Debug Unit

- Comprises:
  - One two-pin UART
  - One Interface for the Debug Communication Channel (DCC) support
  - One set of Chip ID Registers
  - One Interface providing ICE Access Prevention
- Two-pin UART
  - USART-compatible User Interface
  - Programmable Baud Rate Generator
  - Parity, Framing and Overrun Error
  - Automatic Echo, Local Loopback and Remote Loopback Channel Modes
- Debug Communication Channel Support
  - Offers visibility of COMMRX and COMMTX signals from the ARM Processor
- Chip ID Registers
  - Identification of the device revision, sizes of the embedded memories, set of peripherals
  - Chip ID is 0x272A 0A40 (VERSION 0) for SAM7SE512
  - Chip ID is 0x272A 0940 (VERSION 0) for SAM7SE256
  - Chip ID is 0x2728 0340 (VERSION 0) for SAM7SE32

9.6 Periodic Interval Timer

- 20-bit programmable counter plus 12-bit interval counter

9.7 Watchdog Timer

- 12-bit key-protected Programmable Counter running on prescaled SLCK
- Provides reset or interrupt signals to the system
- Counter may be stopped while the processor is in debug state or in idle mode

9.8 Real-time Timer

- 32-bit free-running counter with alarm running on prescaled SLCK
- Programmable 16-bit prescaler for SLCK accuracy compensation

9.9 PIO Controllers

- Three PIO Controllers. PIO A and B each control 32 I/O lines and PIO C controls 24 I/O lines.
- Fully programmable through set/clear registers
- Multiplexing of two peripheral functions per I/O line
- For each I/O line (whether assigned to a peripheral or used as general-purpose I/O)
  - Input change interrupt
  - Half a clock period glitch filter
  - Multi-drive option enables driving in open drain
  - Programmable pull-up on each I/O line
  - Pin data status register, supplies visibility of the level on the pin at any time

- Synchronous output, provides Set and Clear of several I/O lines in a single write

9.10 Voltage Regulator Controller

The purpose of this controller is to select the Power Mode of the Voltage Regulator between Normal Mode (bit 0 is cleared) or Standby Mode (bit 0 is set).

10. Peripherals

10.1 User Interface

The User Peripherals are mapped in the 256 MBytes of the address space between 0xF000 0000 and 0xFFFF EFFF. Each peripheral is allocated 16 Kbytes of address space.

A complete memory map is presented in Figure 8-1 on page 22.

10.2 Peripheral Identifiers

The SAM7SE512/256/32 embeds a wide range of peripherals. Table 10-1 defines the Peripheral Identifiers of the SAM7SE512/256/32. Unique peripheral identifiers are defined for both the Advanced Interrupt Controller and the Power Management Controller.

Table 10-1. Peripheral Identifiers

Peripheral ID	Peripheral Mnemonic	Peripheral Name	External Interrupt
0	AIC	Advanced Interrupt Controller	FIQ
1	SYSC[1]		
2	PIOA	Parallel I/O Controller A	
3	PIOB	Parallel I/O Controller B	
4	PIOC	Parallel I/O Controller C	
5	SPI	Serial Peripheral Interface 0	
6	US0	USART 0	
7	US1	USART 1	
8	SSC	Synchronous Serial Controller	
9	TWI	Two-wire Interface	
10	PWMC	PWM Controller	
11	UDP	USB Device Port	
12	TC0	Timer/Counter 0	
13	TC1	Timer/Counter 1	
14	TC2	Timer/Counter 2	
15	ADC[1]	Analog-to Digital Converter	
16-28	reserved		
29	AIC	Advanced Interrupt Controller	IRQ0
30	AIC	Advanced Interrupt Controller	IRQ1

Note: 1. Setting SYSC and ADC bits in the clock set/clear registers of the PMC has no effect. The System Controller is continuously clocked. The ADC clock is automatically started for the first conversion. In Sleep Mode the ADC clock is automatically stopped after each conversion.

10.3 Peripheral Multiplexing on PIO Lines

The SAM7SE512/256/32 features three PIO controllers, PIOA, PIOB and PIOC, that multiplex the I/O lines of the peripheral set.

PIO Controller A and B control 32 lines; PIO Controller C controls 24 lines. Each line can be assigned to one of two peripheral functions, A or B. Some of them can also be multiplexed with the analog inputs of the ADC Controller.

Table 10-2 on page 37 defines how the I/O lines of the peripherals A and B or the analog inputs are multiplexed on the PIO Controller A, B and C. The two columns “Function” and “Comments” have been inserted for the user’s own comments; they may be used to track how pins are defined in an application.

Note that some peripheral functions that are output only may be duplicated in the table.

At reset, all I/O lines are automatically configured as input with the programmable pull-up enabled, so that the device is maintained in a static state as soon as a reset is detected.

10.6 PIO Controller C Multiplexing

Multiplexing on PIO Controller C

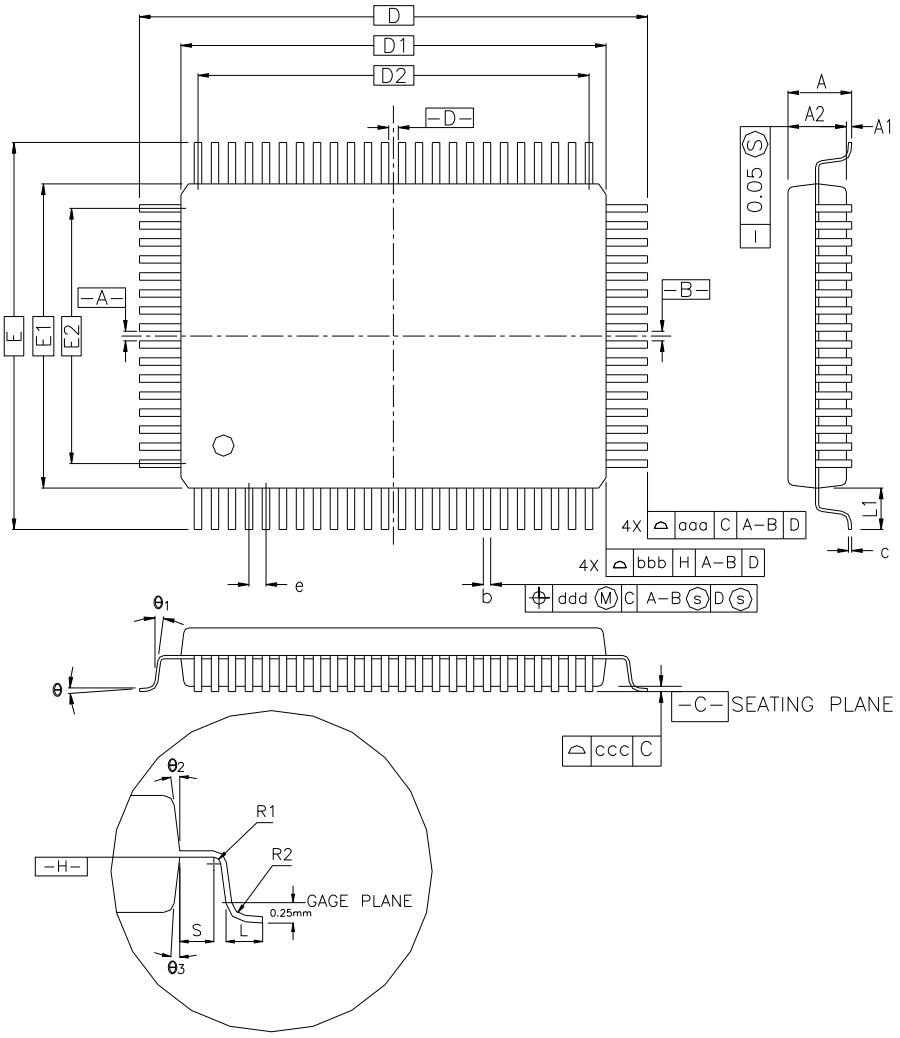
PIO Controller C				Application Usage	
I/O Line	Peripheral A	Peripheral B	Comments	Function	Comments
PC0	D0				
PC1	D1				
PC2	D2				
PC3	D3				
PC4	D4				
PC5	D5				
PC6	D6				
PC7	D7				
PC8	D8	RTS1			
PC9	D9	DTR1			
PC10	D10	PCK0			
PC11	D11	PCK1			
PC12	D12	PCK2			
PC13	D13				
PC14	D14	NPCS1			
PC15	D15	NCS3/NANDCS			
PC16	A18	NWAIT			
PC17	A19	NANDOE			
PC18	A20	NANDWE			
PC19	A21/NANDALE				
PC20	A22/REG/NANDCLE	NCS7			
PC21		NWR0/NWE/CFWE			
PC22		NRD/CFOE			
PC23	CFRNW	NCS0			

10.7 Serial Peripheral Interface

- Supports communication with external serial devices
  - Four chip selects with external decoder allow communication with up to 15 peripherals
  - Serial memories, such as DataFlash® and 3-wire EEPROMs
  - Serial peripherals, such as ADCs, DACs, LCD Controllers, CAN Controllers and Sensors
  - External co-processors
- Master or slave serial peripheral bus interface

11. Package Drawings

Figure 11-1. 128-lead LQFP Package Drawing



COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A_1	0.05	—	0.15	0.002	—	0.006
A_2	1.35	1.40	1.45	0.053	0.055	0.057
D	22.00 BSC.			0.866 BSC.		
D_1	20.00 BSC.			0.787 BSC.		
E	16.00 BSC.			0.630 BSC.		
E_1	14.00 BSC.			0.551 BSC.		
R_2	0.08	—	0.20	0.003	—	0.008
R_1	0.08	—	—	0.003	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ_1	0°	—	—	0°	—	—
θ_2	11°	12°	13°	11°	12°	13°
θ_3	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BSC.			0.020 BSC.		
D2	18.50			0.728		
E2	12.50			0.492		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

12. Ordering Information

Table 12-1. Ordering Information

Ordering Code	MRL	Package	Package Type	Temperature Operating Range
AT91SAM7SE512B-AU	B	LQFP128	Green	Industrial (-40· C to 85· C)
AT91SAM7SE256B-AU	B	LQFP128	Green	Industrial (-40· C to 85· C)
AT91SAM7SE32B-AU	B	LQFP128	Green	Industrial (-40· C to 85· C)
AT91SAM7SE512B-CU	B	LFBGA144	Green	Industrial (-40· C to 85· C)
AT91SAM7SE256B-CU	B	LFBGA144	Green	Industrial (-40· C to 85· C)
AT91SAM7SE32B-CU	B	LFBGA144	Green	Industrial (-40· C to 85· C)
AT91SAM7SE512-AU	A	LQFP128	Green	Industrial (-40· C to 85· C)
AT91SAM7SE256-AU	A	LQFP128	Green	Industrial (-40· C to 85· C)
AT91SAM7SE32-AU	A	LQFP128	Green	Industrial (-40· C to 85· C)
AT91SAM7SE512-CU	A	LFBGA144	Green	Industrial (-40· C to 85· C)
AT91SAM7SE256-CU	A	LFBGA144	Green	Industrial (-40· C to 85· C)
AT91SAM7SE32-CU	A	LFBGA144	Green	Industrial (-40· C to 85· C)