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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	55MHz
Connectivity	EBI/EMI, I²C, SPI, SSC, UART/USART, USB
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	88
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 1.95V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LFBGA
Supplier Device Package	144-LFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at91sam7se256b-cur

1. Description

Atmel's SAM7SE Series is a member of its Smart ARM Microcontroller family based on the 32-bit ARM7™ RISC processor and high-speed Flash memory.

- SAM7SE512 features a 512-Kbyte high-speed Flash and a 32 Kbyte SRAM.
- SAM7SE256 features a 256-Kbyte high-speed Flash and a 32 Kbyte SRAM.
- SAM7SE32 features a 32-Kbyte high-speed Flash and an 8 Kbyte SRAM.

It also embeds a large set of peripherals, including a USB 2.0 device, an External Bus Interface (EBI), and a complete set of system functions minimizing the number of external components.

The EBI incorporates controllers for synchronous DRAM (SDRAM) and Static memories and features specific circuitry facilitating the interface for NAND Flash, SmartMedia and CompactFlash.

The device is an ideal migration path for 8/16-bit microcontroller users looking for additional performance, extended memory and higher levels of system integration.

The embedded Flash memory can be programmed in-system via the JTAG-ICE interface or via a parallel interface on a production programmer prior to mounting. Built-in lock bits and a security bit protect the firmware from accidental overwrite and preserve its confidentiality.

The SAM7SE Series system controller includes a reset controller capable of managing the power-on sequence of the microcontroller and the complete system. Correct device operation can be monitored by a built-in brownout detector and a watchdog running off an integrated RC oscillator.

By combining the ARM7TDMI processor with on-chip Flash and SRAM, and a wide range of peripheral functions, including USART, SPI, External Bus Interface, Timer Counter, RTT and Analog-to-Digital Converters on a monolithic chip, the SAM7SE512/256/32 is a powerful device that provides a flexible, cost-effective solution to many embedded control applications.

1.1 Configuration Summary of the SAM7SE512, SAM7SE256 and SAM7SE32

The SAM7SE512, SAM7SE256 and SAM7SE32 differ in memory sizes and organization. Table 1-1 below summarizes the configurations for the three devices.

Table 1-1. Configuration Summary

Device	Flash Size	Flash Organization	RAM Size
SAM7SE512	512K bytes	dual plane	32K bytes
SAM7SE256	256K bytes	single plane	32K bytes
SAM7SE32	32K bytes	single plane	8K bytes

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Comments
Two-Wire Interface				
TWD	Two-wire Serial Data	I/O		
TWCK	Two-wire Serial Clock	I/O		
Analog-to-Digital Converter				
AD0-AD3	Analog Inputs	Analog		Digital pulled-up inputs at reset
AD4-AD7	Analog Inputs	Analog		Analog Inputs
ADTRG	ADC Trigger	Input		
ADVREF	ADC Reference	Analog		
Fast Flash Programming Interface				
PGMEN0-PGMEN2	Programming Enabling	Input		
PGMM0-PGMM3	Programming Mode	Input		
PGMD0-PGMD15	Programming Data	I/O		
PGMRDY	Programming Ready	Output	High	
PGMNVALID	Data Direction	Output	Low	
PGMNOE	Programming Read	Input	Low	
PGMCK	Programming Clock	Input		
PGMNCMD	Programming Command	Input	Low	
External Bus Interface				
D[31:0]	Data Bus	I/O		
A[22:0]	Address Bus	Output		
NWAIT	External Wait Signal	Input	Low	
Static Memory Controller				
NCS[7:0]	Chip Select Lines	Output	Low	
NWR[1:0]	Write Signals	Output	Low	
NRD	Read Signal	Output	Low	
NWE	Write Enable	Output	Low	
NUB	NUB: Upper Byte Select	Output	Low	
NLB	NLB: Lower Byte Select	Output	Low	
EBI for CompactFlash Support				
CFCE[2:1]	CompactFlash Chip Enable	Output	Low	
CFOE	CompactFlash Output Enable	Output	Low	
CFWE	CompactFlash Write Enable	Output	Low	
CFIOR	CompactFlash I/O Read Signal	Output	Low	
CFIOW	CompactFlash I/O Write Signal	Output	Low	
CFRNW	CompactFlash Read Not Write Signal	Output		
CFCS[1:0]	CompactFlash Chip Select Lines	Output	Low	

4. Package

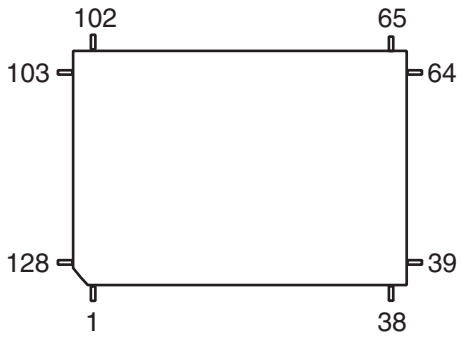
The SAM7SE512/256/32 is available in:

- 20 x 14 mm 128-lead LQFP package with a 0.5 mm lead pitch.
- 10x 10 x 1.4 mm 144-ball LFBGA package with a 0.8 mm lead pitch

4.1 128-lead LQFP Package Outline

Figure 4-1 shows the orientation of the 128-lead LQFP package and a detailed mechanical description is given in the Mechanical Characteristics section of the full datasheet.

Figure 4-1. 128-lead LQFP Package Outline (Top View)



4.2 128-lead LQFP Pinout

Table 4-1. Pinout in 128-lead LQFP Package

1	ADVREF	33	PB31	65	TDI	97	SDCK
2	GND	34	PB30	66	TDO	98	PC8
3	AD7	35	PB29	67	PB2	99	PC7
4	AD6	36	PB28	68	PB1	100	PC6
5	AD5	37	PB27	69	PB0	101	PC5
6	AD4	38	PB26	70	GND	102	PC4
7	VDDOUT	39	PB25	71	VDDIO	103	PC3
8	VDDIN	40	PB24	72	VDDCORE	104	PC2
9	PA20/PGMD8/AD3	41	PB23	73	NRST	105	PC1
10	PA19/PGMD7/AD2	42	PB22	74	TST	106	PC0
11	PA18/PGMD6/AD1	43	PB21	75	ERASE	107	PA31
12	PA17/PGMD5/AD0	44	PB20	76	TCK	108	PA30
13	PA16/PGMD4	45	GND	77	TMS	109	PA29
14	PA15/PGMD3	46	VDDIO	78	JTAGSEL	110	PA28
15	PA14/PGMD2	47	VDDCORE	79	PC23	111	PA27/PGMD15
16	PA13/PGMD1	48	PB19	80	PC22	112	PA26/PGMD14
17	PA12/PGMD0	49	PB18	81	PC21	113	PA25/PGMD13
18	PA11/PGMM3	50	PB17	82	PC20	114	PA24/PGMD12
19	PA10/PGMM2	51	PB16	83	PC19	115	PA23/PGMD11
20	PA9/PGMM1	52	PB15	84	PC18	116	PA22/PGMD10
21	VDDIO	53	PB14	85	PC17	117	PA21/PGMD9
22	GND	54	PB13	86	PC16	118	VDDCORE
23	VDDCORE	55	PB12	87	PC15	119	GND
24	PA8/PGMM0	56	PB11	88	PC14	120	VDDIO
25	PA7/PGMNVALID	57	PB10	89	PC13	121	DM
26	PA6/PGMNOE	58	PB9	90	PC12	122	DP
27	PA5/PGMRDY	59	PB8	91	PC11	123	VDDFLASH
28	PA4/PGMNCMD	60	PB7	92	PC10	124	GND
29	PA3	61	PB6	93	PC9	125	XIN/PGMCK
30	PA2/PGMEN2	62	PB5	94	GND	126	XOUT
31	PA1/PGMEN1	63	PB4	95	VDDIO	127	PLLRC
32	PA0/PGMEN0	64	PB3	96	VDDCORE	128	VDDPLL

5. Power Considerations

5.1 Power Supplies

The SAM7SE512/256/32 has six types of power supply pins and integrates a voltage regulator, allowing the device to be supplied with only one voltage. The six power supply pin types are:

- VDDIN pin. It powers the voltage regulator and the ADC; voltage ranges from 3.0V to 3.6V, 3.3V nominal.
- VDDOUT pin. It is the output of the 1.8V voltage regulator.
- VDDIO pin. It powers the I/O lines; two voltage ranges are supported:
  - from 3.0V to 3.6V, 3.3V nominal
  - or from 1.65V to 1.95V, 1.8V nominal.
- VDDFLASH pin. It powers the USB transceivers and a part of the Flash. It is required for the Flash to operate correctly; voltage ranges from 3.0V to 3.6V, 3.3V nominal.
- VDDCORE pins. They power the logic of the device; voltage ranges from 1.65V to 1.95V, 1.8V typical. It can be connected to the VDDOUT pin with decoupling capacitor. VDDCORE is required for the device, including its embedded Flash, to operate correctly.
- VDDPLL pin. It powers the oscillator and the PLL. It can be connected directly to the VDDOUT pin.

In order to decrease current consumption, if the voltage regulator and the ADC are not used, VDDIN, ADVREF, AD4, AD5, AD6 and AD7 should be connected to GND. In this case VDDOUT should be left unconnected.

No separate ground pins are provided for the different power supplies. Only GND pins are provided and should be connected as shortly as possible to the system ground plane.

5.2 Power Consumption

The SAM7SE512/256/32 has a static current of less than 60 µA on VDDCORE at 25°C, including the RC oscillator, the voltage regulator and the power-on reset when the brownout detector is deactivated. Activating the brownout detector adds 20 µA static current.

The dynamic power consumption on VDDCORE is less than 80 mA at full speed when running out of the Flash. Under the same conditions, the power consumption on VDDFLASH does not exceed 10 mA.

5.3 Voltage Regulator

The SAM7SE512/256/32 embeds a voltage regulator that is managed by the System Controller.

In Normal Mode, the voltage regulator consumes less than 100 µA static current and draws 100 mA of output current.

The voltage regulator also has a Low-power Mode. In this mode, it consumes less than 20 µA static current and draws 1 mA of output current.

Adequate output supply decoupling is mandatory for VDDOUT to reduce ripple and avoid oscillations. The best way to achieve this is to use two capacitors in parallel:

- One external 470 pF (or 1 nF) NPO capacitor should be connected between VDDOUT and GND as close to the chip as possible.

7. Processor and Architecture

7.1 ARM7TDMI Processor

- RISC processor based on ARMv4T Von Neumann architecture
  - Runs at up to 55 MHz, providing 0.9 MIPS/MHz (core supplied with 1.8V)
- Two instruction sets
  - ARM® high-performance 32-bit instruction set
  - Thumb® high code density 16-bit instruction set
- Three-stage pipeline architecture
  - Instruction Fetch (F)
  - Instruction Decode (D)
  - Execute (E)

7.2 Debug and Test Features

- EmbeddedICE™ (Integrated embedded in-circuit emulator)
  - Two watchpoint units
  - Test access port accessible through a JTAG protocol
  - Debug communication channel
- Debug Unit
  - Two-pin UART
  - Debug communication channel interrupt handling
  - Chip ID Register
- IEEE1149.1 JTAG Boundary-scan on all digital pins

7.3 Memory Controller

- Programmable Bus Arbiter
  - Handles requests from the ARM7TDMI and the Peripheral DMA Controller
- Address decoder provides selection signals for
  - Four internal 1 Mbyte memory areas
  - One 256-Mbyte embedded peripheral area
  - Eight external 256-Mbyte memory areas
- Abort Status Registers
  - Source, Type and all parameters of the access leading to an abort are saved
  - Facilitates debug by detection of bad pointers
- Misalignment Detector
  - Alignment checking of all data accesses
  - Abort generation in case of misalignment
- Remap Command
  - Remaps the SRAM in place of the embedded non-volatile memory
  - Allows handling of dynamic exception vectors
- 16-area Memory Protection Unit (Internal Memory and peripheral protection only)

  - Individually programmable size between 1K Byte and 1M Byte
  - Individually programmable protection against write and/or user access
  - Peripheral protection against write and/or user access
- Embedded Flash Controller
  - Embedded Flash interface, up to three programmable wait states
  - Prefetch buffer, buffering and anticipating the 16-bit requests, reducing the required wait states
  - Key-protected program, erase and lock/unlock sequencer
  - Single command for erasing, programming and locking operations
  - Interrupt generation in case of forbidden operation

7.4 External Bus Interface

- Integrates Three External Memory Controllers:
  - Static Memory Controller
  - SDRAM Controller
  - ECC Controller
- Additional Logic for NAND Flash and CompactFlash® Support
  - NAND Flash support: 8-bit as well as 16-bit devices are supported
  - CompactFlash support: all modes (Attribute Memory, Common Memory, I/O, True IDE) are supported but the signals _IOIS16 (I/O and True IDE modes) and -ATA SEL (True IDE mode) are not handled.
- Optimized External Bus:
  - 16- or 32-bit Data Bus (32-bit Data Bus for SDRAM only)
  - Up to 23-bit Address Bus, Up to 8-Mbytes Addressable
  - Up to 8 Chip Selects, each reserved to one of the eight Memory Areas
  - Optimized pin multiplexing to reduce latencies on External Memories
- Configurable Chip Select Assignment:
  - Static Memory Controller on NCS0
  - SDRAM Controller or Static Memory Controller on NCS1
  - Static Memory Controller on NCS2, Optional CompactFlash Support
  - Static Memory Controller on NCS3, NCS5 - NCS6, Optional NAND Flash Support
  - Static Memory Controller on NCS4, Optional CompactFlash Support
  - Static Memory Controller on NCS7

7.5 Static Memory Controller

- External memory mapping, 512-Mbyte address space
- 8-, or 16-bit Data Bus
- Up to 8 Chip Select Lines
- Multiple Access Modes supported
  - Byte Write or Byte Select Lines
  - Two different Read Protocols for each Memory Bank

- Multiple device adaptability
  - Compliant with LCD Module
  - Compliant with PSRAM in synchronous operations
  - Programmable Setup Time Read/Write
  - Programmable Hold Time Read/Write
- Multiple Wait State Management
  - Programmable Wait State Generation
  - External Wait Request
  - Programmable Data Float Time

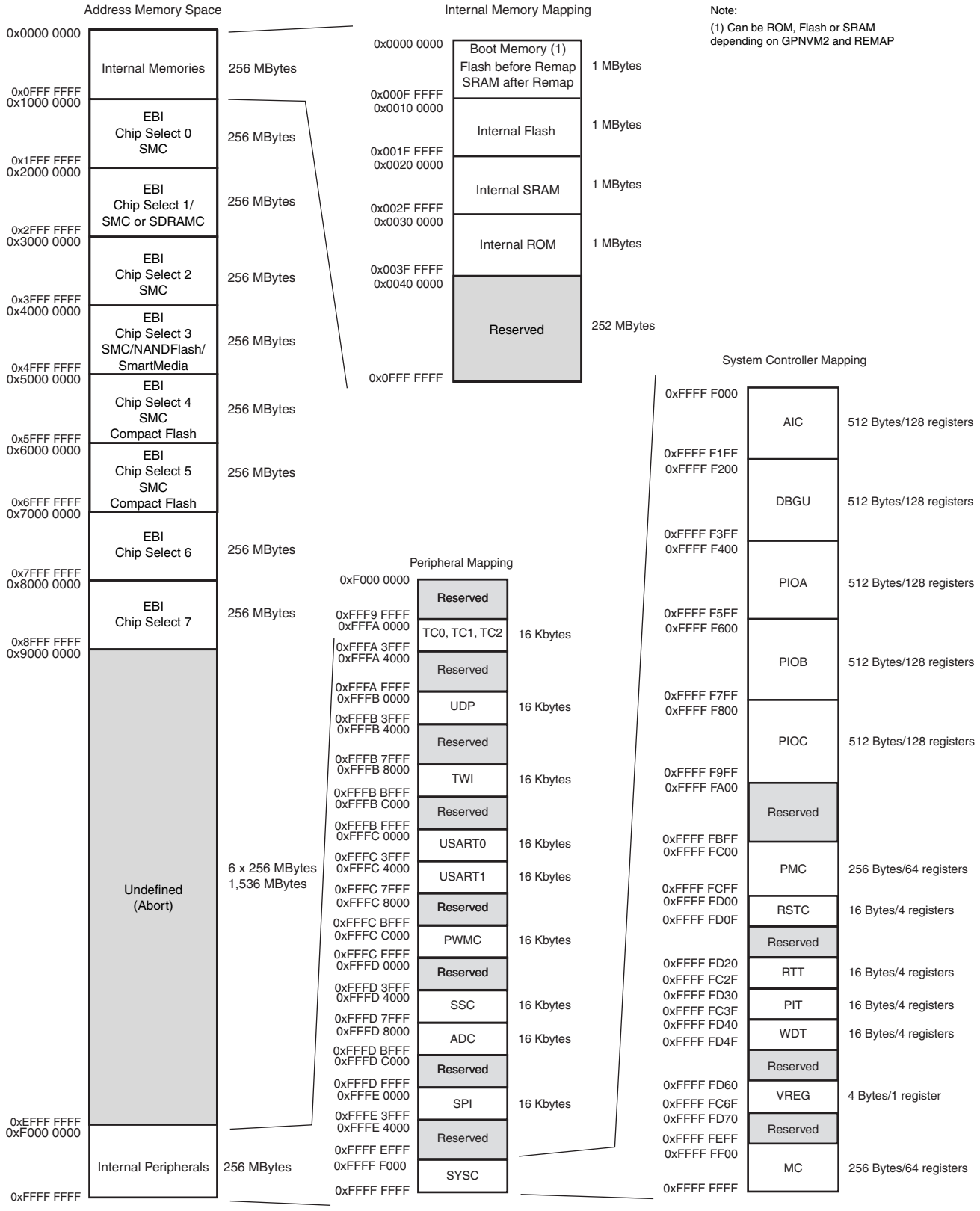
7.6 SDRAM Controller

- Numerous configurations supported
  - **2K, 4K, 8K Row Address Memory Parts**
  - **SDRAM with two or four Internal Banks**
  - **SDRAM with 16- or 32-bit Data Path**
- Programming facilities
  - **Word, half-word, byte access**
  - **Automatic page break when Memory Boundary has been reached**
  - **Multibank Ping-pong Access**
  - **Timing parameters specified by software**
  - **Automatic refresh operation, refresh rate is programmable**
- **Energy-saving capabilities**
  - **Self-refresh, and Low-power Modes supported**
- Error detection
  - **Refresh Error Interrupt**
- **SDRAM Power-up Initialization by software**
- **Latency is set to two clocks (CAS Latency of 1, 3 Not Supported)**
- **Auto Precharge Command not used**
- Mobile SDRAM supported (except for low-power extended mode and deep power-down mode)

7.7 Error Corrected Code Controller

- Tracking the accesses to a NAND Flash device by triggering on the corresponding chip select
- Single bit error correction and 2-bit Random detection.
- Automatic Hamming Code Calculation while writing
  - ECC value available in a register
- Automatic Hamming Code Calculation while reading
  - Error Report, including error flag, correctable error flag and word address being detected erroneous
  - Supports 8- or 16-bit NAND Flash devices with 512-, 1024-, 2048- or 4096-byte pages

Figure 8-1. SAM7SE Memory Mapping



The security bit can only be enabled through the Command “Set Security Bit” of the EFC User Interface. Disabling the security bit can only be achieved by asserting the ERASE pin at 1 and after a full flash erase is performed. When the security bit is deactivated, all accesses to the flash are permitted.

It is important to note that the assertion of the ERASE pin should always be longer than 200 ms.

As the ERASE pin integrates a permanent pull-down, it can be left unconnected during normal operation. However, it is safer to connect it directly to GND for the final application.

8.1.2.5 Non-volatile Brownout Detector Control

Two general purpose NVM (GPNVM) bits are used for controlling the brownout detector (BOD), so that even after a power loss, the brownout detector operations remain in their state.

These two GPNVM bits can be cleared or set respectively through the commands “Clear General-purpose NVM Bit” and “Set General-purpose NVM Bit” of the EFC User Interface.

- GPNVM bit 0 is used as a brownout detector enable bit. Setting the GPNVM bit 0 enables the BOD, clearing it disables the BOD. Asserting ERASE clears the GPNVM bit 0 and thus disables the brownout detector by default.
- GPNVM bit 1 is used as a brownout reset enable signal for the reset controller. Setting the GPNVM bit 1 enables the brownout reset when a brownout is detected, Clearing the GPNVM bit 1 disables the brownout reset. Asserting ERASE disables the brownout reset by default.

8.1.2.6 Calibration Bits

Sixteen NVM bits are used to calibrate the brownout detector and the voltage regulator. These bits are factory configured and cannot be changed by the user. The ERASE pin has no effect on the calibration bits.

8.1.3 Fast Flash Programming Interface

The Fast Flash Programming Interface allows programming the device through either a serial JTAG interface or through a multiplexed fully-handshaked parallel port. It allows gang-programming with market-standard industrial programmers.

The FFPI supports read, page program, page erase, full erase, lock, unlock and protect commands.

The Fast Flash Programming Interface is enabled and the Fast Programming Mode is entered when the TST pin and the PA0 and PA1 pins are all tied high and PA2 tied to low.

- The Flash of the SAM7SE512 is organized in 2048 pages of 256 bytes (dual plane). It reads as 131,072 32-bit words.
- The Flash of the SAM7SE256 is organized in 1024 pages of 256 bytes (single plane). It reads as 65,536 32-bit words.
- The Flash of the SAM7SE32 is organized in 256 pages of 128 bytes (single plane). It reads as 32,768 32-bit words.
- The Flash of the SAM7SE512/256 contains a 256-byte write buffer, accessible through a 32-bit interface.
- The Flash of the SAM7SE32 contains a 128-byte write buffer, accessible through a 32-bit interface.

8.1.4 SAM-BA® Boot

The SAM-BA Boot is a default Boot Program which provides an easy way to program in-situ the on-chip Flash memory.

The SAM-BA Boot Assistant supports serial communication via the DBGU or the USB Device Port.

- Communication via the DBGU supports a wide range of crystals from 3 to 20 MHz via software auto-detection.
- Communication via the USB Device Port is limited to an 18.432 MHz crystal.

The SAM-BA Boot provides an interface with SAM-BA Graphic User Interface (GUI).

The SAM-BA Boot is in ROM and is mapped in Flash at address 0x0 when GPNVM bit 2 is set to 0.

8.2 External Memories

The external memories are accessed through the External Bus Interface.

Refer to the memory map in Figure 8-1 on page 22.

Figure 9-1. System Controller Block Diagram

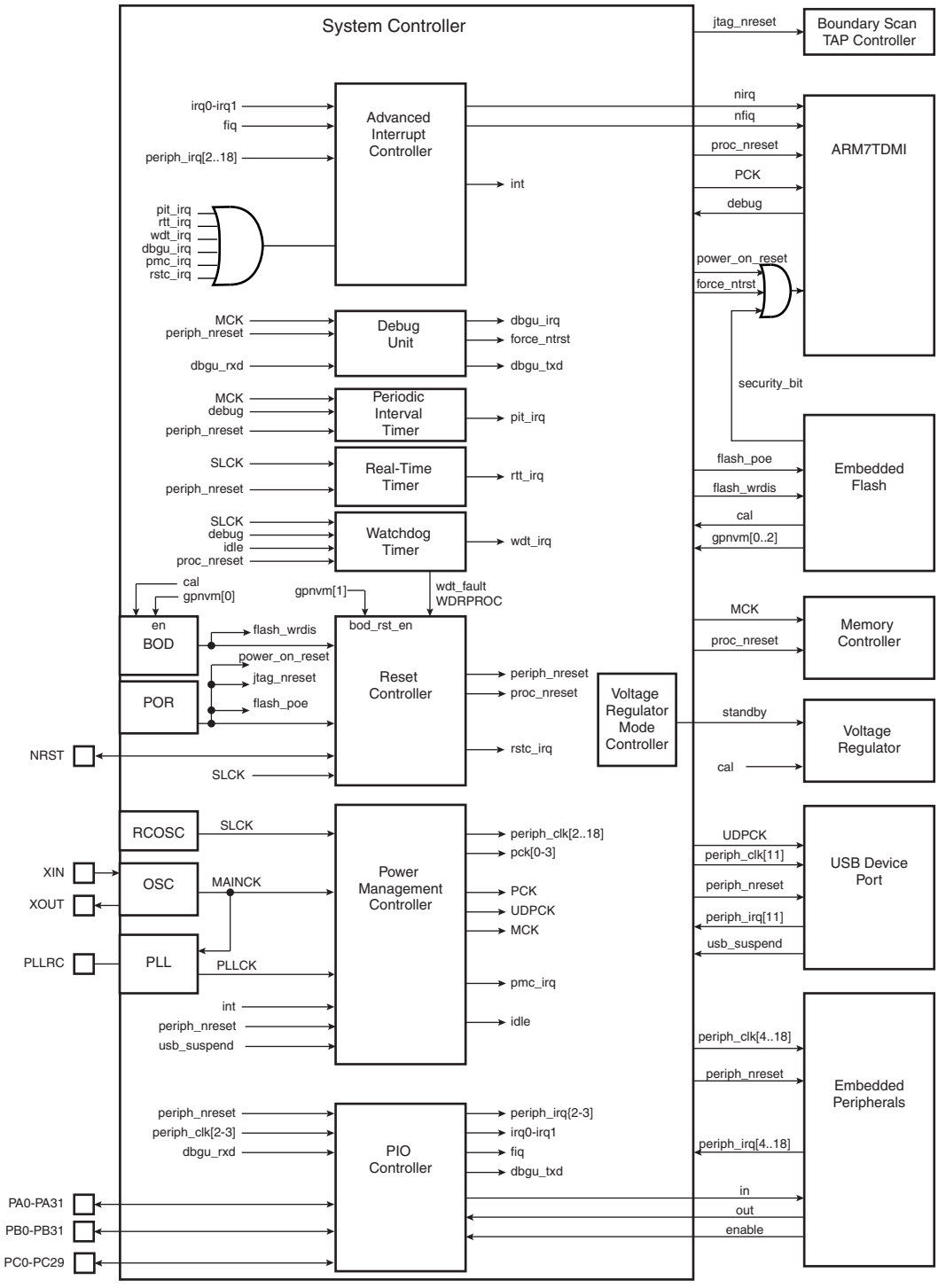
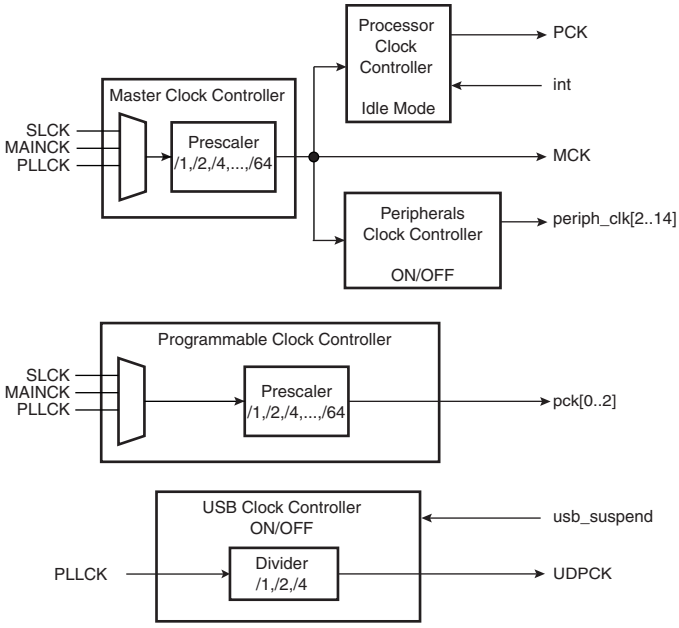


Figure 9-3. Power Management Controller Block Diagram



9.4 Advanced Interrupt Controller

- Controls the interrupt lines (nIRQ and nFIQ) of an ARM Processor
- Individually maskable and vectored interrupt sources
  - Source 0 is reserved for the Fast Interrupt Input (FIQ)
  - Source 1 is reserved for system peripherals (RTT, PIT, EFC, PMC, DBGU, etc.)
  - Other sources control the peripheral interrupts or external interrupts
  - Programmable edge-triggered or level-sensitive internal sources
  - Programmable positive/negative edge-triggered or high/low level-sensitive external sources
- 8-level Priority Controller
  - Drives the normal interrupt nIRQ of the processor
  - Handles priority of the interrupt sources
  - Higher priority interrupts can be served during service of lower priority interrupt
- Vectoring
  - Optimizes interrupt service routine branch and execution
  - One 32-bit vector register per interrupt source
  - Interrupt vector register reads the corresponding current interrupt vector
- Protect Mode
  - Easy debugging by preventing automatic operations
- Fast Forcing
  - Permits redirecting any interrupt source on the fast interrupt
- General Interrupt Mask
  - Provides processor synchronization on events without triggering an interrupt

- Synchronous output, provides Set and Clear of several I/O lines in a single write

9.10 Voltage Regulator Controller

The purpose of this controller is to select the Power Mode of the Voltage Regulator between Normal Mode (bit 0 is cleared) or Standby Mode (bit 0 is set).

10. Peripherals

10.1 User Interface

The User Peripherals are mapped in the 256 MBytes of the address space between 0xF000 0000 and 0xFFFF EFFF. Each peripheral is allocated 16 Kbytes of address space.

A complete memory map is presented in Figure 8-1 on page 22.

10.2 Peripheral Identifiers

The SAM7SE512/256/32 embeds a wide range of peripherals. Table 10-1 defines the Peripheral Identifiers of the SAM7SE512/256/32. Unique peripheral identifiers are defined for both the Advanced Interrupt Controller and the Power Management Controller.

Table 10-1. Peripheral Identifiers

Peripheral ID	Peripheral Mnemonic	Peripheral Name	External Interrupt
0	AIC	Advanced Interrupt Controller	FIQ
1	SYSC[1]		
2	PIOA	Parallel I/O Controller A	
3	PIOB	Parallel I/O Controller B	
4	PIOC	Parallel I/O Controller C	
5	SPI	Serial Peripheral Interface 0	
6	US0	USART 0	
7	US1	USART 1	
8	SSC	Synchronous Serial Controller	
9	TWI	Two-wire Interface	
10	PWMC	PWM Controller	
11	UDP	USB Device Port	
12	TC0	Timer/Counter 0	
13	TC1	Timer/Counter 1	
14	TC2	Timer/Counter 2	
15	ADC[1]	Analog-to Digital Converter	
16-28	reserved		
29	AIC	Advanced Interrupt Controller	IRQ0
30	AIC	Advanced Interrupt Controller	IRQ1

Note: 1. Setting SYSC and ADC bits in the clock set/clear registers of the PMC has no effect. The System Controller is continuously clocked. The ADC clock is automatically started for the first conversion. In Sleep Mode the ADC clock is automatically stopped after each conversion.

10.5 PIO Controller B Multiplexing

Table 10-3. Multiplexing on PIO Controller B

PIO Controller B				Application Usage	
I/O Line	**Peripheral A**	**Peripheral B**	**Comments**	**Function**	**Comments**
PB0	TIOA0	A0/NBS0			
PB1	TIOB0	A1/NBS2			
PB2	SCK0	A2			
PB3	NPCS3	A3			
PB4	TCLK0	A4			
PB5	NPCS3	A5			
PB6	PCK0	A6			
PB7	PWM3	A7			
PB8	ADTRG	A8			
PB9	NPCS1	A9			
PB10	NPCS2	A10			
PB11	PWM0	A11			
PB12	PWM1	A12			
PB13	PWM2	A13			
PB14	PWM3	A14			
PB15	TIOA1	A15			
PB16	TIOB1	A16/BA0			
PB17	PCK1	A17/BA1			
PB18	PCK2	D16			
PB19	FIQ	D17			
PB20	IRQ0	D18			
PB21	PCK1	D19			
PB22	NPCS3	D20			
PB23	PWM0	D21			
PB24	PWM1	D22			
PB25	PWM2	D23			
PB26	TIOA2	D24			
PB27	TIOB2	D25			
PB28	TCLK1	D26			
PB29	TCLK2	D27			
PB30	NPCS2	D28			
PB31	PCK2	D29			

- 8- to 16-bit programmable data length per chip select
- Programmable phase and polarity per chip select
- Programmable transfer delays per chip select, between consecutive transfers and between clock and data
- Programmable delay between consecutive transfers
- Selectable mode fault detection
- Maximum frequency at up to Master Clock

10.8 Two Wire Interface

- Master, Multi-Master and Slave Mode Operation
- Compatibility with standard two-wire serial memories
- One, two or three bytes for slave address
- Sequential read/write operations
- Bit Rate: Up to 400 Kbit/s
- General Call Supported in Slave Mode

10.9 USART

- Programmable Baud Rate Generator
- 5- to 9-bit full-duplex synchronous or asynchronous serial communications
  - 1, 1.5 or 2 stop bits in Asynchronous Mode
  - 1 or 2 stop bits in Synchronous Mode
  - Parity generation and error detection
  - Framing error detection, overrun error detection
  - MSB or LSB first
  - Optional break generation and detection
  - By 8 or by 16 over-sampling receiver frequency
  - Hardware handshaking RTS - CTS
  - Modem Signals Management DTR-DSR-DCD-RI on USART1
  - Receiver time-out and transmitter timeguard
  - Multi-drop Mode with address generation and detection
- RS485 with driver control signal
- ISO7816, T = 0 or T = 1 Protocols for interfacing with smart cards
  - NACK handling, error counter with repetition and iteration limit
- IrDA® modulation and demodulation
  - Communication at up to 115.2 Kbps
- Test Modes
  - Remote Loopback, Local Loopback, Automatic Echo

10.10 Serial Synchronous Controller

- Provides serial synchronous communication links used in audio and telecom applications
- Contains an independent receiver and transmitter and a common clock divider

- Offers a configurable frame sync and data length
- Receiver and transmitter can be programmed to start automatically or on detection of different event on the frame sync signal
- Receiver and transmitter include a data signal, a clock signal and a frame synchronization signal

10.11 Timer Counter

- Three 16-bit Timer Counter Channels
  - Two output compare or one input capture per channel
- Wide range of functions including:
  - Frequency measurement
  - Event counting
  - Interval measurement
  - Pulse generation
  - Delay timing
  - Pulse Width Modulation
  - Up/down capabilities
- Each channel is user-configurable and contains:
  - Three external clock inputs
  - Five internal clock inputs, as defined in Table 10-4

Table 10-4. Timer Counter Clocks Assignment

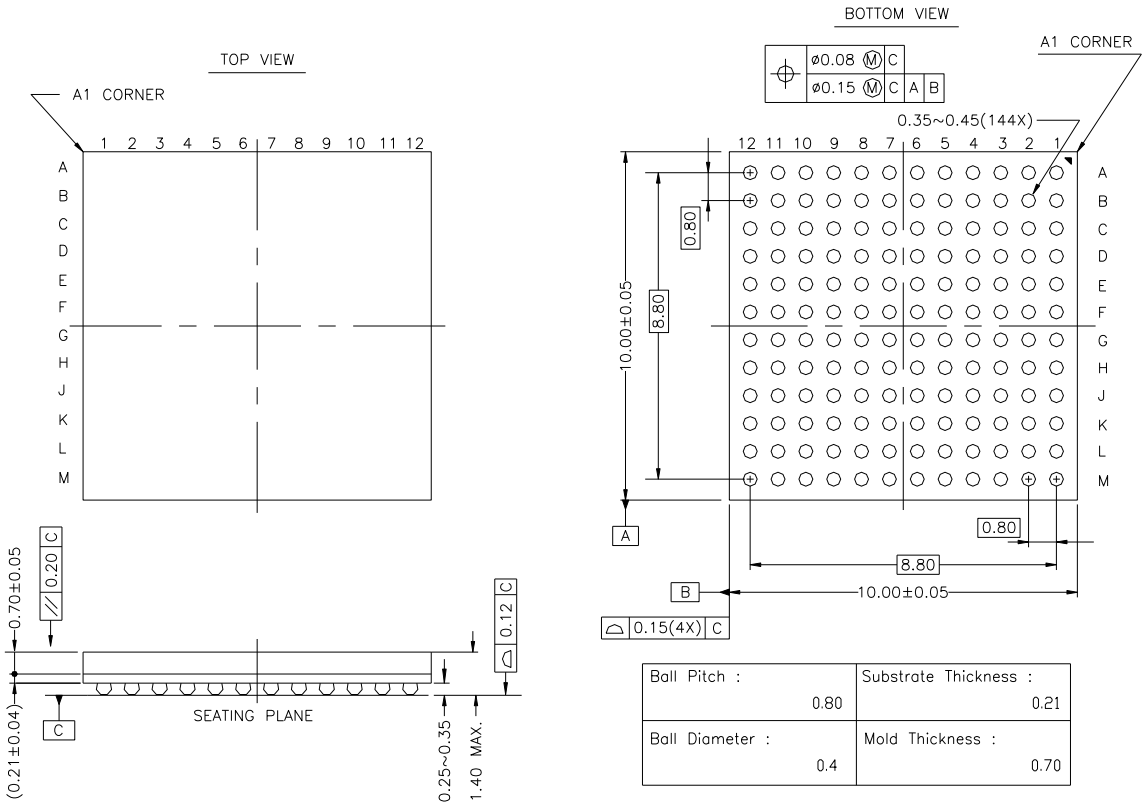
TC Clock input	Clock
TIMER_CLOCK1	MCK/2
TIMER_CLOCK2	MCK/8
TIMER_CLOCK3	MCK/32
TIMER_CLOCK4	MCK/128
TIMER_CLOCK5	MCK/1024

  - Two multi-purpose input/output signals
  - Two global registers that act on all three TC channels

10.12 PWM Controller

- Four channels, one 16-bit counter per channel
- Common clock generator, providing thirteen different clocks
  - One Modulo n counter providing eleven clocks
  - Two independent linear dividers working on modulo n counter outputs
- Independent channel programming
  - Independent enable/disable commands
  - Independent clock selection
  - Independent period and duty cycle, with double buffering
  - Programmable selection of the output waveform polarity
  - Programmable center or left aligned output waveform

Figure 11-2. 144-ball LFBGA Package Drawing



All dimensions are in mm

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