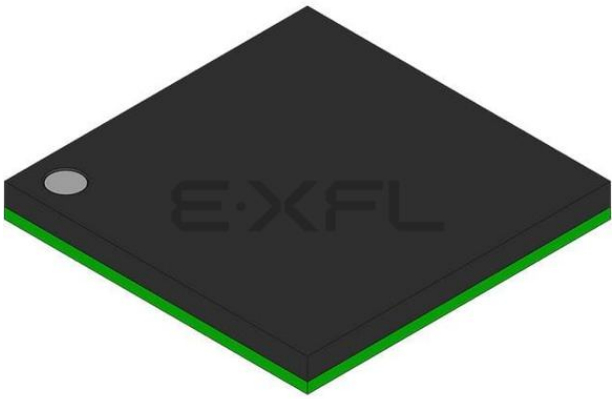

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	55MHz
Connectivity	EBI/EMI, I²C, SPI, SSC, UART/USART, USB
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	88
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 1.95V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LFBGA
Supplier Device Package	144-BGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/atmel/at91sam7se32-cu-999

3. Signal Description

Table 3-1. Signal Description List

Signal Name	Function	Type	Active Level	Comments
Power				
VDDIN	Voltage Regulator and ADC Power Supply Input	Power		3V to 3.6V
VDDOUT	Voltage Regulator Output	Power		1.85V
VDDFLASH	Flash and USB Power Supply	Power		3V to 3.6V
VDDIO	I/O Lines Power Supply	Power		3V to 3.6V or 1.65V to 1.95V
VDDCORE	Core Power Supply	Power		1.65V to 1.95V
VDDPLL	PLL	Power		1.65V to 1.95V
GND	Ground	Ground		
Clocks, Oscillators and PLLs				
XIN	Main Oscillator Input	Input		
XOUT	Main Oscillator Output	Output		
PLLRC	PLL Filter	Input		
PCK0 - PCK2	Programmable Clock Output	Output		
ICE and JTAG				
TCK	Test Clock	Input		No pull-up resistor
TDI	Test Data In	Input		No pull-up resistor
TDO	Test Data Out	Output		
TMS	Test Mode Select	Input		No pull-up resistor.
JTAGSEL	JTAG Selection	Input		Pull-down resistor(1)
Flash Memory				
ERASE	Flash and NVM Configuration Bits Erase Command	Input	High	Pull-down resistor (1)
Reset/Test				
NRST	Microcontroller Reset	I/O	Low	Open drain with pull-up resistor (1)
TST	Test Mode Select	Input	High	Pull-down resistor (1)
Debug Unit				
DRXD	Debug Receive Data	Input		
DTXD	Debug Transmit Data	Output		
AIC				
IRQ0 - IRQ1	External Interrupt Inputs	Input		
FIQ	Fast Interrupt Input	Input		

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Comments
PIO				
PA0 - PA31	Parallel IO Controller A	I/O		Pulled-up input at reset
PB0 - PB31	Parallel IO Controller B	I/O		Pulled-up input at reset
PC0 - PC23	Parallel IO Controller C	I/O		Pulled-up input at reset
USB Device Port				
DDM	USB Device Port Data -	Analog		
DDP	USB Device Port Data +	Analog		
USART				
SCK0 - SCK1	Serial Clock	I/O		
TXD0 - TXD1	Transmit Data	I/O		
RXD0 - RXD1	Receive Data	Input		
RTS0 - RTS1	Request To Send	Output		
CTS0 - CTS1	Clear To Send	Input		
DCD1	Data Carrier Detect	Input		
DTR1	Data Terminal Ready	Output		
DSR1	Data Set Ready	Input		
RI1	Ring Indicator	Input		
Synchronous Serial Controller				
TD	Transmit Data	Output		
RD	Receive Data	Input		
TK	Transmit Clock	I/O		
RK	Receive Clock	I/O		
TF	Transmit Frame Sync	I/O		
RF	Receive Frame Sync	I/O		
Timer/Counter				
TCLK0 - TCLK2	External Clock Inputs	Input		
TIOA0 - TIOA2	Timer Counter I/O Line A	I/O		
TIOB0 - TIOB2	Timer Counter I/O Line B	I/O		
PWM Controller				
PWM0 - PWM3	PWM Channels	Output		
Serial Peripheral Interface				
MISO	Master In Slave Out	I/O		
MOSI	Master Out Slave In	I/O		
SPCK	SPI Serial Clock	I/O		
NPCS0	SPI Peripheral Chip Select 0	I/O	Low	
NPCS1-NPCS3	SPI Peripheral Chip Select 1 to 3	Output	Low	

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Comments
Two-Wire Interface				
TWD	Two-wire Serial Data	I/O		
TWCK	Two-wire Serial Clock	I/O		
Analog-to-Digital Converter				
AD0-AD3	Analog Inputs	Analog		Digital pulled-up inputs at reset
AD4-AD7	Analog Inputs	Analog		Analog Inputs
ADTRG	ADC Trigger	Input		
ADVREF	ADC Reference	Analog		
Fast Flash Programming Interface				
PGMEN0-PGMEN2	Programming Enabling	Input		
PGMM0-PGMM3	Programming Mode	Input		
PGMD0-PGMD15	Programming Data	I/O		
PGMRDY	Programming Ready	Output	High	
PGMNVALID	Data Direction	Output	Low	
PGMNOE	Programming Read	Input	Low	
PGMCK	Programming Clock	Input		
PGMNCMD	Programming Command	Input	Low	
External Bus Interface				
D[31:0]	Data Bus	I/O		
A[22:0]	Address Bus	Output		
NWAIT	External Wait Signal	Input	Low	
Static Memory Controller				
NCS[7:0]	Chip Select Lines	Output	Low	
NWR[1:0]	Write Signals	Output	Low	
NRD	Read Signal	Output	Low	
NWE	Write Enable	Output	Low	
NUB	NUB: Upper Byte Select	Output	Low	
NLB	NLB: Lower Byte Select	Output	Low	
EBI for CompactFlash Support				
CFCE[2:1]	CompactFlash Chip Enable	Output	Low	
CFOE	CompactFlash Output Enable	Output	Low	
CFWE	CompactFlash Write Enable	Output	Low	
CFIOR	CompactFlash I/O Read Signal	Output	Low	
CFIOW	CompactFlash I/O Write Signal	Output	Low	
CFRNW	CompactFlash Read Not Write Signal	Output		
CFCS[1:0]	CompactFlash Chip Select Lines	Output	Low	

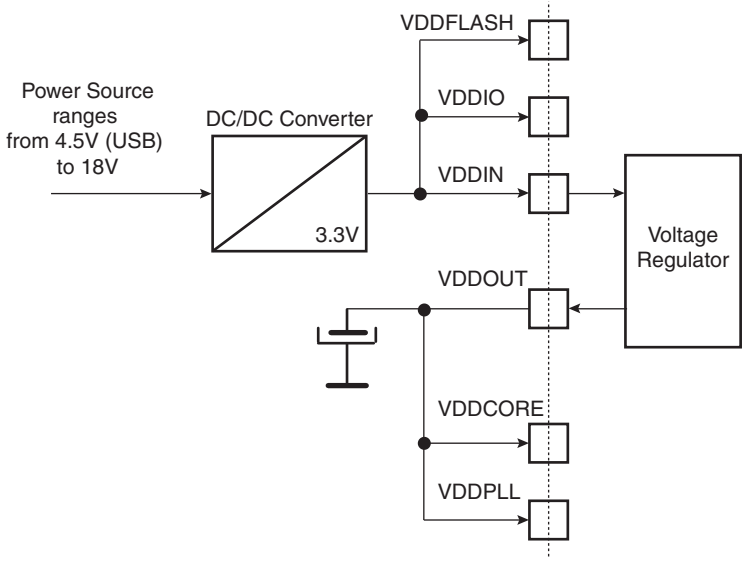
- One external 2.2 µF (or 3.3 µF) X7R capacitor should be connected between VDDOUT and GND.

Adequate input supply decoupling is mandatory for VDDIN in order to improve startup stability and reduce source voltage drop. The input decoupling capacitor should be placed close to the chip. For example, two capacitors can be used in parallel: 100 nF NPO and 4.7 µF X7R.

5.4 Typical Powering Schematics

The SAM7SE512/256/32 supports a 3.3V single supply mode. The internal regulator input connected to the 3.3V source and its output feeds VDDCORE and the VDDPLL. Figure 5-1 shows the power schematics to be used for USB bus-powered systems.

Figure 5-1. 3.3V System Single Power Supply Schematic



7. Processor and Architecture

7.1 ARM7TDMI Processor

- RISC processor based on ARMv4T Von Neumann architecture
  - Runs at up to 55 MHz, providing 0.9 MIPS/MHz (core supplied with 1.8V)
- Two instruction sets
  - ARM® high-performance 32-bit instruction set
  - Thumb® high code density 16-bit instruction set
- Three-stage pipeline architecture
  - Instruction Fetch (F)
  - Instruction Decode (D)
  - Execute (E)

7.2 Debug and Test Features

- EmbeddedICE™ (Integrated embedded in-circuit emulator)
  - Two watchpoint units
  - Test access port accessible through a JTAG protocol
  - Debug communication channel
- Debug Unit
  - Two-pin UART
  - Debug communication channel interrupt handling
  - Chip ID Register
- IEEE1149.1 JTAG Boundary-scan on all digital pins

7.3 Memory Controller

- Programmable Bus Arbiter
  - Handles requests from the ARM7TDMI and the Peripheral DMA Controller
- Address decoder provides selection signals for
  - Four internal 1 Mbyte memory areas
  - One 256-Mbyte embedded peripheral area
  - Eight external 256-Mbyte memory areas
- Abort Status Registers
  - Source, Type and all parameters of the access leading to an abort are saved
  - Facilitates debug by detection of bad pointers
- Misalignment Detector
  - Alignment checking of all data accesses
  - Abort generation in case of misalignment
- Remap Command
  - Remaps the SRAM in place of the embedded non-volatile memory
  - Allows handling of dynamic exception vectors
- 16-area Memory Protection Unit (Internal Memory and peripheral protection only)

  - Individually programmable size between 1K Byte and 1M Byte
  - Individually programmable protection against write and/or user access
  - Peripheral protection against write and/or user access
- Embedded Flash Controller
  - Embedded Flash interface, up to three programmable wait states
  - Prefetch buffer, buffering and anticipating the 16-bit requests, reducing the required wait states
  - Key-protected program, erase and lock/unlock sequencer
  - Single command for erasing, programming and locking operations
  - Interrupt generation in case of forbidden operation

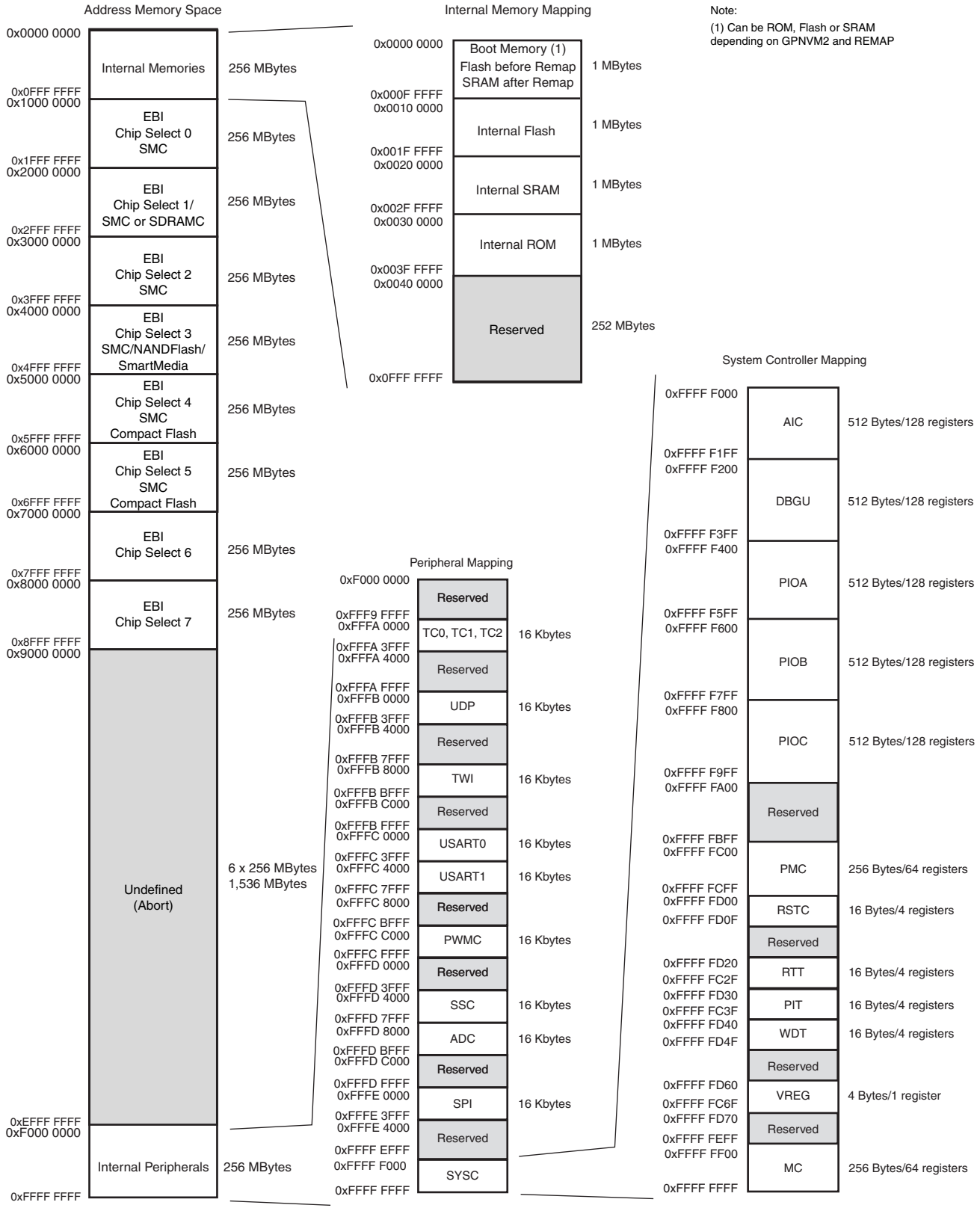
7.4 External Bus Interface

- Integrates Three External Memory Controllers:
  - Static Memory Controller
  - SDRAM Controller
  - ECC Controller
- Additional Logic for NAND Flash and CompactFlash® Support
  - NAND Flash support: 8-bit as well as 16-bit devices are supported
  - CompactFlash support: all modes (Attribute Memory, Common Memory, I/O, True IDE) are supported but the signals _IOIS16 (I/O and True IDE modes) and -ATA SEL (True IDE mode) are not handled.
- Optimized External Bus:
  - 16- or 32-bit Data Bus (32-bit Data Bus for SDRAM only)
  - Up to 23-bit Address Bus, Up to 8-Mbytes Addressable
  - Up to 8 Chip Selects, each reserved to one of the eight Memory Areas
  - Optimized pin multiplexing to reduce latencies on External Memories
- Configurable Chip Select Assignment:
  - Static Memory Controller on NCS0
  - SDRAM Controller or Static Memory Controller on NCS1
  - Static Memory Controller on NCS2, Optional CompactFlash Support
  - Static Memory Controller on NCS3, NCS5 - NCS6, Optional NAND Flash Support
  - Static Memory Controller on NCS4, Optional CompactFlash Support
  - Static Memory Controller on NCS7

7.5 Static Memory Controller

- External memory mapping, 512-Mbyte address space
- 8-, or 16-bit Data Bus
- Up to 8 Chip Select Lines
- Multiple Access Modes supported
  - Byte Write or Byte Select Lines
  - Two different Read Protocols for each Memory Bank

Figure 8-1. SAM7SE Memory Mapping



The Flash benefits from the integration of a power reset cell and from the brownout detector. This prevents code corruption during power supply changes, even in the worst conditions.

8.1.2.2 *Embedded Flash Controller*

The Embedded Flash Controller (EFC) manages accesses performed by the masters of the system. It enables reading the Flash and writing the write buffer. It also contains a User Interface, mapped within the Memory Controller on the APB. The User Interface allows:

- programming of the access parameters of the Flash (number of wait states, timings, etc.)
- starting commands such as full erase, page erase, page program, NVM bit set, NVM bit clear, etc.
- getting the end status of the last command
- getting error status
- programming interrupts on the end of the last commands or on errors

The Embedded Flash Controller also provides a dual 32-bit Prefetch Buffer that optimizes 16-bit access to the Flash. This is particularly efficient when the processor is running in Thumb mode.

- Two EFCs (EFC0 and EFC1) are embedded in the SAM7SE512 to control each plane of 256 KBytes. Dual plane organization allows concurrent Read and Program.
- One EFC (EFC0) is embedded in the SAM7SE256 to control the single plane 256 KBytes.
- One EFC (EFC0) is embedded in the SAM7SE32 to control the single plane 32 KBytes.

8.1.2.3 *Lock Regions*

The SAM7SE512 Embedded Flash Controller manages 32 lock bits to protect 32 regions of the flash against inadvertent flash erasing or programming commands. The SAM7SE512 contains 32 lock regions and each lock region contains 64 pages of 256 bytes. Each lock region has a size of 16 Kbytes.

The SAM7SE256 Embedded Flash Controller manages 16 lock bits to protect 16 regions of the flash against inadvertent flash erasing or programming commands. The SAM7SE256 contains 16 lock regions and each lock region contains 64 pages of 256 bytes. Each lock region has a size of 16 Kbytes.

The SAM7SE32 Embedded Flash Controller manages 8 lock bits to protect 8 regions of the flash against inadvertent flash erasing or programming commands. The SAM7SE32 contains 8 lock regions and each lock region contains 32 pages of 128 bytes. Each lock region has a size of 4 Kbytes.

If a locked-region's erase or program command occurs, the command is aborted and the EFC triggers an interrupt.

The 32 (SAM7SE512), 16 (SAM7SE256) or 8 (SAM7SE32) NVM bits are software programmable through the EFC User Interface. The command "Set Lock Bit" enables the protection. The command "Clear Lock Bit" unlocks the lock region.

Asserting the ERASE pin clears the lock bits, thus unlocking the entire Flash.

8.1.2.4 *Security Bit Feature*

The SAM7SE512/256/32 features a security bit, based on a specific NVM-bit. When the security is enabled, any access to the Flash, either through the ICE interface or through the Fast Flash Programming Interface, is forbidden.

8.1.4 SAM-BA® Boot

The SAM-BA Boot is a default Boot Program which provides an easy way to program in-situ the on-chip Flash memory.

The SAM-BA Boot Assistant supports serial communication via the DBGU or the USB Device Port.

- Communication via the DBGU supports a wide range of crystals from 3 to 20 MHz via software auto-detection.
- Communication via the USB Device Port is limited to an 18.432 MHz crystal.

The SAM-BA Boot provides an interface with SAM-BA Graphic User Interface (GUI).

The SAM-BA Boot is in ROM and is mapped in Flash at address 0x0 when GPNVM bit 2 is set to 0.

8.2 External Memories

The external memories are accessed through the External Bus Interface.

Refer to the memory map in Figure 8-1 on page 22.

9. System Controller

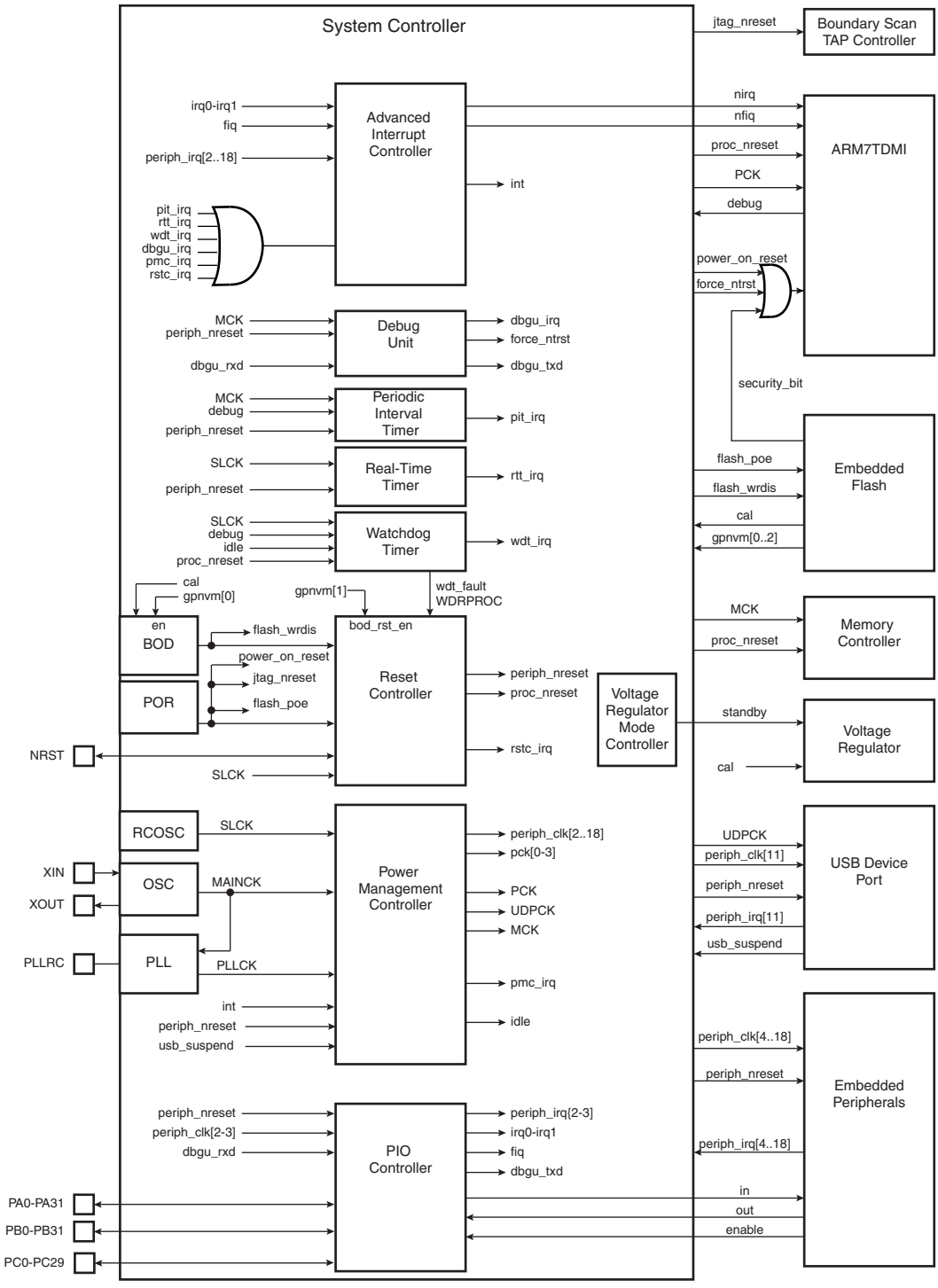
The System Controller manages all vital blocks of the microcontroller: interrupts, clocks, power, time, debug and reset.

The System Controller peripherals are all mapped to the highest 4 Kbytes of address space, between addresses 0xFFFF F000 and 0xFFFF FFFF.

Figure 9-1 on page 29 shows the System Controller Block Diagram.

Figure 8-1 on page 22 shows the mapping of the User Interface of the System Controller peripherals. Note that the Memory Controller configuration user interface is also mapped within this address space.

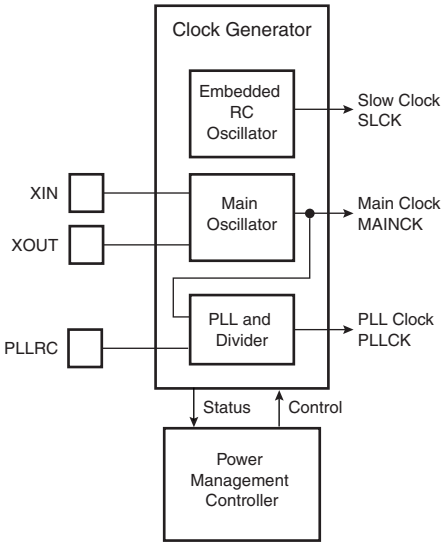
Figure 9-1. System Controller Block Diagram



- Main Oscillator frequency ranges between 3 and 20 MHz
- Main Oscillator can be bypassed
- PLL output ranges between 80 and 220 MHz

It provides SLCK, MAINCK and PLLCK.

Figure 9-2. Clock Generator Block Diagram



9.3 Power Management Controller

The Power Management Controller uses the Clock Generator outputs to provide:

- the Processor Clock PCK
- the Master Clock MCK
- the USB Clock UDPCK
- all the peripheral clocks, independently controllable
- three programmable clock outputs

The Master Clock (MCK) is programmable from a few hundred Hz to the maximum operating frequency of the device.

The Processor Clock (PCK) switches off when entering processor idle mode, thus allowing reduced power consumption while waiting for an interrupt.

9.5 Debug Unit

- Comprises:
  - One two-pin UART
  - One Interface for the Debug Communication Channel (DCC) support
  - One set of Chip ID Registers
  - One Interface providing ICE Access Prevention
- Two-pin UART
  - USART-compatible User Interface
  - Programmable Baud Rate Generator
  - Parity, Framing and Overrun Error
  - Automatic Echo, Local Loopback and Remote Loopback Channel Modes
- Debug Communication Channel Support
  - Offers visibility of COMMRX and COMMTX signals from the ARM Processor
- Chip ID Registers
  - Identification of the device revision, sizes of the embedded memories, set of peripherals
  - Chip ID is 0x272A 0A40 (VERSION 0) for SAM7SE512
  - Chip ID is 0x272A 0940 (VERSION 0) for SAM7SE256
  - Chip ID is 0x2728 0340 (VERSION 0) for SAM7SE32

9.6 Periodic Interval Timer

- 20-bit programmable counter plus 12-bit interval counter

9.7 Watchdog Timer

- 12-bit key-protected Programmable Counter running on prescaled SLCK
- Provides reset or interrupt signals to the system
- Counter may be stopped while the processor is in debug state or in idle mode

9.8 Real-time Timer

- 32-bit free-running counter with alarm running on prescaled SLCK
- Programmable 16-bit prescaler for SLCK accuracy compensation

9.9 PIO Controllers

- Three PIO Controllers. PIO A and B each control 32 I/O lines and PIO C controls 24 I/O lines.
- Fully programmable through set/clear registers
- Multiplexing of two peripheral functions per I/O line
- For each I/O line (whether assigned to a peripheral or used as general-purpose I/O)
  - Input change interrupt
  - Half a clock period glitch filter
  - Multi-drive option enables driving in open drain
  - Programmable pull-up on each I/O line
  - Pin data status register, supplies visibility of the level on the pin at any time

10.4 PIO Controller A Multiplexing

Table 10-2. Multiplexing on PIO Controller A

PIO Controller A				Application Usage	
I/O Line	**Peripheral A**	**Peripheral B**	**Comments**	**Function**	**Comments**
PA0	PWM0	A0/NBS0	High-Drive		
PA1	PWM1	A1/NBS2	High-Drive		
PA2	PWM2	A2	High-Drive		
PA3	TWD	A3	High-Drive		
PA4	TWCK	A4			
PA5	RXD0	A5			
PA6	TXD0	A6			
PA7	RTS0	A7			
PA8	CTS0	A8			
PA9	DRXD	A9			
PA10	DTXD	A10			
PA11	NPCS0	A11			
PA12	MISO	A12			
PA13	MOSI	A13			
PA14	SPCK	A14			
PA15	TF	A15			
PA16	TK	A16/BA0			
PA17	TD	A17/BA1	AD0		
PA18	RD	NBS3/CFIOW	AD1		
PA19	RK	NCS4/CFCS0	AD2		
PA20	RF	NCS2/CFCS1	AD3		
PA21	RXD1	NCS6/CFCE2			
PA22	TXD1	NCS5/CFCE1			
PA23	SCK1	NWR1/NBS1/CFIOR			
PA24	RTS1	SDA10			
PA25	CTS1	SDCKE			
PA26	DCD1	NCS1/SDCS			
PA27	DTR1	SDWE			
PA28	DSR1	CAS			
PA29	RI1	RAS			
PA30	IRQ1	D30			
PA31	NPCS1	D31			

10.6 PIO Controller C Multiplexing

Multiplexing on PIO Controller C

PIO Controller C				Application Usage	
I/O Line	Peripheral A	Peripheral B	Comments	Function	Comments
PC0	D0				
PC1	D1				
PC2	D2				
PC3	D3				
PC4	D4				
PC5	D5				
PC6	D6				
PC7	D7				
PC8	D8	RTS1			
PC9	D9	DTR1			
PC10	D10	PCK0			
PC11	D11	PCK1			
PC12	D12	PCK2			
PC13	D13				
PC14	D14	NPCS1			
PC15	D15	NCS3/NANDCS			
PC16	A18	NWAIT			
PC17	A19	NANDOE			
PC18	A20	NANDWE			
PC19	A21/NANDALE				
PC20	A22/REG/NANDCLE	NCS7			
PC21		NWR0/NWE/CFWE			
PC22		NRD/CFOE			
PC23	CFRNW	NCS0			

10.7 Serial Peripheral Interface

- Supports communication with external serial devices
  - Four chip selects with external decoder allow communication with up to 15 peripherals
  - Serial memories, such as DataFlash® and 3-wire EEPROMs
  - Serial peripherals, such as ADCs, DACs, LCD Controllers, CAN Controllers and Sensors
  - External co-processors
- Master or slave serial peripheral bus interface

10.13 USB Device Port

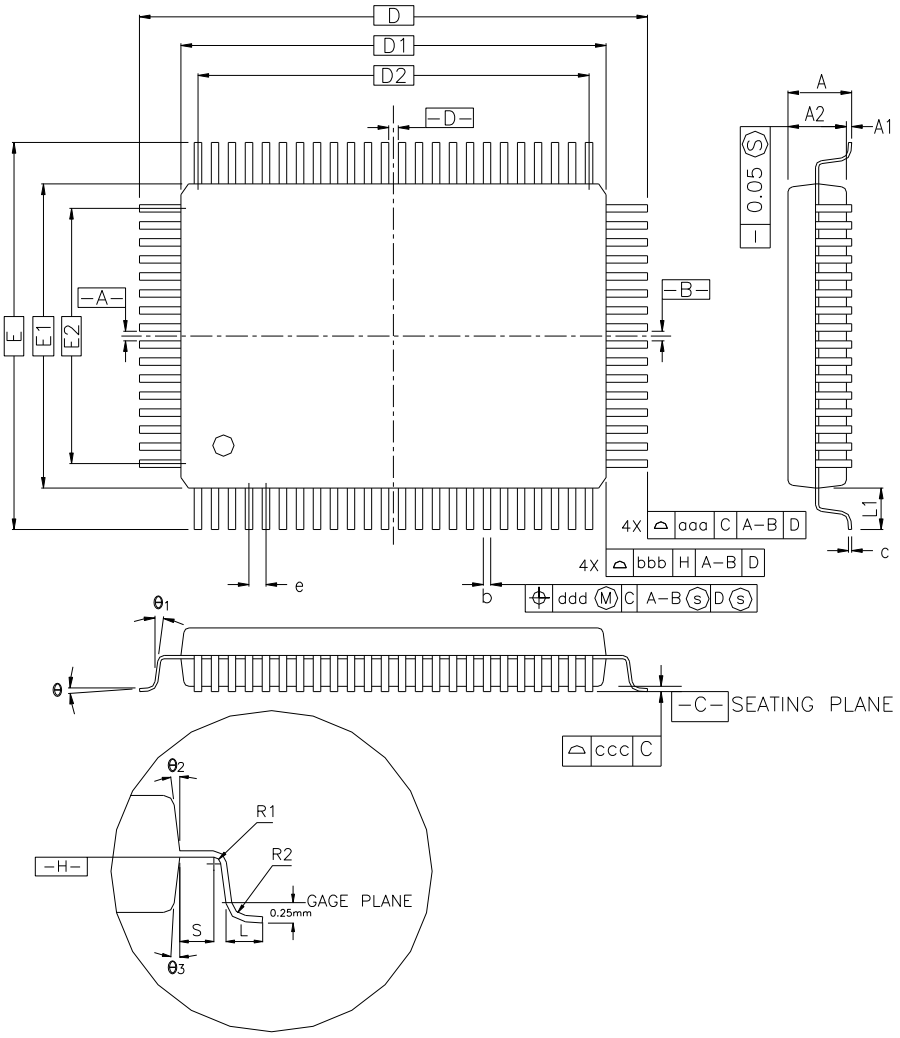
- USB V2.0 full-speed compliant,12 Mbits per second.
- Embedded USB V2.0 full-speed transceiver
- Embedded 2688-byte dual-port RAM for endpoints
- Eight endpoints
  - Endpoint 0: 64bytes
  - Endpoint 1 and 2: 64 bytes ping-pong
  - Endpoint 3: 64 bytes
  - Endpoint 4 and 5: 512 bytes ping-pong
  - Endpoint 6 and 7: 64 bytes ping-pong
  - Ping-pong Mode (two memory banks) for Isochronous and bulk endpoints
- Suspend/resume logic
- Integrated Pull-up on DDP

10.14 Analog-to-Digital Converter

- 8-channel ADC
- 10-bit 384 Ksamples/sec. or 8-bit 583 Ksamples/sec. Successive Approximation Register ADC
- ±2 LSB Integral Non Linearity, ±1 LSB Differential Non Linearity
- Integrated 8-to-1 multiplexer, offering eight independent 3.3V analog inputs
- External voltage reference for better accuracy on low voltage inputs
- Individual enable and disable of each channel
- Multiple trigger sources
  - Hardware or software trigger
  - External trigger pin
  - Timer Counter 0 to 2 outputs TIOA0 to TIOA2 trigger
- Sleep Mode and conversion sequencer
  - Automatic wakeup on trigger and back to sleep mode after conversions of all enabled channels
- Each analog input shared with digital signals

11. Package Drawings

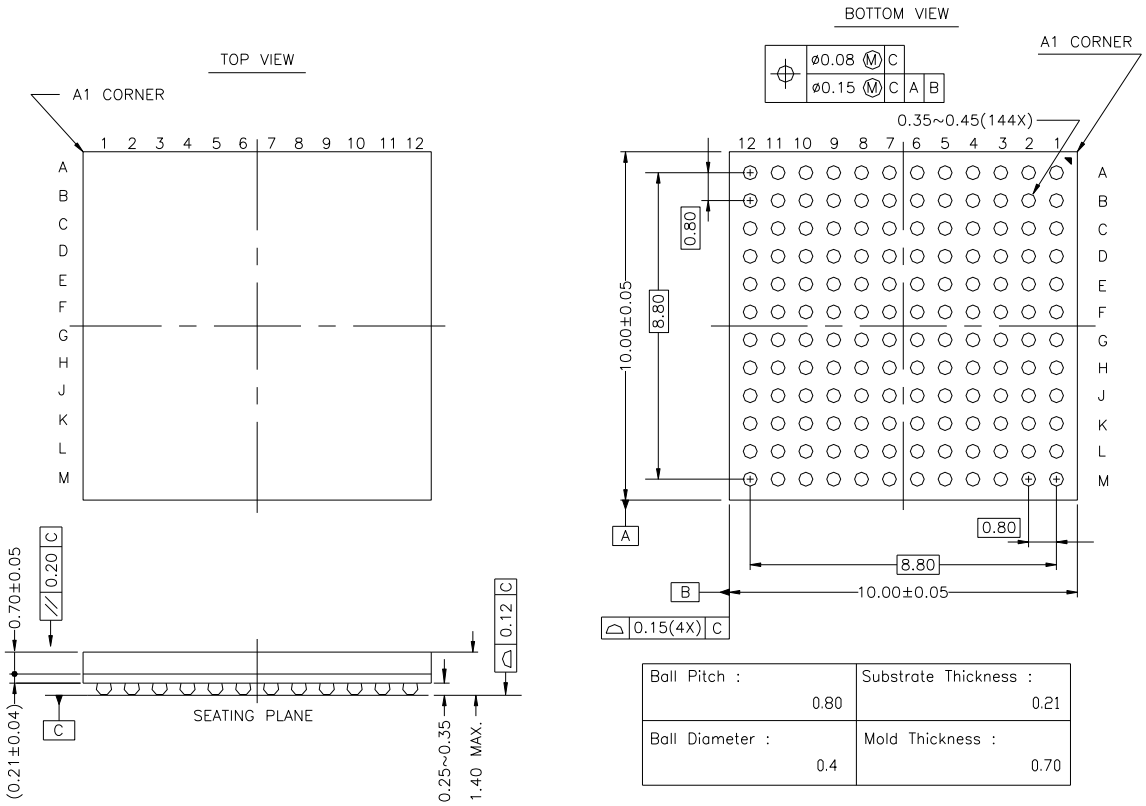
Figure 11-1. 128-lead LQFP Package Drawing



COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A_1	0.05	—	0.15	0.002	—	0.006
A_2	1.35	1.40	1.45	0.053	0.055	0.057
D	22.00 BSC.			0.866 BSC.		
D_1	20.00 BSC.			0.787 BSC.		
E	16.00 BSC.			0.630 BSC.		
E_1	14.00 BSC.			0.551 BSC.		
R_2	0.08	—	0.20	0.003	—	0.008
R_1	0.08	—	—	0.003	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ_1	0°	—	—	0°	—	—
θ_2	11°	12°	13°	11°	12°	13°
θ_3	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BSC.			0.020 BSC.		
D2	18.50			0.728		
E2	12.50			0.492		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

Figure 11-2. 144-ball LFBGA Package Drawing



All dimensions are in mm

12. Ordering Information

Table 12-1. Ordering Information

Ordering Code	MRL	Package	Package Type	Temperature Operating Range
AT91SAM7SE512B-AU	B	LQFP128	Green	Industrial (-40· C to 85· C)
AT91SAM7SE256B-AU	B	LQFP128	Green	Industrial (-40· C to 85· C)
AT91SAM7SE32B-AU	B	LQFP128	Green	Industrial (-40· C to 85· C)
AT91SAM7SE512B-CU	B	LFBGA144	Green	Industrial (-40· C to 85· C)
AT91SAM7SE256B-CU	B	LFBGA144	Green	Industrial (-40· C to 85· C)
AT91SAM7SE32B-CU	B	LFBGA144	Green	Industrial (-40· C to 85· C)
AT91SAM7SE512-AU	A	LQFP128	Green	Industrial (-40· C to 85· C)
AT91SAM7SE256-AU	A	LQFP128	Green	Industrial (-40· C to 85· C)
AT91SAM7SE32-AU	A	LQFP128	Green	Industrial (-40· C to 85· C)
AT91SAM7SE512-CU	A	LFBGA144	Green	Industrial (-40· C to 85· C)
AT91SAM7SE256-CU	A	LFBGA144	Green	Industrial (-40· C to 85· C)
AT91SAM7SE32-CU	A	LFBGA144	Green	Industrial (-40· C to 85· C)

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