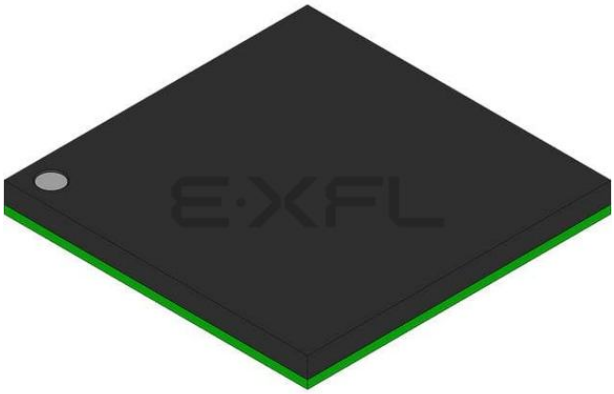

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

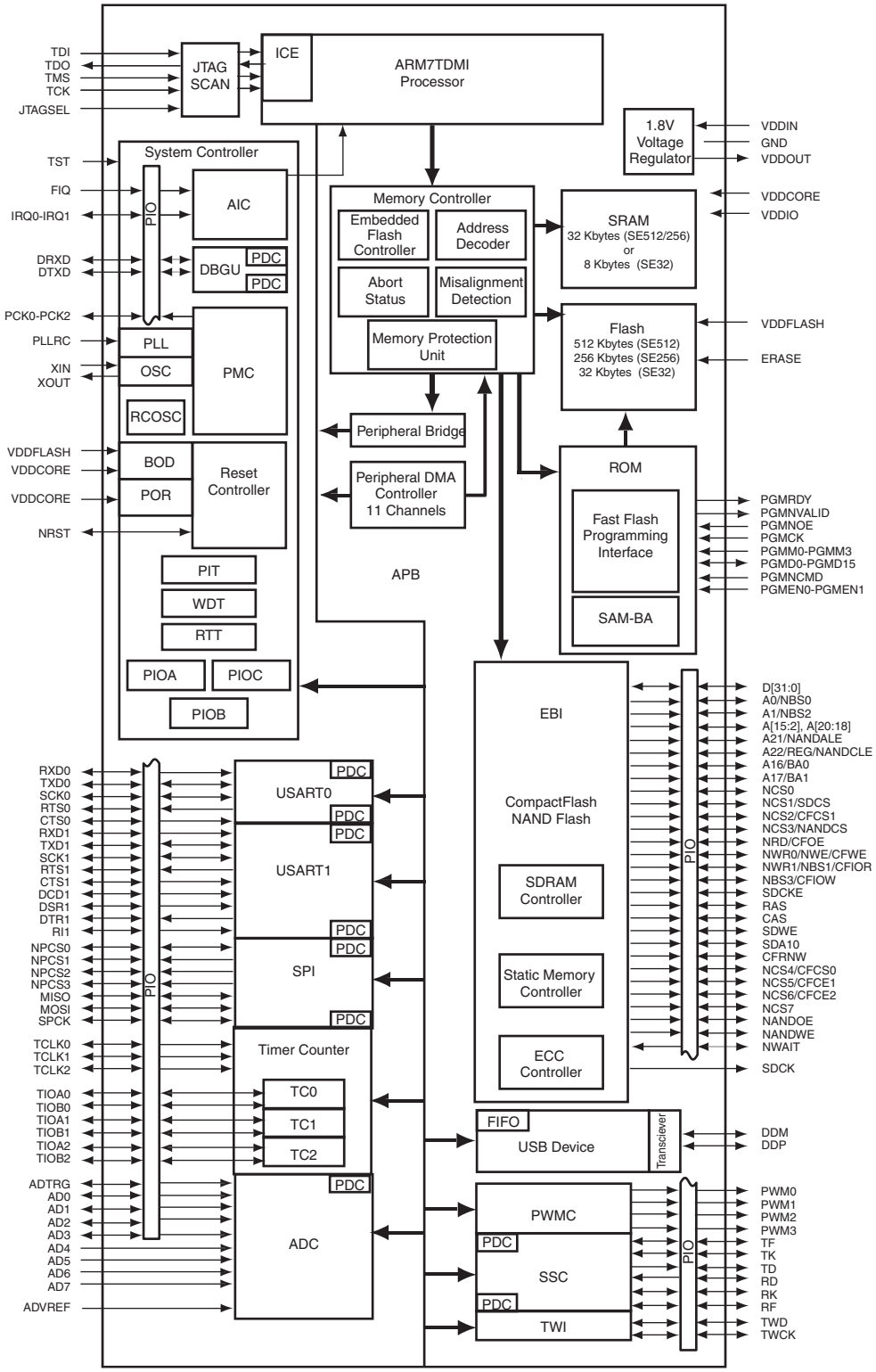
Details	
Product Status	Obsolete
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	55MHz
Connectivity	EBI/EMI, I²C, SPI, SSC, UART/USART, USB
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	88
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 1.95V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LFBGA
Supplier Device Package	144-BGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/atmel/at91sam7se32-cu

- Provides Reset or Interrupt Signals to the System
- Counter May Be Stopped While the Processor is in Debug State or in Idle Mode

- Real-time Timer (RTT)
  - 32-bit Free-running Counter with Alarm
  - Runs Off the Internal RC Oscillator
- Three Parallel Input/Output Controllers (PIO)
  - Eighty-eight Programmable I/O Lines Multiplexed with up to Two Peripheral I/Os
  - Input Change Interrupt Capability on Each I/O Line
  - Individually Programmable Open-drain, Pull-up Resistor and Synchronous Output
  - Schmitt Trigger on All inputs
- Eleven Peripheral DMA Controller (PDC) Channels
- One USB 2.0 Full Speed (12 Mbits per second) Device Port
  - On-chip Transceiver, Eight Endpoints, 2688-byte Configurable Integrated FIFOs
- One Synchronous Serial Controller (SSC)
  - Independent Clock and Frame Sync Signals for Each Receiver and Transmitter
  - I^2S Analog Interface Support, Time Division Multiplex Support
  - High-speed Continuous Data Stream Capabilities with 32-bit Data Transfer
- Two Universal Synchronous/Asynchronous Receiver Transmitters (USART)
  - Individual Baud Rate Generator, IrDA® Infrared Modulation/Demodulation
  - Support for ISO7816 T0/T1 Smart Card, Hardware Handshaking, RS485 Support
  - Full Modem Line Support on USART1
- One Master/Slave Serial Peripheral Interfaces (SPI)
  - 8- to 16-bit Programmable Data Length, Four External Peripheral Chip Selects
- One Three-channel 16-bit Timer/Counter (TC)
  - Three External Clock Inputs, Two Multi-purpose I/O Pins per Channel
  - Double PWM Generation, Capture/Waveform Mode, Up/Down Capability
- One Four-channel 16-bit PWM Controller (PWMC)
- One Two-wire Interface (TWI)
  - Master, Multi-Master and Slave Mode Support, All Two-wire Atmel EEPROMs Supported
  - General Call Supported in Slave Mode
- One 8-channel 10-bit Analog-to-Digital Converter, Four Channels Multiplexed with Digital I/Os
- SAM-BA®
  - Default Boot program
  - Interface with SAM-BA Graphic User Interface
- IEEE® 1149.1 JTAG Boundary Scan on All Digital Pins
- Four High-current Drive I/O lines, Up to 16 mA Each
- Power Supplies
  - Embedded 1.8V Regulator, Drawing up to 100 mA for the Core and External Components
  - 1.8V or 3,3V VDDIO I/O Lines Power Supply, Independent 3.3V VDDFLASH Flash Power Supply
  - 1.8V VDDCORE Core Power Supply with Brownout Detector
- Fully Static Operation:
  - Up to 55 MHz at 1.8V and 85° C Worst Case Conditions
  - Up to 48 MHz at 1.65V and 85° C Worst Case Conditions
- Available in a 128-lead LQFP Green Package, or a 144-ball LFBGA RoHS-compliant Package

2. Block Diagram

Figure 2-1. SAM7SE512/256/32 Block Diagram Signal Description



3. Signal Description

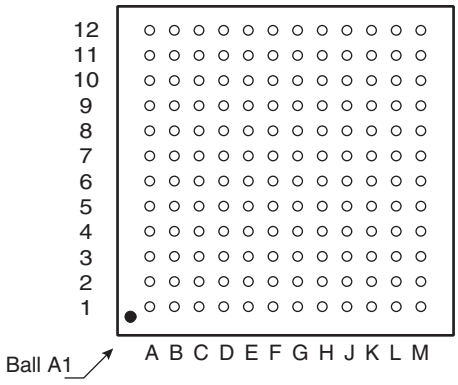
Table 3-1. Signal Description List

Signal Name	Function	Type	Active Level	Comments
Power				
VDDIN	Voltage Regulator and ADC Power Supply Input	Power		3V to 3.6V
VDDOUT	Voltage Regulator Output	Power		1.85V
VDDFLASH	Flash and USB Power Supply	Power		3V to 3.6V
VDDIO	I/O Lines Power Supply	Power		3V to 3.6V or 1.65V to 1.95V
VDDCORE	Core Power Supply	Power		1.65V to 1.95V
VDDPLL	PLL	Power		1.65V to 1.95V
GND	Ground	Ground		
Clocks, Oscillators and PLLs				
XIN	Main Oscillator Input	Input		
XOUT	Main Oscillator Output	Output		
PLLRC	PLL Filter	Input		
PCK0 - PCK2	Programmable Clock Output	Output		
ICE and JTAG				
TCK	Test Clock	Input		No pull-up resistor
TDI	Test Data In	Input		No pull-up resistor
TDO	Test Data Out	Output		
TMS	Test Mode Select	Input		No pull-up resistor.
JTAGSEL	JTAG Selection	Input		Pull-down resistor(1)
Flash Memory				
ERASE	Flash and NVM Configuration Bits Erase Command	Input	High	Pull-down resistor (1)
Reset/Test				
NRST	Microcontroller Reset	I/O	Low	Open drain with pull-up resistor (1)
TST	Test Mode Select	Input	High	Pull-down resistor (1)
Debug Unit				
DRXD	Debug Receive Data	Input		
DTXD	Debug Transmit Data	Output		
AIC				
IRQ0 - IRQ1	External Interrupt Inputs	Input		
FIQ	Fast Interrupt Input	Input		

4.3 144-ball LFBGA Package Outline

Figure 4-2 shows the orientation of the 144-ball LFBGA package and a detailed mechanical description is given in the Mechanical Characteristics section.

Figure 4-2. 144-ball LFBGA Package Outline (Top View)



5. Power Considerations

5.1 Power Supplies

The SAM7SE512/256/32 has six types of power supply pins and integrates a voltage regulator, allowing the device to be supplied with only one voltage. The six power supply pin types are:

- VDDIN pin. It powers the voltage regulator and the ADC; voltage ranges from 3.0V to 3.6V, 3.3V nominal.
- VDDOUT pin. It is the output of the 1.8V voltage regulator.
- VDDIO pin. It powers the I/O lines; two voltage ranges are supported:
  - from 3.0V to 3.6V, 3.3V nominal
  - or from 1.65V to 1.95V, 1.8V nominal.
- VDDFLASH pin. It powers the USB transceivers and a part of the Flash. It is required for the Flash to operate correctly; voltage ranges from 3.0V to 3.6V, 3.3V nominal.
- VDDCORE pins. They power the logic of the device; voltage ranges from 1.65V to 1.95V, 1.8V typical. It can be connected to the VDDOUT pin with decoupling capacitor. VDDCORE is required for the device, including its embedded Flash, to operate correctly.
- VDDPLL pin. It powers the oscillator and the PLL. It can be connected directly to the VDDOUT pin.

In order to decrease current consumption, if the voltage regulator and the ADC are not used, VDDIN, ADVREF, AD4, AD5, AD6 and AD7 should be connected to GND. In this case VDDOUT should be left unconnected.

No separate ground pins are provided for the different power supplies. Only GND pins are provided and should be connected as shortly as possible to the system ground plane.

5.2 Power Consumption

The SAM7SE512/256/32 has a static current of less than 60 µA on VDDCORE at 25°C, including the RC oscillator, the voltage regulator and the power-on reset when the brownout detector is deactivated. Activating the brownout detector adds 20 µA static current.

The dynamic power consumption on VDDCORE is less than 80 mA at full speed when running out of the Flash. Under the same conditions, the power consumption on VDDFLASH does not exceed 10 mA.

5.3 Voltage Regulator

The SAM7SE512/256/32 embeds a voltage regulator that is managed by the System Controller.

In Normal Mode, the voltage regulator consumes less than 100 µA static current and draws 100 mA of output current.

The voltage regulator also has a Low-power Mode. In this mode, it consumes less than 20 µA static current and draws 1 mA of output current.

Adequate output supply decoupling is mandatory for VDDOUT to reduce ripple and avoid oscillations. The best way to achieve this is to use two capacitors in parallel:

- One external 470 pF (or 1 nF) NPO capacitor should be connected between VDDOUT and GND as close to the chip as possible.

- Multiple device adaptability
  - Compliant with LCD Module
  - Compliant with PSRAM in synchronous operations
  - Programmable Setup Time Read/Write
  - Programmable Hold Time Read/Write
- Multiple Wait State Management
  - Programmable Wait State Generation
  - External Wait Request
  - Programmable Data Float Time

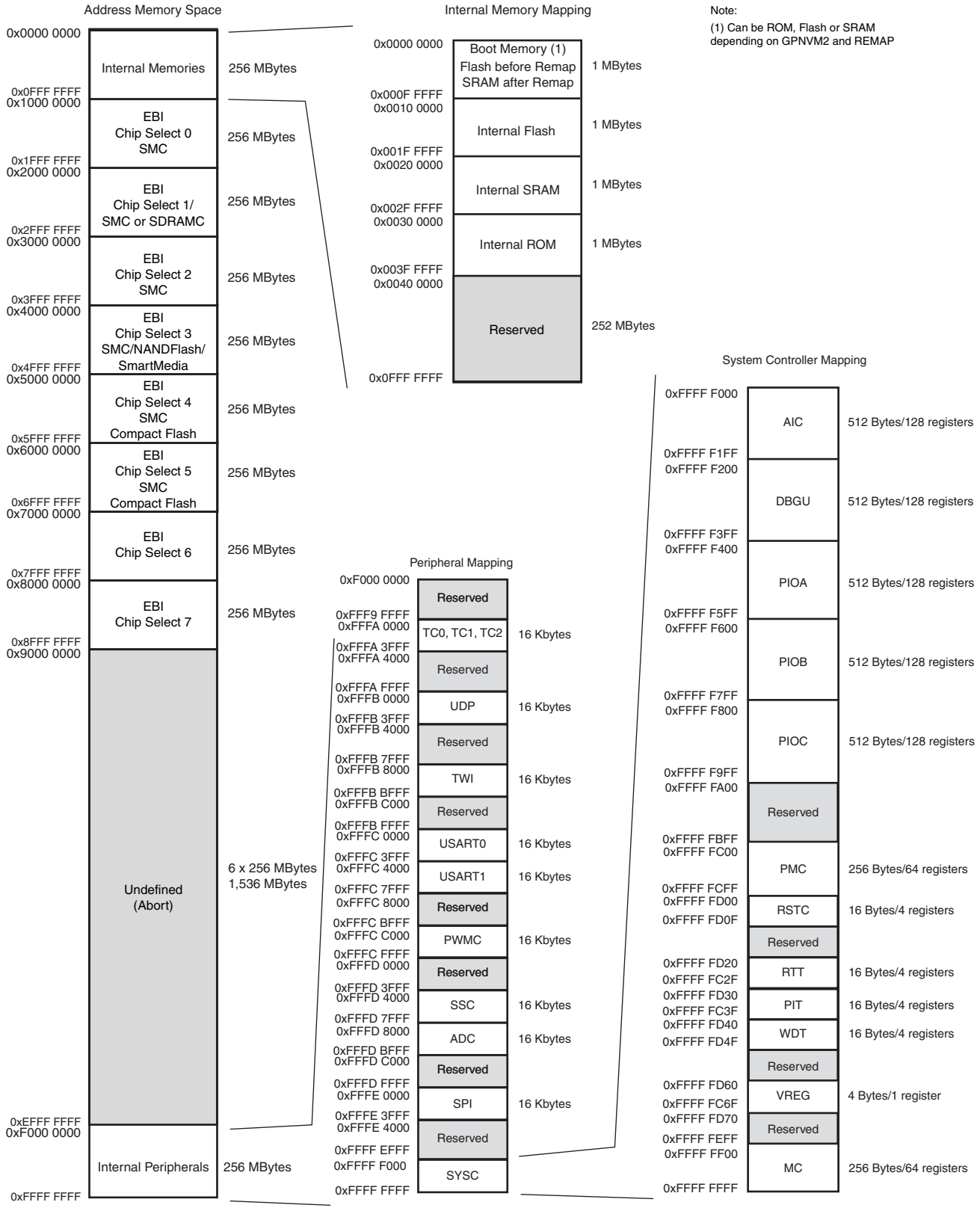
7.6 SDRAM Controller

- Numerous configurations supported
  - **2K, 4K, 8K Row Address Memory Parts**
  - **SDRAM with two or four Internal Banks**
  - **SDRAM with 16- or 32-bit Data Path**
- Programming facilities
  - **Word, half-word, byte access**
  - **Automatic page break when Memory Boundary has been reached**
  - **Multibank Ping-pong Access**
  - **Timing parameters specified by software**
  - **Automatic refresh operation, refresh rate is programmable**
- **Energy-saving capabilities**
  - **Self-refresh, and Low-power Modes supported**
- Error detection
  - **Refresh Error Interrupt**
- **SDRAM Power-up Initialization by software**
- **Latency is set to two clocks (CAS Latency of 1, 3 Not Supported)**
- **Auto Precharge Command not used**
- Mobile SDRAM supported (except for low-power extended mode and deep power-down mode)

7.7 Error Corrected Code Controller

- Tracking the accesses to a NAND Flash device by triggering on the corresponding chip select
- Single bit error correction and 2-bit Random detection.
- Automatic Hamming Code Calculation while writing
  - ECC value available in a register
- Automatic Hamming Code Calculation while reading
  - Error Report, including error flag, correctable error flag and word address being detected erroneous
  - Supports 8- or 16-bit NAND Flash devices with 512-, 1024-, 2048- or 4096-byte pages

Figure 8-1. SAM7SE Memory Mapping



The security bit can only be enabled through the Command “Set Security Bit” of the EFC User Interface. Disabling the security bit can only be achieved by asserting the ERASE pin at 1 and after a full flash erase is performed. When the security bit is deactivated, all accesses to the flash are permitted.

It is important to note that the assertion of the ERASE pin should always be longer than 200 ms.

As the ERASE pin integrates a permanent pull-down, it can be left unconnected during normal operation. However, it is safer to connect it directly to GND for the final application.

8.1.2.5 Non-volatile Brownout Detector Control

Two general purpose NVM (GPNVM) bits are used for controlling the brownout detector (BOD), so that even after a power loss, the brownout detector operations remain in their state.

These two GPNVM bits can be cleared or set respectively through the commands “Clear General-purpose NVM Bit” and “Set General-purpose NVM Bit” of the EFC User Interface.

- GPNVM bit 0 is used as a brownout detector enable bit. Setting the GPNVM bit 0 enables the BOD, clearing it disables the BOD. Asserting ERASE clears the GPNVM bit 0 and thus disables the brownout detector by default.
- GPNVM bit 1 is used as a brownout reset enable signal for the reset controller. Setting the GPNVM bit 1 enables the brownout reset when a brownout is detected, Clearing the GPNVM bit 1 disables the brownout reset. Asserting ERASE disables the brownout reset by default.

8.1.2.6 Calibration Bits

Sixteen NVM bits are used to calibrate the brownout detector and the voltage regulator. These bits are factory configured and cannot be changed by the user. The ERASE pin has no effect on the calibration bits.

8.1.3 Fast Flash Programming Interface

The Fast Flash Programming Interface allows programming the device through either a serial JTAG interface or through a multiplexed fully-handshaked parallel port. It allows gang-programming with market-standard industrial programmers.

The FFPI supports read, page program, page erase, full erase, lock, unlock and protect commands.

The Fast Flash Programming Interface is enabled and the Fast Programming Mode is entered when the TST pin and the PA0 and PA1 pins are all tied high and PA2 tied to low.

- The Flash of the SAM7SE512 is organized in 2048 pages of 256 bytes (dual plane). It reads as 131,072 32-bit words.
- The Flash of the SAM7SE256 is organized in 1024 pages of 256 bytes (single plane). It reads as 65,536 32-bit words.
- The Flash of the SAM7SE32 is organized in 256 pages of 128 bytes (single plane). It reads as 32,768 32-bit words.
- The Flash of the SAM7SE512/256 contains a 256-byte write buffer, accessible through a 32-bit interface.
- The Flash of the SAM7SE32 contains a 128-byte write buffer, accessible through a 32-bit interface.

9. System Controller

The System Controller manages all vital blocks of the microcontroller: interrupts, clocks, power, time, debug and reset.

The System Controller peripherals are all mapped to the highest 4 Kbytes of address space, between addresses 0xFFFF F000 and 0xFFFF FFFF.

Figure 9-1 on page 29 shows the System Controller Block Diagram.

Figure 8-1 on page 22 shows the mapping of the User Interface of the System Controller peripherals. Note that the Memory Controller configuration user interface is also mapped within this address space.

9.1 Reset Controller

- Based on one power-on reset cell and a double brownout detector
- Status of the last reset, either Power-up Reset, Software Reset, User Reset, Watchdog Reset, Brownout Reset
- Controls the internal resets and the NRST pin output
- Allows to shape a signal on the NRST line, guaranteeing that the length of the pulse meets any requirement.

9.1.1 Brownout Detector and Power On Reset

The SAM7SE512/256/32 embeds one brownout detection circuit and a power-on reset cell. The power-on reset is supplied with and monitors VDDCORE.

Both signals are provided to the Flash to prevent any code corruption during power-up or power-down sequences or if brownouts occur on the VDDCORE power supply.

The power-on reset cell has a limited-accuracy threshold at around 1.5V. Its output remains low during power-up until VDDCORE goes over this voltage level. This signal goes to the reset controller and allows a full re-initialization of the device.

The brownout detector monitors the VDDCORE and VDDFLASH levels during operation by comparing it to a fixed trigger level. It secures system operations in the most difficult environments and prevents code corruption in case of brownout on the VDDCORE or VDDFLASH.

When the brownout detector is enabled and VDDCORE decreases to a value below the trigger level (Vbot18-, defined as Vbot18 - hyst/2), the brownout output is immediately activated.

When VDDCORE increases above the trigger level (Vbot18+, defined as Vbot18 + hyst/2), the reset is released. The brownout detector only detects a drop if the voltage on VDDCORE stays below the threshold voltage for longer than about 1µs.

The VDDCORE threshold voltage has a hysteresis of about 50 mV, to ensure spike free brownout detection. The typical value of the brownout detector threshold is 1.68V with an accuracy of ± 2% and is factory calibrated.

When the brownout detector is enabled and VDDFLASH decreases to a value below the trigger level (Vbot33-, defined as Vbot33 - hyst/2), the brownout output is immediately activated.

When VDDFLASH increases above the trigger level (Vbot33+, defined as Vbot33 + hyst/2), the reset is released. The brownout detector only detects a drop if the voltage on VDDCORE stays below the threshold voltage for longer than about 1µs.

The VDDFLASH threshold voltage has a hysteresis of about 50 mV, to ensure spike free brownout detection. The typical value of the brownout detector threshold is 2.80V with an accuracy of ± 3.5% and is factory calibrated.

The brownout detector is low-power, as it consumes less than 20 µA static current. However, it can be deactivated to save its static current. In this case, it consumes less than 1µA. The deactivation is configured through the GPNVM bit 0 of the Flash.

9.2 Clock Generator

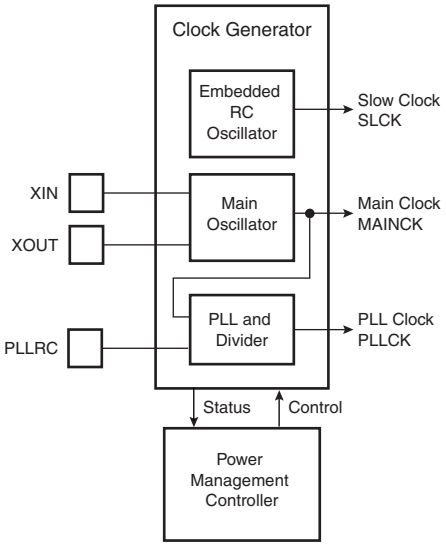
The Clock Generator embeds one low-power RC Oscillator, one Main Oscillator and one PLL with the following characteristics:

- RC Oscillator ranges between 22 KHz and 42 KHz

- Main Oscillator frequency ranges between 3 and 20 MHz
- Main Oscillator can be bypassed
- PLL output ranges between 80 and 220 MHz

It provides SLCK, MAINCK and PLLCK.

Figure 9-2. Clock Generator Block Diagram



9.3 Power Management Controller

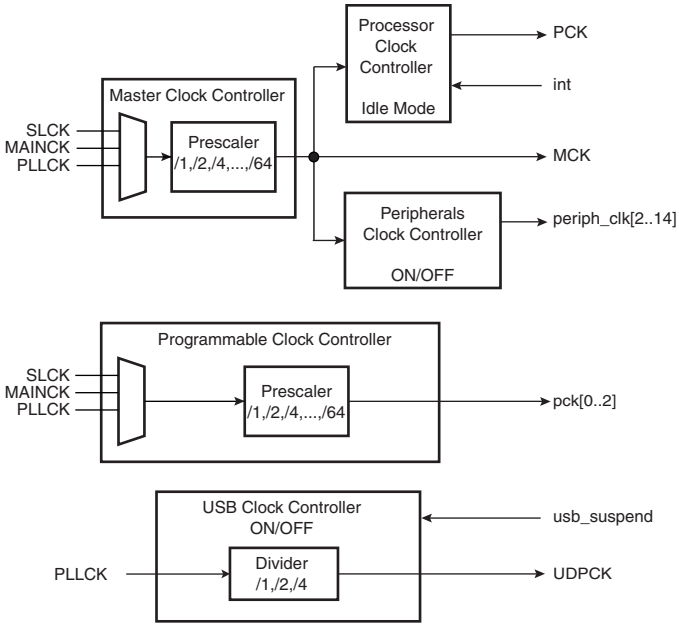
The Power Management Controller uses the Clock Generator outputs to provide:

- the Processor Clock PCK
- the Master Clock MCK
- the USB Clock UDPCK
- all the peripheral clocks, independently controllable
- three programmable clock outputs

The Master Clock (MCK) is programmable from a few hundred Hz to the maximum operating frequency of the device.

The Processor Clock (PCK) switches off when entering processor idle mode, thus allowing reduced power consumption while waiting for an interrupt.

Figure 9-3. Power Management Controller Block Diagram



9.4 Advanced Interrupt Controller

- Controls the interrupt lines (nIRQ and nFIQ) of an ARM Processor
- Individually maskable and vectored interrupt sources
  - Source 0 is reserved for the Fast Interrupt Input (FIQ)
  - Source 1 is reserved for system peripherals (RTT, PIT, EFC, PMC, DBGU, etc.)
  - Other sources control the peripheral interrupts or external interrupts
  - Programmable edge-triggered or level-sensitive internal sources
  - Programmable positive/negative edge-triggered or high/low level-sensitive external sources
- 8-level Priority Controller
  - Drives the normal interrupt nIRQ of the processor
  - Handles priority of the interrupt sources
  - Higher priority interrupts can be served during service of lower priority interrupt
- Vectoring
  - Optimizes interrupt service routine branch and execution
  - One 32-bit vector register per interrupt source
  - Interrupt vector register reads the corresponding current interrupt vector
- Protect Mode
  - Easy debugging by preventing automatic operations
- Fast Forcing
  - Permits redirecting any interrupt source on the fast interrupt
- General Interrupt Mask
  - Provides processor synchronization on events without triggering an interrupt

9.5 Debug Unit

- Comprises:
  - One two-pin UART
  - One Interface for the Debug Communication Channel (DCC) support
  - One set of Chip ID Registers
  - One Interface providing ICE Access Prevention
- Two-pin UART
  - USART-compatible User Interface
  - Programmable Baud Rate Generator
  - Parity, Framing and Overrun Error
  - Automatic Echo, Local Loopback and Remote Loopback Channel Modes
- Debug Communication Channel Support
  - Offers visibility of COMMRX and COMMTX signals from the ARM Processor
- Chip ID Registers
  - Identification of the device revision, sizes of the embedded memories, set of peripherals
  - Chip ID is 0x272A 0A40 (VERSION 0) for SAM7SE512
  - Chip ID is 0x272A 0940 (VERSION 0) for SAM7SE256
  - Chip ID is 0x2728 0340 (VERSION 0) for SAM7SE32

9.6 Periodic Interval Timer

- 20-bit programmable counter plus 12-bit interval counter

9.7 Watchdog Timer

- 12-bit key-protected Programmable Counter running on prescaled SLCK
- Provides reset or interrupt signals to the system
- Counter may be stopped while the processor is in debug state or in idle mode

9.8 Real-time Timer

- 32-bit free-running counter with alarm running on prescaled SLCK
- Programmable 16-bit prescaler for SLCK accuracy compensation

9.9 PIO Controllers

- Three PIO Controllers. PIO A and B each control 32 I/O lines and PIO C controls 24 I/O lines.
- Fully programmable through set/clear registers
- Multiplexing of two peripheral functions per I/O line
- For each I/O line (whether assigned to a peripheral or used as general-purpose I/O)
  - Input change interrupt
  - Half a clock period glitch filter
  - Multi-drive option enables driving in open drain
  - Programmable pull-up on each I/O line
  - Pin data status register, supplies visibility of the level on the pin at any time

- Synchronous output, provides Set and Clear of several I/O lines in a single write

9.10 Voltage Regulator Controller

The purpose of this controller is to select the Power Mode of the Voltage Regulator between Normal Mode (bit 0 is cleared) or Standby Mode (bit 0 is set).

10.4 PIO Controller A Multiplexing

Table 10-2. Multiplexing on PIO Controller A

PIO Controller A				Application Usage	
I/O Line	**Peripheral A**	**Peripheral B**	**Comments**	**Function**	**Comments**
PA0	PWM0	A0/NBS0	High-Drive		
PA1	PWM1	A1/NBS2	High-Drive		
PA2	PWM2	A2	High-Drive		
PA3	TWD	A3	High-Drive		
PA4	TWCK	A4			
PA5	RXD0	A5			
PA6	TXD0	A6			
PA7	RTS0	A7			
PA8	CTS0	A8			
PA9	DRXD	A9			
PA10	DTXD	A10			
PA11	NPCS0	A11			
PA12	MISO	A12			
PA13	MOSI	A13			
PA14	SPCK	A14			
PA15	TF	A15			
PA16	TK	A16/BA0			
PA17	TD	A17/BA1	AD0		
PA18	RD	NBS3/CFIOW	AD1		
PA19	RK	NCS4/CFCS0	AD2		
PA20	RF	NCS2/CFCS1	AD3		
PA21	RXD1	NCS6/CFCE2			
PA22	TXD1	NCS5/CFCE1			
PA23	SCK1	NWR1/NBS1/CFIOR			
PA24	RTS1	SDA10			
PA25	CTS1	SDCKE			
PA26	DCD1	NCS1/SDCS			
PA27	DTR1	SDWE			
PA28	DSR1	CAS			
PA29	RI1	RAS			
PA30	IRQ1	D30			
PA31	NPCS1	D31			

10.5 PIO Controller B Multiplexing

Table 10-3. Multiplexing on PIO Controller B

PIO Controller B				Application Usage	
I/O Line	**Peripheral A**	**Peripheral B**	**Comments**	**Function**	**Comments**
PB0	TIOA0	A0/NBS0			
PB1	TIOB0	A1/NBS2			
PB2	SCK0	A2			
PB3	NPCS3	A3			
PB4	TCLK0	A4			
PB5	NPCS3	A5			
PB6	PCK0	A6			
PB7	PWM3	A7			
PB8	ADTRG	A8			
PB9	NPCS1	A9			
PB10	NPCS2	A10			
PB11	PWM0	A11			
PB12	PWM1	A12			
PB13	PWM2	A13			
PB14	PWM3	A14			
PB15	TIOA1	A15			
PB16	TIOB1	A16/BA0			
PB17	PCK1	A17/BA1			
PB18	PCK2	D16			
PB19	FIQ	D17			
PB20	IRQ0	D18			
PB21	PCK1	D19			
PB22	NPCS3	D20			
PB23	PWM0	D21			
PB24	PWM1	D22			
PB25	PWM2	D23			
PB26	TIOA2	D24			
PB27	TIOB2	D25			
PB28	TCLK1	D26			
PB29	TCLK2	D27			
PB30	NPCS2	D28			
PB31	PCK2	D29			

10.6 PIO Controller C Multiplexing

Multiplexing on PIO Controller C

PIO Controller C				Application Usage	
I/O Line	Peripheral A	Peripheral B	Comments	Function	Comments
PC0	D0				
PC1	D1				
PC2	D2				
PC3	D3				
PC4	D4				
PC5	D5				
PC6	D6				
PC7	D7				
PC8	D8	RTS1			
PC9	D9	DTR1			
PC10	D10	PCK0			
PC11	D11	PCK1			
PC12	D12	PCK2			
PC13	D13				
PC14	D14	NPCS1			
PC15	D15	NCS3/NANDCS			
PC16	A18	NWAIT			
PC17	A19	NANDOE			
PC18	A20	NANDWE			
PC19	A21/NANDALE				
PC20	A22/REG/NANDCLE	NCS7			
PC21		NWR0/NWE/CFWE			
PC22		NRD/CFOE			
PC23	CFRNW	NCS0			

10.7 Serial Peripheral Interface

- Supports communication with external serial devices
  - Four chip selects with external decoder allow communication with up to 15 peripherals
  - Serial memories, such as DataFlash® and 3-wire EEPROMs
  - Serial peripherals, such as ADCs, DACs, LCD Controllers, CAN Controllers and Sensors
  - External co-processors
- Master or slave serial peripheral bus interface

- Offers a configurable frame sync and data length
- Receiver and transmitter can be programmed to start automatically or on detection of different event on the frame sync signal
- Receiver and transmitter include a data signal, a clock signal and a frame synchronization signal

10.11 Timer Counter

- Three 16-bit Timer Counter Channels
  - Two output compare or one input capture per channel
- Wide range of functions including:
  - Frequency measurement
  - Event counting
  - Interval measurement
  - Pulse generation
  - Delay timing
  - Pulse Width Modulation
  - Up/down capabilities
- Each channel is user-configurable and contains:
  - Three external clock inputs
  - Five internal clock inputs, as defined in Table 10-4

Table 10-4. Timer Counter Clocks Assignment

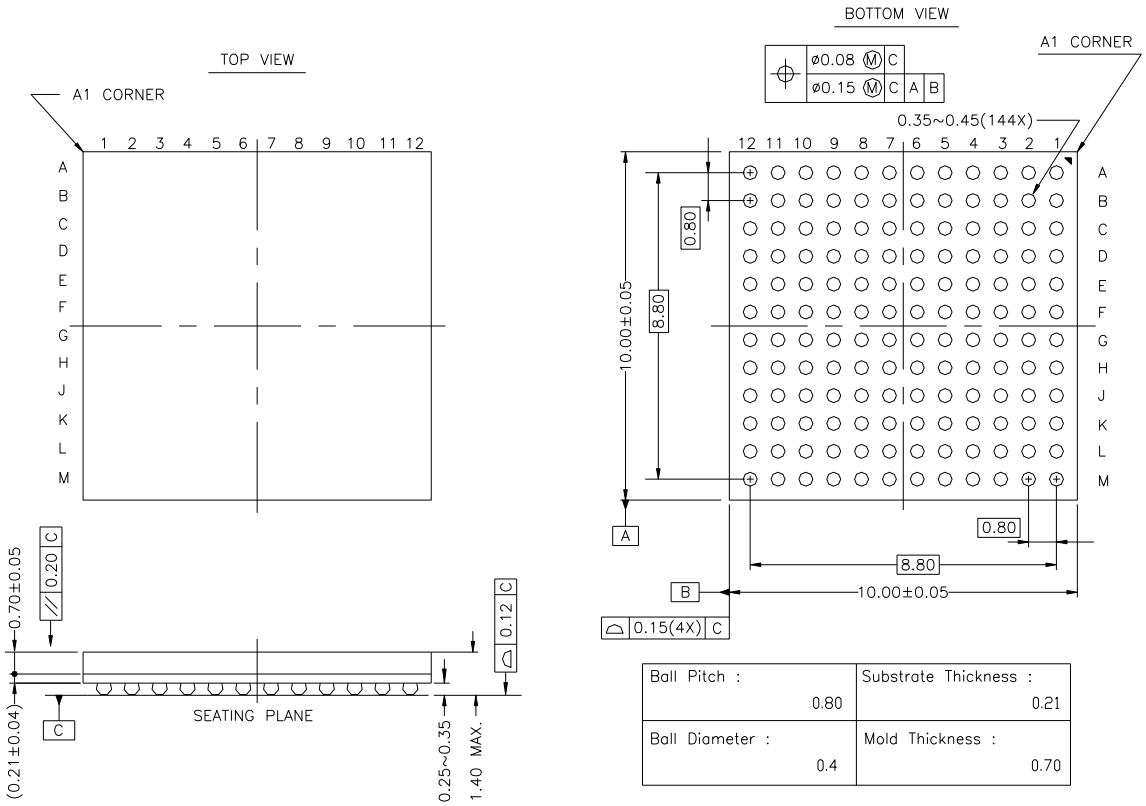
TC Clock input	Clock
TIMER_CLOCK1	MCK/2
TIMER_CLOCK2	MCK/8
TIMER_CLOCK3	MCK/32
TIMER_CLOCK4	MCK/128
TIMER_CLOCK5	MCK/1024

  - Two multi-purpose input/output signals
  - Two global registers that act on all three TC channels

10.12 PWM Controller

- Four channels, one 16-bit counter per channel
- Common clock generator, providing thirteen different clocks
  - One Modulo n counter providing eleven clocks
  - Two independent linear dividers working on modulo n counter outputs
- Independent channel programming
  - Independent enable/disable commands
  - Independent clock selection
  - Independent period and duty cycle, with double buffering
  - Programmable selection of the output waveform polarity
  - Programmable center or left aligned output waveform

Figure 11-2. 144-ball LFBGA Package Drawing



All dimensions are in mm

12. Ordering Information

Table 12-1. Ordering Information

Ordering Code	MRL	Package	Package Type	Temperature Operating Range
AT91SAM7SE512B-AU	B	LQFP128	Green	Industrial (-40· C to 85· C)
AT91SAM7SE256B-AU	B	LQFP128	Green	Industrial (-40· C to 85· C)
AT91SAM7SE32B-AU	B	LQFP128	Green	Industrial (-40· C to 85· C)
AT91SAM7SE512B-CU	B	LFBGA144	Green	Industrial (-40· C to 85· C)
AT91SAM7SE256B-CU	B	LFBGA144	Green	Industrial (-40· C to 85· C)
AT91SAM7SE32B-CU	B	LFBGA144	Green	Industrial (-40· C to 85· C)
AT91SAM7SE512-AU	A	LQFP128	Green	Industrial (-40· C to 85· C)
AT91SAM7SE256-AU	A	LQFP128	Green	Industrial (-40· C to 85· C)
AT91SAM7SE32-AU	A	LQFP128	Green	Industrial (-40· C to 85· C)
AT91SAM7SE512-CU	A	LFBGA144	Green	Industrial (-40· C to 85· C)
AT91SAM7SE256-CU	A	LFBGA144	Green	Industrial (-40· C to 85· C)
AT91SAM7SE32-CU	A	LFBGA144	Green	Industrial (-40· C to 85· C)