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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM7® |
| Core Size | 16/32-Bit |
| Speed | 55MHz |
| Connectivity | EBI/EMI, I²C, SPI, SSC, UART/USART, USB |
| Peripherals | Brown-out Detect/Reset, POR, PWM, WDT |
| Number of I/O | 88 |
| Program Memory Size | 32KB (32K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 8K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.65V ~ 1.95V |
| Data Converters | A/D 8x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 128-LQFP |
| Supplier Device Package | 128-LQFP (20x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/at91sam7se32b-au |

# 2. Block Diagram

**Figure 2-1.** SAM7SE512/256/32 Block Diagram Signal Description

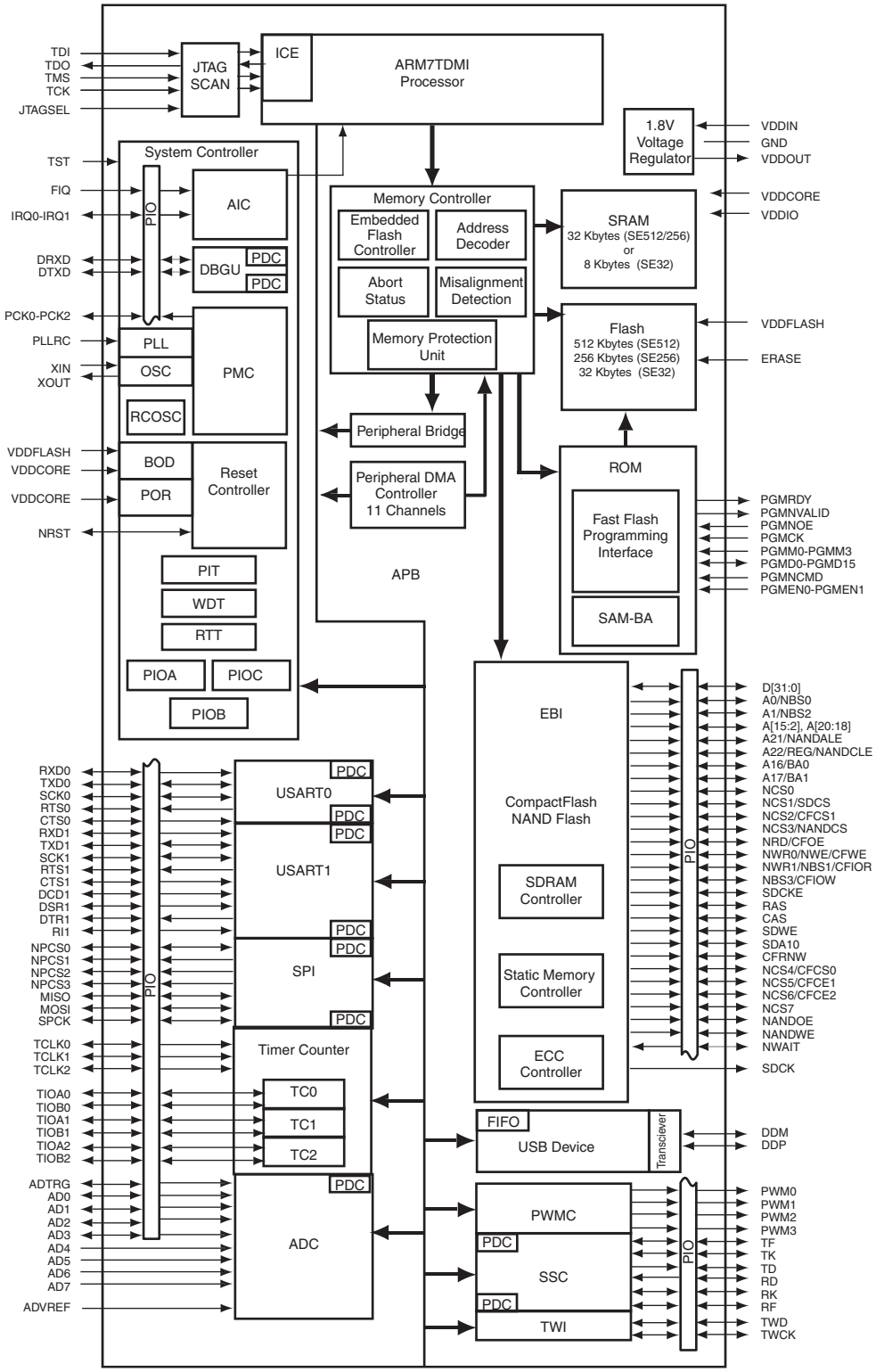


**Table 3-1.** Signal Description List (Continued)

| Signal Name | Function | Type | Active Level | Comments |
|---|---|---|---|---|
| **Two-Wire Interface** | | | | |
| TWD | Two-wire Serial Data | I/O | | |
| TWCK | Two-wire Serial Clock | I/O | | |
| **Analog-to-Digital Converter** | | | | |
| AD0-AD3 | Analog Inputs | Analog | | Digital pulled-up inputs at reset |
| AD4-AD7 | Analog Inputs | Analog | | Analog Inputs |
| ADTRG | ADC Trigger | Input | | |
| ADVREF | ADC Reference | Analog | | |
| **Fast Flash Programming Interface** | | | | |
| PGMEN0-PGMEN2 | Programming Enabling | Input | | |
| PGMM0-PGMM3 | Programming Mode | Input | | |
| PGMD0-PGMD15 | Programming Data | I/O | | |
| PGMRDY | Programming Ready | Output | High | |
| PGMNVALID | Data Direction | Output | Low | |
| PGMNOE | Programming Read | Input | Low | |
| PGMCK | Programming Clock | Input | | |
| PGMNCMD | Programming Command | Input | Low | |
| **External Bus Interface** | | | | |
| D[31:0] | Data Bus | I/O | | |
| A[22:0] | Address Bus | Output | | |
| NWAIT | External Wait Signal | Input | Low | |
| **Static Memory Controller** | | | | |
| NCS[7:0] | Chip Select Lines | Output | Low | |
| NWR[1:0] | Write Signals | Output | Low | |
| NRD | Read Signal | Output | Low | |
| NWE | Write Enable | Output | Low | |
| NUB | NUB: Upper Byte Select | Output | Low | |
| NLB | NLB: Lower Byte Select | Output | Low | |
| **EBI for CompactFlash Support** | | | | |
| CFCE[2:1] | CompactFlash Chip Enable | Output | Low | |
| CFOE | CompactFlash Output Enable | Output | Low | |
| CFWE | CompactFlash Write Enable | Output | Low | |
| CFIOR | CompactFlash I/O Read Signal | Output | Low | |
| CFIOW | CompactFlash I/O Write Signal | Output | Low | |
| CFRNW | CompactFlash Read Not Write Signal | Output | | |
| CFCS[1:0] | CompactFlash Chip Select Lines | Output | Low | |

## 4.2 128-lead LQFP Pinout

**Table 4-1.** Pinout in 128-lead LQFP Package

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 1 | ADVREF | 33 | PB31 | 65 | TDI | 97 | SDCK |
| 2 | GND | 34 | PB30 | 66 | TDO | 98 | PC8 |
| 3 | AD7 | 35 | PB29 | 67 | PB2 | 99 | PC7 |
| 4 | AD6 | 36 | PB28 | 68 | PB1 | 100 | PC6 |
| 5 | AD5 | 37 | PB27 | 69 | PB0 | 101 | PC5 |
| 6 | AD4 | 38 | PB26 | 70 | GND | 102 | PC4 |
| 7 | VDDOUT | 39 | PB25 | 71 | VDDIO | 103 | PC3 |
| 8 | VDDIN | 40 | PB24 | 72 | VDDCORE | 104 | PC2 |
| 9 | PA20/PGMD8/AD3 | 41 | PB23 | 73 | NRST | 105 | PC1 |
| 10 | PA19/PGMD7/AD2 | 42 | PB22 | 74 | TST | 106 | PC0 |
| 11 | PA18/PGMD6/AD1 | 43 | PB21 | 75 | ERASE | 107 | PA31 |
| 12 | PA17/PGMD5/AD0 | 44 | PB20 | 76 | TCK | 108 | PA30 |
| 13 | PA16/PGMD4 | 45 | GND | 77 | TMS | 109 | PA29 |
| 14 | PA15/PGMD3 | 46 | VDDIO | 78 | JTAGSEL | 110 | PA28 |
| 15 | PA14/PGMD2 | 47 | VDDCORE | 79 | PC23 | 111 | PA27/PGMD15 |
| 16 | PA13/PGMD1 | 48 | PB19 | 80 | PC22 | 112 | PA26/PGMD14 |
| 17 | PA12/PGMD0 | 49 | PB18 | 81 | PC21 | 113 | PA25/PGMD13 |
| 18 | PA11/PGMM3 | 50 | PB17 | 82 | PC20 | 114 | PA24/PGMD12 |
| 19 | PA10/PGMM2 | 51 | PB16 | 83 | PC19 | 115 | PA23/PGMD11 |
| 20 | PA9/PGMM1 | 52 | PB15 | 84 | PC18 | 116 | PA22/PGMD10 |
| 21 | VDDIO | 53 | PB14 | 85 | PC17 | 117 | PA21/PGMD9 |
| 22 | GND | 54 | PB13 | 86 | PC16 | 118 | VDDCORE |
| 23 | VDDCORE | 55 | PB12 | 87 | PC15 | 119 | GND |
| 24 | PA8/PGMM0 | 56 | PB11 | 88 | PC14 | 120 | VDDIO |
| 25 | PA7/PGMNVALID | 57 | PB10 | 89 | PC13 | 121 | DM |
| 26 | PA6/PGMNOE | 58 | PB9 | 90 | PC12 | 122 | DP |
| 27 | PA5/PGMRDY | 59 | PB8 | 91 | PC11 | 123 | VDDFLASH |
| 28 | PA4/PGMNCMD | 60 | PB7 | 92 | PC10 | 124 | GND |
| 29 | PA3 | 61 | PB6 | 93 | PC9 | 125 | XIN/PGMCK |
| 30 | PA2/PGMEN2 | 62 | PB5 | 94 | GND | 126 | XOUT |
| 31 | PA1/PGMEN1 | 63 | PB4 | 95 | VDDIO | 127 | PLLRC |
| 32 | PA0/PGMEN0 | 64 | PB3 | 96 | VDDCORE | 128 | VDDPLL |

## 4.4 144-ball LFBGA Pinout

**Table 4-2.** SAM7SE512/256/32 Pinout for 144-ball LFBGA Package

| Pin | Signal Name | Pin | Signal Name | Pin | Signal Name | Pin | Signal Name |
|---|---|---|---|---|---|---|---|
| A1 | PB7 | D1 | VDDCORE | G1 | PC18 | K1 | PC11 |
| A2 | PB8 | D2 | VDDCORE | G2 | PC16 | K2 | PC6 |
| A3 | PB9 | D3 | PB2 | G3 | PC17 | K3 | PC2 |
| A4 | PB12 | D4 | TDO | G4 | PC9 | K4 | PC0 |
| A5 | PB13 | D5 | TDI | G5 | VDDIO | K5 | PA27/PGMD15 |
| A6 | PB16 | D6 | PB17 | G6 | GND | K6 | PA26/PGMD14 |
| A7 | PB22 | D7 | PB26 | G7 | GND | K7 | GND |
| A8 | PB23 | D8 | PA14/PGMD2 | G8 | GND | K8 | VDDCORE |
| A9 | PB25 | D9 | PA12/PGMD0 | G9 | GND | K9 | VDDFLASH |
| A10 | PB29 | D10 | PA11/PGMM3 | G10 | AD4 | K10 | VDDIO |
| A11 | PB30 | D11 | PA8/PGMM0 | G11 | VDDIN | K11 | VDDIO |
| A12 | PB31 | D12 | PA7/PGMNVALID | G12 | VDDOUT | K12 | PA18/PGMD6/AD1 |
| B1 | PB6 | E1 | PC22 | H1 | PC15 | L1 | SDCK |
| B2 | PB3 | E2 | PC23 | H2 | PC14 | L2 | PC7 |
| B3 | PB4 | E3 | NRST | H3 | PC13 | L3 | PC4 |
| B4 | PB10 | E4 | TCK | H4 | VDDCORE | L4 | PC1 |
| B5 | PB14 | E5 | ERASE | H5 | VDDCORE | L5 | PA29 |
| B6 | PB18 | E6 | TEST | H6 | GND | L6 | PA24/PGMD12 |
| B7 | PB20 | E7 | VDDCORE | H7 | GND | L7 | PA21/PGMD9 |
| B8 | PB24 | E8 | VDDCORE | H8 | GND | L8 | ADVREF |
| B9 | PB28 | E9 | GND | H9 | GND | L9 | VDDFLASH |
| B10 | PA4/PGMNCMD | E10 | PA9/PGMM1 | H10 | PA19/PGMD7/AD2 | L10 | VDDFLASH |
| B11 | PA0/PGMEN0 | E11 | PA10/PGMM2 | H11 | PA20/PGMD8/AD3 | L11 | PA17/PGMD5/AD0 |
| B12 | PA1/PGMEN1 | E12 | PA13/PGMD1 | H12 | VDDIO | L12 | GND |
| C1 | PB0 | F1 | PC21 | J1 | PC12 | M1 | PC8 |
| C2 | PB1 | F2 | PC20 | J2 | PC10 | M2 | PC5 |
| C3 | PB5 | F3 | PC19 | J3 | PA30 | M3 | PC3 |
| C4 | PB11 | F4 | JTAGSEL | J4 | PA28 | M4 | PA31 |
| C5 | PB15 | F5 | TMS | J5 | PA23/PGMD11 | M5 | PA25/PGMD13 |
| C6 | PB19 | F6 | VDDIO | J6 | PA22/PGMD10 | M6 | DM |
| C7 | PB21 | F7 | GND | J7 | AD6 | M7 | DP |
| C8 | PB27 | F8 | GND | J8 | AD7 | M8 | GND |
| C9 | PA6/PGMNOE | F9 | GND | J9 | VDDCORE | M9 | XIN/PGMCK |
| C10 | PA5/PGMRDY | F10 | AD5 | J10 | VDDCORE | M10 | XOUT |
| C11 | PA2/PGMEN2 | F11 | PA15/PGMD3 | J11 | VDDCORE | M11 | PLLRC |
| C12 | PA3 | F12 | PA16/PGMD4 | J12 | VDDIO | M12 | VDDPLL |

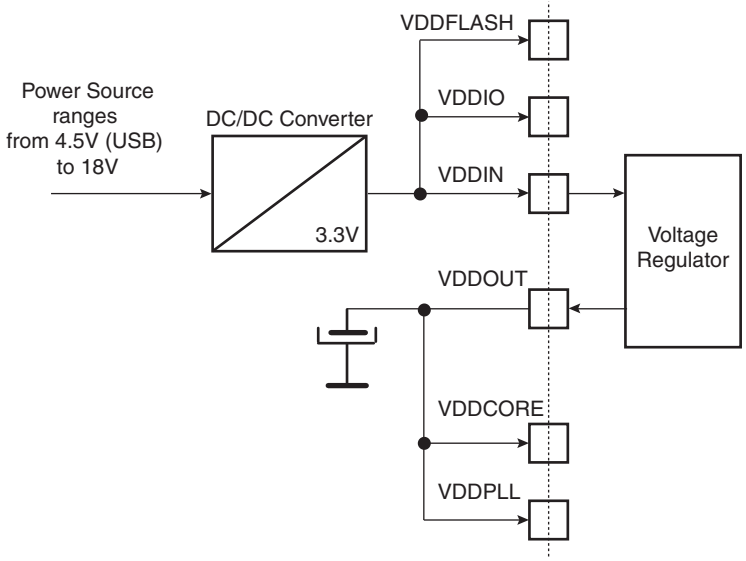
- One external 2.2 µF (or 3.3 µF) X7R capacitor should be connected between VDDOUT and GND.

Adequate input supply decoupling is mandatory for VDDIN in order to improve startup stability and reduce source voltage drop. The input decoupling capacitor should be placed close to the chip. For example, two capacitors can be used in parallel: 100 nF NPO and 4.7 µF X7R.

## 5.4 Typical Powering Schematics

The SAM7SE512/256/32 supports a 3.3V single supply mode. The internal regulator input connected to the 3.3V source and its output feeds VDDCORE and the VDDPLL. Figure 5-1 shows the power schematics to be used for USB bus-powered systems.

**Figure 5-1.** 3.3V System Single Power Supply Schematic



## 6.5 SDCK Pin

The SDCK pin is dedicated to the SDRAM Clock and is an output-only without pull-up. Maximum Output Frequency of this pad is 48 MHz at 3.0V and 25 MHz at 1.65V with a maximum load of 30 pF.

## 6.6 PIO Controller lines

All the I/O lines PA0 to PA31, PB0 to PB31, PC0 to PC23 integrate a programmable pull-up resistor. Programming of this pull-up resistor is performed independently for each I/O line through the PIO controllers.

Typical pull-up value is 100 kΩ

All the I/O lines have schmitt trigger inputs.

## 6.7 I/O Lines Current Drawing

The PIO lines PA0 to PA3 are high-drive current capable. Each of these I/O lines can drive up to 16 mA permanently.

The remaining I/O lines can draw only 8 mA.

However, the total current drawn by all the I/O lines cannot exceed 300 mA.

# 7. Processor and Architecture

## 7.1 ARM7TDMI Processor

- RISC processor based on ARMv4T Von Neumann architecture
  - Runs at up to 55 MHz, providing 0.9 MIPS/MHz (core supplied with 1.8V)
- Two instruction sets
  - ARM® high-performance 32-bit instruction set
  - Thumb® high code density 16-bit instruction set
- Three-stage pipeline architecture
  - Instruction Fetch (F)
  - Instruction Decode (D)
  - Execute (E)

## 7.2 Debug and Test Features

- EmbeddedICE™ (Integrated embedded in-circuit emulator)
  - Two watchpoint units
  - Test access port accessible through a JTAG protocol
  - Debug communication channel
- Debug Unit
  - Two-pin UART
  - Debug communication channel interrupt handling
  - Chip ID Register
- IEEE1149.1 JTAG Boundary-scan on all digital pins

## 7.3 Memory Controller

- Programmable Bus Arbiter
  - Handles requests from the ARM7TDMI and the Peripheral DMA Controller
- Address decoder provides selection signals for
  - Four internal 1 Mbyte memory areas
  - One 256-Mbyte embedded peripheral area
  - Eight external 256-Mbyte memory areas
- Abort Status Registers
  - Source, Type and all parameters of the access leading to an abort are saved
  - Facilitates debug by detection of bad pointers
- Misalignment Detector
  - Alignment checking of all data accesses
  - Abort generation in case of misalignment
- Remap Command
  - Remaps the SRAM in place of the embedded non-volatile memory
  - Allows handling of dynamic exception vectors
- 16-area Memory Protection Unit (Internal Memory and peripheral protection only)

- Multiple device adaptability
  - Compliant with LCD Module
  - Compliant with PSRAM in synchronous operations
  - Programmable Setup Time Read/Write
  - Programmable Hold Time Read/Write
- Multiple Wait State Management
  - Programmable Wait State Generation
  - External Wait Request
  - Programmable Data Float Time

## 7.6 SDRAM Controller

- Numerous configurations supported
  - **2K, 4K, 8K Row Address Memory Parts**
  - **SDRAM with two or four Internal Banks**
  - **SDRAM with 16- or 32-bit Data Path**
- Programming facilities
  - **Word, half-word, byte access**
  - **Automatic page break when Memory Boundary has been reached**
  - **Multibank Ping-pong Access**
  - **Timing parameters specified by software**
  - **Automatic refresh operation, refresh rate is programmable**
- **Energy-saving capabilities**
  - **Self-refresh, and Low-power Modes supported**
- Error detection
  - **Refresh Error Interrupt**
- **SDRAM Power-up Initialization by software**
- **Latency is set to two clocks (CAS Latency of 1, 3 Not Supported)**
- **Auto Precharge Command not used**
- Mobile SDRAM supported (except for low-power extended mode and deep power-down mode)

## 7.7 Error Corrected Code Controller

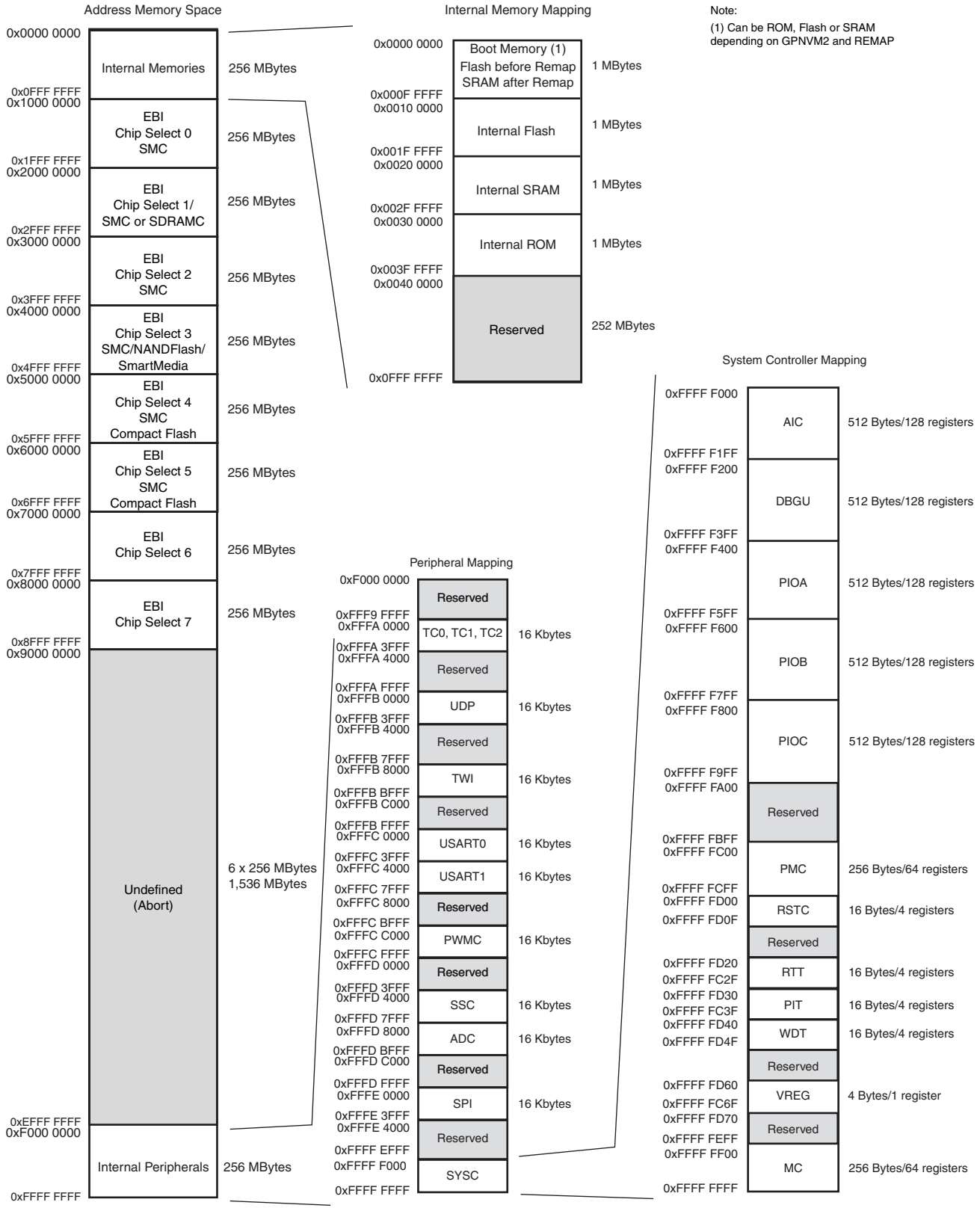
- Tracking the accesses to a NAND Flash device by triggering on the corresponding chip select
- Single bit error correction and 2-bit Random detection.
- Automatic Hamming Code Calculation while writing
  - ECC value available in a register
- Automatic Hamming Code Calculation while reading
  - Error Report, including error flag, correctable error flag and word address being detected erroneous
  - Supports 8- or 16-bit NAND Flash devices with 512-, 1024-, 2048- or 4096-byte pages

## 7.8 Peripheral DMA Controller

- Handles data transfer between peripherals and memories
- Eleven channels
  - Two for each USART
  - Two for the Debug Unit
  - Two for the Serial Synchronous Controller
  - Two for the Serial Peripheral Interface
  - One for the Analog-to-digital Converter
- Low bus arbitration overhead
  - One Master Clock cycle needed for a transfer from memory to peripheral
  - Two Master Clock cycles needed for a transfer from peripheral to memory
- Next Pointer management for reducing interrupt latency requirements
- Peripheral DMA Controller (PDC) priority is as follows (from the highest priority to the lowest):

| | |
|---|---|
| Receive | DBGU |
| Receive | USART0 |
| Receive | USART1 |
| Receive | SSC |
| Receive | ADC |
| Receive | SPI |
| Transmit | DBGU |
| Transmit | USART0 |
| Transmit | USART1 |
| Transmit | SSC |
| Transmit | SPI |

**Figure 8-1.** SAM7SE Memory Mapping



A first level of address decoding is performed by the Memory Controller, i.e., by the implementation of the Advanced System Bus (ASB) with additional features.

Decoding splits the 4G bytes of address space into 16 areas of 256M bytes. The areas 1 to 8 are directed to the EBI that associates these areas to the external chip selects NC0 to NCS7. The area 0 is reserved for the addressing of the internal memories, and a second level of decoding provides 1M byte of internal memory area. The area 15 is reserved for the peripherals and provides access to the Advanced Peripheral Bus (APB).

Other areas are unused and performing an access within them provides an abort to the master requesting such an access.

## 8.1 Embedded Memories

### 8.1.1 Internal Memories

#### *8.1.1.1 Internal SRAM*

The SAM7SE512/256 embeds a high-speed 32-Kbyte SRAM bank. The SAM7SE32 embeds a high-speed 8-Kbyte SRAM bank. After reset and until the Remap Command is performed, the SRAM is only accessible at address 0x0020 0000. After Remap, the SRAM also becomes available at address 0x0.

#### *8.1.1.2 Internal ROM*

The SAM7SE512/256/32 embeds an Internal ROM. At any time, the ROM is mapped at address 0x30 0000. The ROM contains the FFPI and the SAM-BA boot program.

#### *8.1.1.3 Internal Flash*

- The SAM7SE512 features two banks of 256 Kbytes of Flash.
- The SAM7SE256 features one bank of 256 Kbytes of Flash.
- The SAM7SE32 features one bank of 32 Kbytes of Flash.

At any time, the Flash is mapped to address 0x0010 0000.

A general purpose NVM (GPNVM) bit is used to boot either on the ROM (default) or from the Flash.

This GPNVM bit can be cleared or set respectively through the commands “Clear General-purpose NVM Bit” and “Set General-purpose NVM Bit” of the EFC User Interface.

Setting the GPNVM bit 2 selects the boot from the Flash, clearing it selects the boot from the ROM. Asserting ERASE clears the GPNVM bit 2 and thus selects the boot from the ROM by default.

The security bit can only be enabled through the Command “Set Security Bit” of the EFC User Interface. Disabling the security bit can only be achieved by asserting the ERASE pin at 1 and after a full flash erase is performed. When the security bit is deactivated, all accesses to the flash are permitted.

It is important to note that the assertion of the ERASE pin should always be longer than 200 ms.

As the ERASE pin integrates a permanent pull-down, it can be left unconnected during normal operation. However, it is safer to connect it directly to GND for the final application.

#### *8.1.2.5 Non-volatile Brownout Detector Control*

Two general purpose NVM (GPNVM) bits are used for controlling the brownout detector (BOD), so that even after a power loss, the brownout detector operations remain in their state.

These two GPNVM bits can be cleared or set respectively through the commands “Clear General-purpose NVM Bit” and “Set General-purpose NVM Bit” of the EFC User Interface.

- GPNVM bit 0 is used as a brownout detector enable bit. Setting the GPNVM bit 0 enables the BOD, clearing it disables the BOD. Asserting ERASE clears the GPNVM bit 0 and thus disables the brownout detector by default.
- GPNVM bit 1 is used as a brownout reset enable signal for the reset controller. Setting the GPNVM bit 1 enables the brownout reset when a brownout is detected, Clearing the GPNVM bit 1 disables the brownout reset. Asserting ERASE disables the brownout reset by default.

#### *8.1.2.6 Calibration Bits*

Sixteen NVM bits are used to calibrate the brownout detector and the voltage regulator. These bits are factory configured and cannot be changed by the user. The ERASE pin has no effect on the calibration bits.

### 8.1.3 Fast Flash Programming Interface

The Fast Flash Programming Interface allows programming the device through either a serial JTAG interface or through a multiplexed fully-handshaked parallel port. It allows gang-programming with market-standard industrial programmers.

The FFPI supports read, page program, page erase, full erase, lock, unlock and protect commands.

The Fast Flash Programming Interface is enabled and the Fast Programming Mode is entered when the TST pin and the PA0 and PA1 pins are all tied high and PA2 tied to low.

- The Flash of the SAM7SE512 is organized in 2048 pages of 256 bytes (dual plane). It reads as 131,072 32-bit words.
- The Flash of the SAM7SE256 is organized in 1024 pages of 256 bytes (single plane). It reads as 65,536 32-bit words.
- The Flash of the SAM7SE32 is organized in 256 pages of 128 bytes (single plane). It reads as 32,768 32-bit words.
- The Flash of the SAM7SE512/256 contains a 256-byte write buffer, accessible through a 32-bit interface.
- The Flash of the SAM7SE32 contains a 128-byte write buffer, accessible through a 32-bit interface.

### 8.1.4 SAM-BA® Boot

The SAM-BA Boot is a default Boot Program which provides an easy way to program in-situ the on-chip Flash memory.

The SAM-BA Boot Assistant supports serial communication via the DBGU or the USB Device Port.

- Communication via the DBGU supports a wide range of crystals from 3 to 20 MHz via software auto-detection.
- Communication via the USB Device Port is limited to an 18.432 MHz crystal.

The SAM-BA Boot provides an interface with SAM-BA Graphic User Interface (GUI).

The SAM-BA Boot is in ROM and is mapped in Flash at address 0x0 when GPNVM bit 2 is set to 0.

## 8.2 External Memories

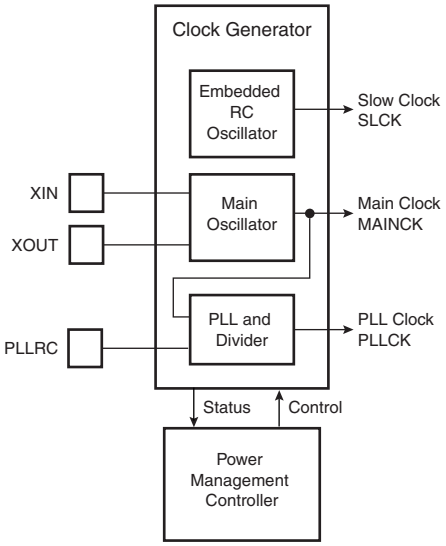
The external memories are accessed through the External Bus Interface.

Refer to the memory map in Figure 8-1 on page 22.

- Main Oscillator frequency ranges between 3 and 20 MHz
- Main Oscillator can be bypassed
- PLL output ranges between 80 and 220 MHz

It provides SLCK, MAINCK and PLLCK.

**Figure 9-2.** Clock Generator Block Diagram




## 9.3 Power Management Controller

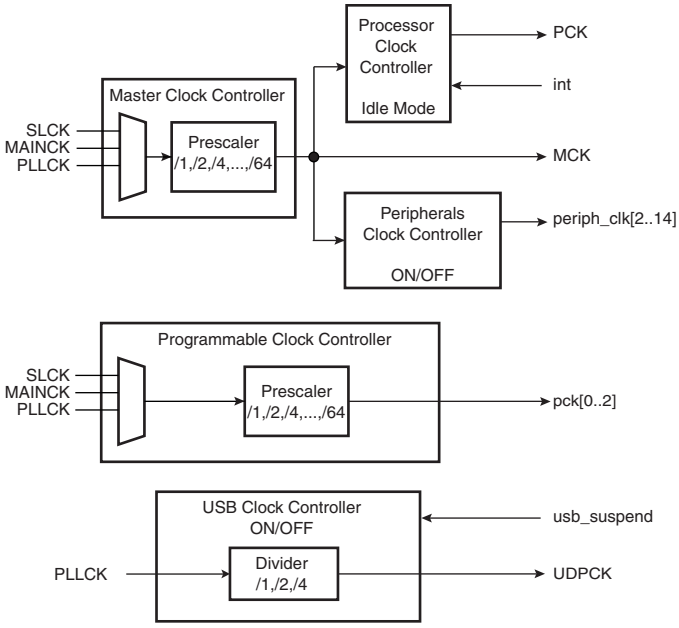
The Power Management Controller uses the Clock Generator outputs to provide:

- the Processor Clock PCK
- the Master Clock MCK
- the USB Clock UDPCK
- all the peripheral clocks, independently controllable
- three programmable clock outputs

The Master Clock (MCK) is programmable from a few hundred Hz to the maximum operating frequency of the device.

The Processor Clock (PCK) switches off when entering processor idle mode, thus allowing reduced power consumption while waiting for an interrupt.

**Figure 9-3.** Power Management Controller Block Diagram




## 9.4 Advanced Interrupt Controller

- Controls the interrupt lines (nIRQ and nFIQ) of an ARM Processor
- Individually maskable and vectored interrupt sources
  - Source 0 is reserved for the Fast Interrupt Input (FIQ)
  - Source 1 is reserved for system peripherals (RTT, PIT, EFC, PMC, DBGU, etc.)
  - Other sources control the peripheral interrupts or external interrupts
  - Programmable edge-triggered or level-sensitive internal sources
  - Programmable positive/negative edge-triggered or high/low level-sensitive external sources
- 8-level Priority Controller
  - Drives the normal interrupt nIRQ of the processor
  - Handles priority of the interrupt sources
  - Higher priority interrupts can be served during service of lower priority interrupt
- Vectoring
  - Optimizes interrupt service routine branch and execution
  - One 32-bit vector register per interrupt source
  - Interrupt vector register reads the corresponding current interrupt vector
- Protect Mode
  - Easy debugging by preventing automatic operations
- Fast Forcing
  - Permits redirecting any interrupt source on the fast interrupt
- General Interrupt Mask
  - Provides processor synchronization on events without triggering an interrupt

- Synchronous output, provides Set and Clear of several I/O lines in a single write

## 9.10 Voltage Regulator Controller

The purpose of this controller is to select the Power Mode of the Voltage Regulator between Normal Mode (bit 0 is cleared) or Standby Mode (bit 0 is set).

## 10.5 PIO Controller B Multiplexing

**Table 10-3.** Multiplexing on PIO Controller B

| PIO Controller B | | | | Application Usage | |
|---|---|---|---|---|---|
| **I/O Line** | **Peripheral A** | **Peripheral B** | **Comments** | **Function** | **Comments** |
| PB0 | TIOA0 | A0/NBS0 | | | |
| PB1 | TIOB0 | A1/NBS2 | | | |
| PB2 | SCK0 | A2 | | | |
| PB3 | NPCS3 | A3 | | | |
| PB4 | TCLK0 | A4 | | | |
| PB5 | NPCS3 | A5 | | | |
| PB6 | PCK0 | A6 | | | |
| PB7 | PWM3 | A7 | | | |
| PB8 | ADTRG | A8 | | | |
| PB9 | NPCS1 | A9 | | | |
| PB10 | NPCS2 | A10 | | | |
| PB11 | PWM0 | A11 | | | |
| PB12 | PWM1 | A12 | | | |
| PB13 | PWM2 | A13 | | | |
| PB14 | PWM3 | A14 | | | |
| PB15 | TIOA1 | A15 | | | |
| PB16 | TIOB1 | A16/BA0 | | | |
| PB17 | PCK1 | A17/BA1 | | | |
| PB18 | PCK2 | D16 | | | |
| PB19 | FIQ | D17 | | | |
| PB20 | IRQ0 | D18 | | | |
| PB21 | PCK1 | D19 | | | |
| PB22 | NPCS3 | D20 | | | |
| PB23 | PWM0 | D21 | | | |
| PB24 | PWM1 | D22 | | | |
| PB25 | PWM2 | D23 | | | |
| PB26 | TIOA2 | D24 | | | |
| PB27 | TIOB2 | D25 | | | |
| PB28 | TCLK1 | D26 | | | |
| PB29 | TCLK2 | D27 | | | |
| PB30 | NPCS2 | D28 | | | |
| PB31 | PCK2 | D29 | | | |

## 10.13 USB Device Port

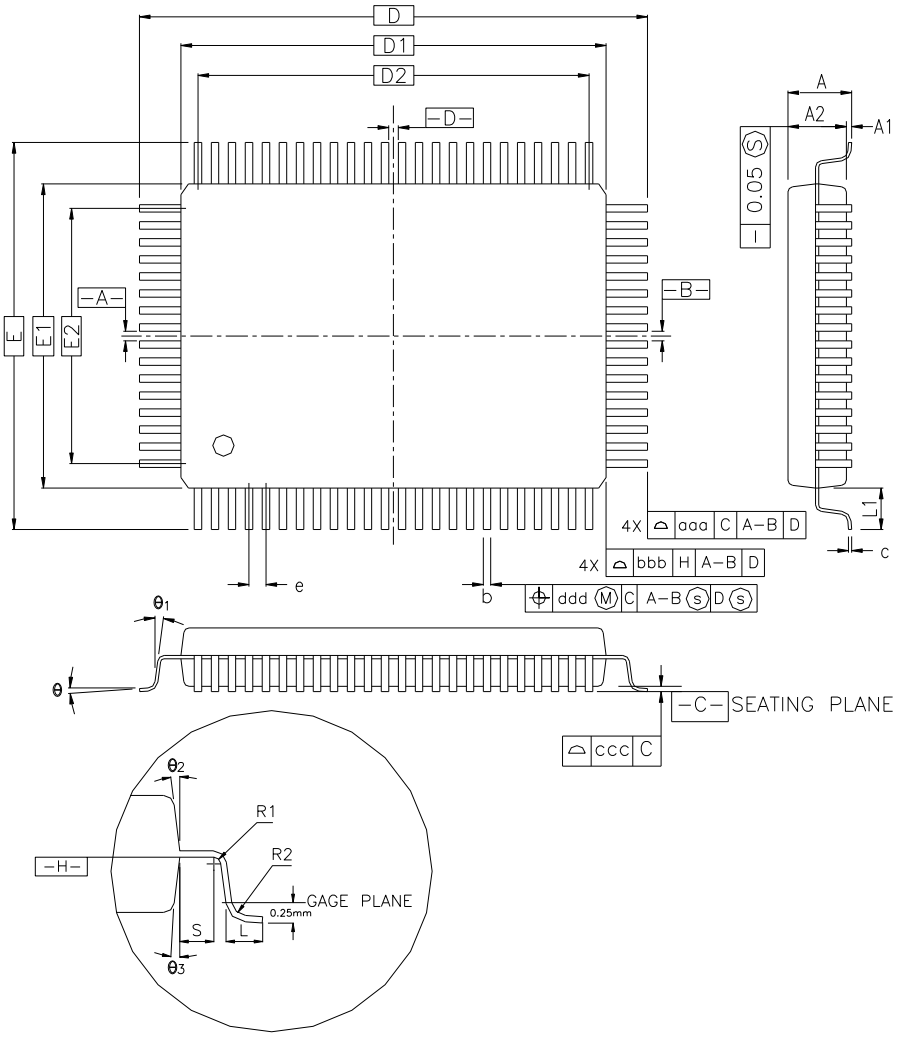
- USB V2.0 full-speed compliant,12 Mbits per second.
- Embedded USB V2.0 full-speed transceiver
- Embedded 2688-byte dual-port RAM for endpoints
- Eight endpoints
  - Endpoint 0: 64bytes
  - Endpoint 1 and 2: 64 bytes ping-pong
  - Endpoint 3: 64 bytes
  - Endpoint 4 and 5: 512 bytes ping-pong
  - Endpoint 6 and 7: 64 bytes ping-pong
  - Ping-pong Mode (two memory banks) for Isochronous and bulk endpoints
- Suspend/resume logic
- Integrated Pull-up on DDP

## 10.14 Analog-to-Digital Converter

- 8-channel ADC
- 10-bit 384 Ksamples/sec. or 8-bit 583 Ksamples/sec. Successive Approximation Register ADC
- ±2 LSB Integral Non Linearity, ±1 LSB Differential Non Linearity
- Integrated 8-to-1 multiplexer, offering eight independent 3.3V analog inputs
- External voltage reference for better accuracy on low voltage inputs
- Individual enable and disable of each channel
- Multiple trigger sources
  - Hardware or software trigger
  - External trigger pin
  - Timer Counter 0 to 2 outputs TIOA0 to TIOA2 trigger
- Sleep Mode and conversion sequencer
  - Automatic wakeup on trigger and back to sleep mode after conversions of all enabled channels
- Each analog input shared with digital signals

## 11. Package Drawings

**Figure 11-1.** 128-lead LQFP Package Drawing




COTROL DIMENSIONS ARE IN MILLIMETERS.

| SYMBOL | MILLIMETER | | | INCH | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | — | — | 1.60 | — | — | 0.063 |
| $A_1$ | 0.05 | — | 0.15 | 0.002 | — | 0.006 |
| $A_2$ | 1.35 | 1.40 | 1.45 | 0.053 | 0.055 | 0.057 |
| D | 22.00 BSC. | | | 0.866 BSC. | | |
| $D_1$ | 20.00 BSC. | | | 0.787 BSC. | | |
| E | 16.00 BSC. | | | 0.630 BSC. | | |
| $E_1$ | 14.00 BSC. | | | 0.551 BSC. | | |
| $R_2$ | 0.08 | — | 0.20 | 0.003 | — | 0.008 |
| $R_1$ | 0.08 | — | — | 0.003 | — | — |
| θ | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| $\theta_1$ | 0° | — | — | 0° | — | — |
| $\theta_2$ | 11° | 12° | 13° | 11° | 12° | 13° |
| $\theta_3$ | 11° | 12° | 13° | 11° | 12° | 13° |
| c | 0.09 | — | 0.20 | 0.004 | — | 0.008 |
| L | 0.45 | 0.60 | 0.75 | 0.018 | 0.024 | 0.030 |
| $L_1$ | 1.00 REF | | | 0.039 REF | | |
| S | 0.20 | — | — | 0.008 | — | — |
| b | 0.17 | 0.20 | 0.27 | 0.007 | 0.008 | 0.011 |
| e | 0.50 BSC. | | | 0.020 BSC. | | |
| D2 | 18.50 | | | 0.728 | | |
| E2 | 12.50 | | | 0.492 | | |
| TOLERANCES OF FORM AND POSITION | | | | | | |
| aaa | 0.20 | | | 0.008 | | |
| bbb | 0.20 | | | 0.008 | | |
| ccc | 0.08 | | | 0.003 | | |
| ddd | 0.08 | | | 0.003 | | |

# Revision History

| Doc. Rev | Comments | Change Request Ref. |
|---|---|---|
| 6222AS | First issue | |
| | Revised Memories with condensed mapping.<br>Added Package Outlines and 144-ball LFBGA pin and ordering information. | #2709 |
| 6222BS | Section 12. “Ordering Information” on page 45 ordering information code reference changed | #3699 |
| 6222CS | Section 6.1 ”JTAG Port Pins”, Section 6.3 ”Reset Pin”, Section 6.5 ”SDCK Pin”, removed statement: “not 5V tolerant” | #3826 |
| | Section 7.6 ”SDRAM Controller”, Mobile SDRAM controller added to SDRAMC features | |
| | INL and DNL updated in Section 10.14 ”Analog-to-Digital Converter” | #4005 |
| | “Features” on page 2, Fully Static Operation; added, up to 55 MHz at 1.8V and 85°C worst case conditions | #3924 |
| | Section 7.1 ”ARM7TDMI Processor”, Runs at up to 55 MHz, providing 0.9 MIPS/MHz (core supplied with 1.8V) | |
| | Section 7.8 ”Peripheral DMA Controller” PDC priority list added | #3833 |
| | Section 7.5 ”Static Memory Controller”, Multiple device adaptability includes: compliant w/PSRAM in synchronous operations. | review |
| 6222DS | Figure 8-1 ”SAM7SE Memory Mapping” Compact Flash not shown w/EBI Chip Select 5. Compact Flash is shown with EBI Chip Select 2. | 4804 |
| | Section 8.1.2.1 ”Flash Overview”, updated AT91SAM7SE32 ...”reads as 8192 32-bit words.” | 4512 |
| | Section 6. ”/O Lines Considerations”, “JTAG Port Pins”, “Test Pin”, “Reset Pin”, “ERASE Pin” descriptions updated | 5062 |
| 6222ES | Section 10.11 ”Timer Counter”, .....the TC has two output compare and one input capture per channel. | 4209 |
| 6222FS | **Features:** | |
| | “Mode for General Purpose Two-wire UART Serial Communication” added to “Debug Unit (DBGU)”. | 5846 |
| | **Signal Description:** | |
| | Table 3-1, “Signal Description List”, AD0-AD3 and AD4-AD7 comments reversed. | 5271 |
| | **System Controller:** | |
| | Figure 9-1 ”System Controller Block Diagram”, ‘periph_nreset’ changed into ‘power_on_reset’ for RTT. | 5222 |
| 6222GS | MRL B Ordering Codes added to Table 12-1, “Ordering Information” | 7749 |
| | ‘Product Description’ changed to ‘AT91SAM ARM-based Flash MCU’ on the first page. | |
| | ‘AT91SAM’ product prefix changed to ‘SAM’, except for Chip ID and ordering codes. | rfo |