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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	55MHz
Connectivity	EBI/EMI, I²C, SPI, SSC, UART/USART, USB
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	88
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 1.95V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LFBGA
Supplier Device Package	144-BGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at91sam7se512-cu

1. Description

Atmel's SAM7SE Series is a member of its Smart ARM Microcontroller family based on the 32-bit ARM7™ RISC processor and high-speed Flash memory.

- SAM7SE512 features a 512-Kbyte high-speed Flash and a 32 Kbyte SRAM.
- SAM7SE256 features a 256-Kbyte high-speed Flash and a 32 Kbyte SRAM.
- SAM7SE32 features a 32-Kbyte high-speed Flash and an 8 Kbyte SRAM.

It also embeds a large set of peripherals, including a USB 2.0 device, an External Bus Interface (EBI), and a complete set of system functions minimizing the number of external components.

The EBI incorporates controllers for synchronous DRAM (SDRAM) and Static memories and features specific circuitry facilitating the interface for NAND Flash, SmartMedia and CompactFlash.

The device is an ideal migration path for 8/16-bit microcontroller users looking for additional performance, extended memory and higher levels of system integration.

The embedded Flash memory can be programmed in-system via the JTAG-ICE interface or via a parallel interface on a production programmer prior to mounting. Built-in lock bits and a security bit protect the firmware from accidental overwrite and preserve its confidentiality.

The SAM7SE Series system controller includes a reset controller capable of managing the power-on sequence of the microcontroller and the complete system. Correct device operation can be monitored by a built-in brownout detector and a watchdog running off an integrated RC oscillator.

By combining the ARM7TDMI processor with on-chip Flash and SRAM, and a wide range of peripheral functions, including USART, SPI, External Bus Interface, Timer Counter, RTT and Analog-to-Digital Converters on a monolithic chip, the SAM7SE512/256/32 is a powerful device that provides a flexible, cost-effective solution to many embedded control applications.

1.1 Configuration Summary of the SAM7SE512, SAM7SE256 and SAM7SE32

The SAM7SE512, SAM7SE256 and SAM7SE32 differ in memory sizes and organization. [Table 1-1](#) below summarizes the configurations for the three devices.

Table 1-1. Configuration Summary

Device	Flash Size	Flash Organization	RAM Size
SAM7SE512	512K bytes	dual plane	32K bytes
SAM7SE256	256K bytes	single plane	32K bytes
SAM7SE32	32K bytes	single plane	8K bytes

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Comments
Two-Wire Interface				
TWD	Two-wire Serial Data	I/O		
TWCK	Two-wire Serial Clock	I/O		
Analog-to-Digital Converter				
AD0-AD3	Analog Inputs	Analog		Digital pulled-up inputs at reset
AD4-AD7	Analog Inputs	Analog		Analog Inputs
ADTRG	ADC Trigger	Input		
ADVREF	ADC Reference	Analog		
Fast Flash Programming Interface				
PGMEN0-PGMEN2	Programming Enabling	Input		
PGMM0-PGMM3	Programming Mode	Input		
PGMD0-PGMD15	Programming Data	I/O		
PGMRDY	Programming Ready	Output	High	
PGMNVALID	Data Direction	Output	Low	
PGMNOE	Programming Read	Input	Low	
PGMCK	Programming Clock	Input		
PGMNCMD	Programming Command	Input	Low	
External Bus Interface				
D[31:0]	Data Bus	I/O		
A[22:0]	Address Bus	Output		
NWAIT	External Wait Signal	Input	Low	
Static Memory Controller				
NCS[7:0]	Chip Select Lines	Output	Low	
NWR[1:0]	Write Signals	Output	Low	
NRD	Read Signal	Output	Low	
NWE	Write Enable	Output	Low	
NUB	NUB: Upper Byte Select	Output	Low	
NLB	NLB: Lower Byte Select	Output	Low	
EBI for CompactFlash Support				
CFCE[2:1]	CompactFlash Chip Enable	Output	Low	
CFOE	CompactFlash Output Enable	Output	Low	
CFWE	CompactFlash Write Enable	Output	Low	
CFIOR	CompactFlash I/O Read Signal	Output	Low	
CFIOW	CompactFlash I/O Write Signal	Output	Low	
CFRNW	CompactFlash Read Not Write Signal	Output		
CFCS[1:0]	CompactFlash Chip Select Lines	Output	Low	

4.4 144-ball LFBGA Pinout

Table 4-2. SAM7SE512/256/32 Pinout for 144-ball LFBGA Package

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
A1	PB7	D1	VDDCORE	G1	PC18	K1	PC11
A2	PB8	D2	VDDCORE	G2	PC16	K2	PC6
A3	PB9	D3	PB2	G3	PC17	K3	PC2
A4	PB12	D4	TDO	G4	PC9	K4	PC0
A5	PB13	D5	TDI	G5	VDDIO	K5	PA27/PGMD15
A6	PB16	D6	PB17	G6	GND	K6	PA26/PGMD14
A7	PB22	D7	PB26	G7	GND	K7	GND
A8	PB23	D8	PA14/PGMD2	G8	GND	K8	VDDCORE
A9	PB25	D9	PA12/PGMD0	G9	GND	K9	VDDFLASH
A10	PB29	D10	PA11/PGMM3	G10	AD4	K10	VDDIO
A11	PB30	D11	PA8/PGMM0	G11	VDDIN	K11	VDDIO
A12	PB31	D12	PA7/PGMNVAILD	G12	VDDOUT	K12	PA18/PGMD6/AD1
B1	PB6	E1	PC22	H1	PC15	L1	SDCK
B2	PB3	E2	PC23	H2	PC14	L2	PC7
B3	PB4	E3	NRST	H3	PC13	L3	PC4
B4	PB10	E4	TCK	H4	VDDCORE	L4	PC1
B5	PB14	E5	ERASE	H5	VDDCORE	L5	PA29
B6	PB18	E6	TEST	H6	GND	L6	PA24/PGMD12
B7	PB20	E7	VDDCORE	H7	GND	L7	PA21/PGMD9
B8	PB24	E8	VDDCORE	H8	GND	L8	ADVREF
B9	PB28	E9	GND	H9	GND	L9	VDDFLASH
B10	PA4/PGMNCMD	E10	PA9/PGMM1	H10	PA19/PGMD7/AD2	L10	VDDFLASH
B11	PA0/PGMEN0	E11	PA10/PGMM2	H11	PA20/PGMD8/AD3	L11	PA17/PGMD5/AD0
B12	PA1/PGMEN1	E12	PA13/PGMD1	H12	VDDIO	L12	GND
C1	PB0	F1	PC21	J1	PC12	M1	PC8
C2	PB1	F2	PC20	J2	PC10	M2	PC5
C3	PB5	F3	PC19	J3	PA30	M3	PC3
C4	PB11	F4	JTAGSEL	J4	PA28	M4	PA31
C5	PB15	F5	TMS	J5	PA23/PGMD11	M5	PA25/PGMD13
C6	PB19	F6	VDDIO	J6	PA22/PGMD10	M6	DM
C7	PB21	F7	GND	J7	AD6	M7	DP
C8	PB27	F8	GND	J8	AD7	M8	GND
C9	PA6/PGMNOE	F9	GND	J9	VDDCORE	M9	XIN/PGMCK
C10	PA5/PGMRDY	F10	AD5	J10	VDDCORE	M10	XOUT
C11	PA2/PGMEN2	F11	PA15/PGMD3	J11	VDDCORE	M11	PLLRC
C12	PA3	F12	PA16/PGMD4	J12	VDDIO	M12	VDDPLL

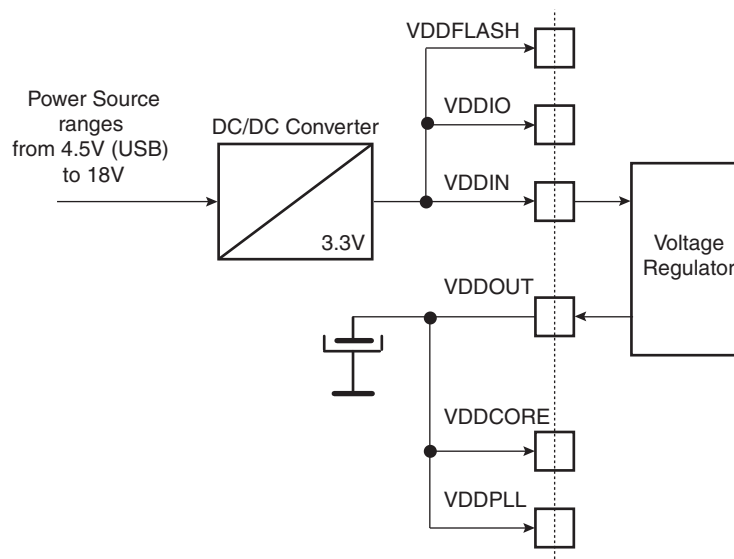
- One external 2.2 μF (or 3.3 μF) X7R capacitor should be connected between VDDOUT and GND.

Adequate input supply decoupling is mandatory for VDDIN in order to improve startup stability and reduce source voltage drop. The input decoupling capacitor should be placed close to the chip. For example, two capacitors can be used in parallel: 100 nF NPO and 4.7 μF X7R.

5.4 Typical Powering Schematics

The SAM7SE512/256/32 supports a 3.3V single supply mode. The internal regulator input connected to the 3.3V source and its output feeds VDDCORE and the VDDPLL. [Figure 5-1](#) shows the power schematics to be used for USB bus-powered systems.

Figure 5-1. 3.3V System Single Power Supply Schematic



6. /O Lines Considerations

6.1 JTAG Port Pins

TMS, TDI and TCK are Schmitt trigger inputs. TMS, TDI and TCK do not integrate a pull-up resistor.

TDO is an output, driven at up to VDDIO, and has no pull-up resistor.

The JTAGSEL pin is used to select the JTAG boundary scan when asserted at a high level. The JTAGSEL pin integrates a permanent pull-down resistor of about 15 k Ω .

To eliminate any risk of spuriously entering the JTAG boundary scan mode due to noise on JTAGSEL, it should be tied externally to GND if boundary scan is not used, or put in place an external low value resistor (such as 1 k Ω).

6.2 Test Pin

The TST pin is used for manufacturing test or fast programming mode of the SAM7SE512/256/32 when asserted high. The TST pin integrates a permanent pull-down resistor of about 15 k Ω to GND.

To eliminate any risk of entering the test mode due to noise on the TST pin, it should be tied to GND if the FFPI is not used, or put in place an external low value resistor (such as 1 k Ω).

To enter fast programming mode, the TST pin and the PA0 and PA1 pins should be tied high and PA2 tied low.

Driving the TST pin at a high level while PA0 or PA1 is driven at 0 leads to unpredictable results.

6.3 Reset Pin

The NRST pin is bidirectional with an open-drain output buffer. It is handled by the on-chip reset controller and can be driven low to provide a reset signal to the external components or asserted low externally to reset the microcontroller. There is no constraint on the length of the reset pulse, and the reset controller can guarantee a minimum pulse length. This allows connection of a simple push-button on the NRST pin as system user reset, and the use of the NRST signal to reset all the components of the system.

An external power-on reset can drive this pin during the start-up instead of using the internal power-on reset circuit.

The NRST pin integrates a permanent pull-up of about 100 k Ω resistor to VDDIO.

This pin has Schmitt trigger input.

6.4 ERASE Pin

The ERASE pin is used to re-initialize the Flash content and some of its NVM bits. It integrates a permanent pull-down resistor of about 15 k Ω to GND.

To eliminate any risk of erasing the Flash due to noise on the ERASE pin, it should be tied externally to GND, which prevents erasing the Flash from the application, or put in place an external low value resistor (such as 1 k Ω).

This pin is debounced by the RC oscillator to improve the glitch tolerance. When the pin is tied to high during less than 100 ms, ERASE pin is not taken into account. The pin must be tied high during more than 220 ms to perform the re-initialization of the Flash.

6.5 SDCK Pin

The SDCK pin is dedicated to the SDRAM Clock and is an output-only without pull-up. Maximum Output Frequency of this pad is 48 MHz at 3.0V and 25 MHz at 1.65V with a maximum load of 30 pF.

6.6 PIO Controller lines

All the I/O lines PA0 to PA31, PB0 to PB31, PC0 to PC23 integrate a programmable pull-up resistor. Programming of this pull-up resistor is performed independently for each I/O line through the PIO controllers.

Typical pull-up value is 100 k Ω .

All the I/O lines have schmitt trigger inputs.

6.7 I/O Lines Current Drawing

The PIO lines PA0 to PA3 are high-drive current capable. Each of these I/O lines can drive up to 16 mA permanently.

The remaining I/O lines can draw only 8 mA.

However, the total current drawn by all the I/O lines cannot exceed 300 mA.

- Individually programmable size between 1K Byte and 1M Byte
- Individually programmable protection against write and/or user access
- Peripheral protection against write and/or user access
- Embedded Flash Controller
 - Embedded Flash interface, up to three programmable wait states
 - Prefetch buffer, buffering and anticipating the 16-bit requests, reducing the required wait states
 - Key-protected program, erase and lock/unlock sequencer
 - Single command for erasing, programming and locking operations
 - Interrupt generation in case of forbidden operation

7.4 External Bus Interface

- Integrates Three External Memory Controllers:
 - Static Memory Controller
 - SDRAM Controller
 - ECC Controller
- Additional Logic for NAND Flash and CompactFlash® Support
 - NAND Flash support: 8-bit as well as 16-bit devices are supported
 - CompactFlash support: all modes (Attribute Memory, Common Memory, I/O, True IDE) are supported but the signals _IOIS16 (I/O and True IDE modes) and -ATA SEL (True IDE mode) are not handled.
- Optimized External Bus:
 - 16- or 32-bit Data Bus (32-bit Data Bus for SDRAM only)
 - Up to 23-bit Address Bus, Up to 8-Mbytes Addressable
 - Up to 8 Chip Selects, each reserved to one of the eight Memory Areas
 - Optimized pin multiplexing to reduce latencies on External Memories
- Configurable Chip Select Assignment:
 - Static Memory Controller on NCS0
 - SDRAM Controller or Static Memory Controller on NCS1
 - Static Memory Controller on NCS2, Optional CompactFlash Support
 - Static Memory Controller on NCS3, NCS5 - NCS6, Optional NAND Flash Support
 - Static Memory Controller on NCS4, Optional CompactFlash Support
 - Static Memory Controller on NCS7

7.5 Static Memory Controller

- External memory mapping, 512-Mbyte address space
- 8-, or 16-bit Data Bus
- Up to 8 Chip Select Lines
- Multiple Access Modes supported
 - Byte Write or Byte Select Lines
 - Two different Read Protocols for each Memory Bank

7.8 Peripheral DMA Controller

- Handles data transfer between peripherals and memories
- Eleven channels
 - Two for each USART
 - Two for the Debug Unit
 - Two for the Serial Synchronous Controller
 - Two for the Serial Peripheral Interface
 - One for the Analog-to-digital Converter
- Low bus arbitration overhead
 - One Master Clock cycle needed for a transfer from memory to peripheral
 - Two Master Clock cycles needed for a transfer from peripheral to memory
- Next Pointer management for reducing interrupt latency requirements
- Peripheral DMA Controller (PDC) priority is as follows (from the highest priority to the lowest):

Receive	DBGU
Receive	USART0
Receive	USART1
Receive	SSC
Receive	ADC
Receive	SPI
Transmit	DBGU
Transmit	USART0
Transmit	USART1
Transmit	SSC
Transmit	SPI

Figure 8-2. Internal Memory Mapping with GPNVM Bit 2 = 0 (default)

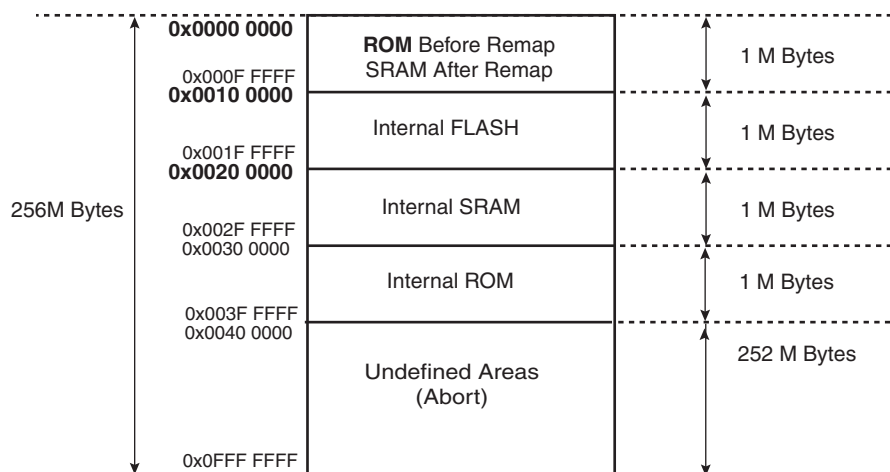
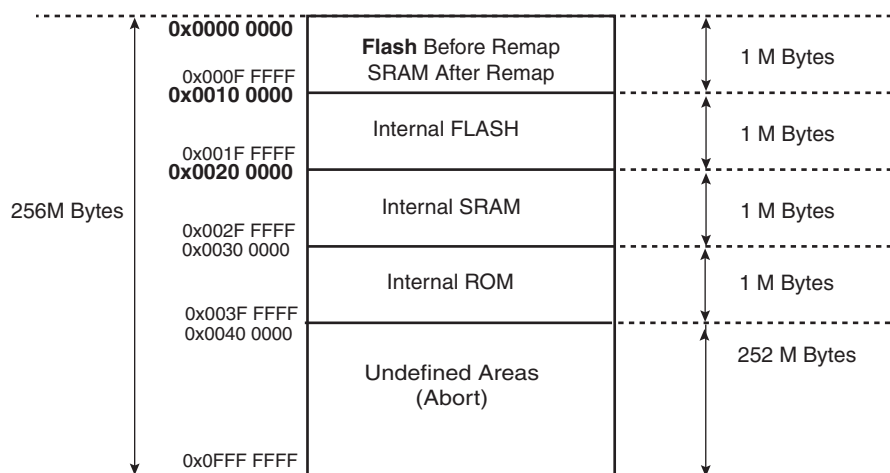


Figure 8-3. Internal Memory Mapping with GPNVM Bit 2 = 1



8.1.2 Embedded Flash

8.1.2.1 Flash Overview

The Flash of the SAM7SE512 is organized in two banks (dual plane) of 1024 pages of 256 bytes. It reads as 131,072 32-bit words.

The Flash of the SAM7SE256 is organized in 1024 pages (single plane) of 256 bytes. It reads as 65,536 32-bit words.

The Flash of the SAM7SE32 is organized in 256 pages (single plane) of 128 bytes. It reads as 8192 32-bit words.

The Flash of the SAM7SE32 contains a 128-byte write buffer, accessible through a 32-bit interface.

The Flash of the SAM7SE512/256 contains a 256-byte write buffer, accessible through a 32-bit interface.

The Flash benefits from the integration of a power reset cell and from the brownout detector. This prevents code corruption during power supply changes, even in the worst conditions.

8.1.2.2 *Embedded Flash Controller*

The Embedded Flash Controller (EFC) manages accesses performed by the masters of the system. It enables reading the Flash and writing the write buffer. It also contains a User Interface, mapped within the Memory Controller on the APB. The User Interface allows:

- programming of the access parameters of the Flash (number of wait states, timings, etc.)
- starting commands such as full erase, page erase, page program, NVM bit set, NVM bit clear, etc.
- getting the end status of the last command
- getting error status
- programming interrupts on the end of the last commands or on errors

The Embedded Flash Controller also provides a dual 32-bit Prefetch Buffer that optimizes 16-bit access to the Flash. This is particularly efficient when the processor is running in Thumb mode.

- Two EFCs (EFC0 and EFC1) are embedded in the SAM7SE512 to control each plane of 256 KBytes. Dual plane organization allows concurrent Read and Program.
- One EFC (EFC0) is embedded in the SAM7SE256 to control the single plane 256 KBytes.
- One EFC (EFC0) is embedded in the SAM7SE32 to control the single plane 32 KBytes.

8.1.2.3 *Lock Regions*

The SAM7SE512 Embedded Flash Controller manages 32 lock bits to protect 32 regions of the flash against inadvertent flash erasing or programming commands. The SAM7SE512 contains 32 lock regions and each lock region contains 64 pages of 256 bytes. Each lock region has a size of 16 Kbytes.

The SAM7SE256 Embedded Flash Controller manages 16 lock bits to protect 16 regions of the flash against inadvertent flash erasing or programming commands. The SAM7SE256 contains 16 lock regions and each lock region contains 64 pages of 256 bytes. Each lock region has a size of 16 Kbytes.

The SAM7SE32 Embedded Flash Controller manages 8 lock bits to protect 8 regions of the flash against inadvertent flash erasing or programming commands. The SAM7SE32 contains 8 lock regions and each lock region contains 32 pages of 128 bytes. Each lock region has a size of 4 Kbytes.

If a locked-region's erase or program command occurs, the command is aborted and the EFC triggers an interrupt.

The 32 (SAM7SE512), 16 (SAM7SE256) or 8 (SAM7SE32) NVM bits are software programmable through the EFC User Interface. The command "Set Lock Bit" enables the protection. The command "Clear Lock Bit" unlocks the lock region.

Asserting the ERASE pin clears the lock bits, thus unlocking the entire Flash.

8.1.2.4 *Security Bit Feature*

The SAM7SE512/256/32 features a security bit, based on a specific NVM-bit. When the security is enabled, any access to the Flash, either through the ICE interface or through the Fast Flash Programming Interface, is forbidden.

8.1.4 SAM-BA® Boot

The SAM-BA Boot is a default Boot Program which provides an easy way to program in-situ the on-chip Flash memory.

The SAM-BA Boot Assistant supports serial communication via the DBGU or the USB Device Port.

- Communication via the DBGU supports a wide range of crystals from 3 to 20 MHz via software auto-detection.
- Communication via the USB Device Port is limited to an 18.432 MHz crystal.

The SAM-BA Boot provides an interface with SAM-BA Graphic User Interface (GUI).

The SAM-BA Boot is in ROM and is mapped in Flash at address 0x0 when GPNVM bit 2 is set to 0.

8.2 External Memories

The external memories are accessed through the External Bus Interface.

Refer to the memory map in [Figure 8-1 on page 22](#).

9.5 Debug Unit

- Comprises:
 - One two-pin UART
 - One Interface for the Debug Communication Channel (DCC) support
 - One set of Chip ID Registers
 - One Interface providing ICE Access Prevention
- Two-pin UART
 - USART-compatible User Interface
 - Programmable Baud Rate Generator
 - Parity, Framing and Overrun Error
 - Automatic Echo, Local Loopback and Remote Loopback Channel Modes
- Debug Communication Channel Support
 - Offers visibility of COMMRX and COMMTX signals from the ARM Processor
- Chip ID Registers
 - Identification of the device revision, sizes of the embedded memories, set of peripherals
 - Chip ID is 0x272A 0A40 (VERSION 0) for SAM7SE512
 - Chip ID is 0x272A 0940 (VERSION 0) for SAM7SE256
 - Chip ID is 0x2728 0340 (VERSION 0) for SAM7SE32

9.6 Periodic Interval Timer

- 20-bit programmable counter plus 12-bit interval counter

9.7 Watchdog Timer

- 12-bit key-protected Programmable Counter running on prescaled SLCK
- Provides reset or interrupt signals to the system
- Counter may be stopped while the processor is in debug state or in idle mode

9.8 Real-time Timer

- 32-bit free-running counter with alarm running on prescaled SLCK
- Programmable 16-bit prescaler for SLCK accuracy compensation

9.9 PIO Controllers

- Three PIO Controllers. PIO A and B each control 32 I/O lines and PIO C controls 24 I/O lines.
- Fully programmable through set/clear registers
- Multiplexing of two peripheral functions per I/O line
- For each I/O line (whether assigned to a peripheral or used as general-purpose I/O)
 - Input change interrupt
 - Half a clock period glitch filter
 - Multi-drive option enables driving in open drain
 - Programmable pull-up on each I/O line
 - Pin data status register, supplies visibility of the level on the pin at any time

10. Peripherals

10.1 User Interface

The User Peripherals are mapped in the 256 MBytes of the address space between 0xF000 0000 and 0xFFFF EFFF. Each peripheral is allocated 16 Kbytes of address space.

A complete memory map is presented in [Figure 8-1 on page 22](#).

10.2 Peripheral Identifiers

The SAM7SE512/256/32 embeds a wide range of peripherals. [Table 10-1](#) defines the Peripheral Identifiers of the SAM7SE512/256/32. Unique peripheral identifiers are defined for both the Advanced Interrupt Controller and the Power Management Controller.

Table 10-1. Peripheral Identifiers

Peripheral ID	Peripheral Mnemonic	Peripheral Name	External Interrupt
0	AIC	Advanced Interrupt Controller	FIQ
1	SYSC ⁽¹⁾		
2	PIOA	Parallel I/O Controller A	
3	PIOB	Parallel I/O Controller B	
4	PIOC	Parallel I/O Controller C	
5	SPI	Serial Peripheral Interface 0	
6	US0	USART 0	
7	US1	USART 1	
8	SSC	Synchronous Serial Controller	
9	TWI	Two-wire Interface	
10	PWMC	PWM Controller	
11	UDP	USB Device Port	
12	TC0	Timer/Counter 0	
13	TC1	Timer/Counter 1	
14	TC2	Timer/Counter 2	
15	ADC ⁽¹⁾	Analog-to Digital Converter	
16-28	reserved		
29	AIC	Advanced Interrupt Controller	IRQ0
30	AIC	Advanced Interrupt Controller	IRQ1

Note: 1. Setting SYSC and ADC bits in the clock set/clear registers of the PMC has no effect. The System Controller is continuously clocked. The ADC clock is automatically started for the first conversion. In Sleep Mode the ADC clock is automatically stopped after each conversion.

10.5 PIO Controller B Multiplexing

Table 10-3. Multiplexing on PIO Controller B

PIO Controller B				Application Usage	
I/O Line	Peripheral A	Peripheral B	Comments	Function	Comments
PB0	TIOA0	A0/NBS0			
PB1	TIOB0	A1/NBS2			
PB2	SCK0	A2			
PB3	NPCS3	A3			
PB4	TCLK0	A4			
PB5	NPCS3	A5			
PB6	PCK0	A6			
PB7	PWM3	A7			
PB8	ADTRG	A8			
PB9	NPCS1	A9			
PB10	NPCS2	A10			
PB11	PWM0	A11			
PB12	PWM1	A12			
PB13	PWM2	A13			
PB14	PWM3	A14			
PB15	TIOA1	A15			
PB16	TIOB1	A16/BA0			
PB17	PCK1	A17/BA1			
PB18	PCK2	D16			
PB19	FIQ	D17			
PB20	IRQ0	D18			
PB21	PCK1	D19			
PB22	NPCS3	D20			
PB23	PWM0	D21			
PB24	PWM1	D22			
PB25	PWM2	D23			
PB26	TIOA2	D24			
PB27	TIOB2	D25			
PB28	TCLK1	D26			
PB29	TCLK2	D27			
PB30	NPCS2	D28			
PB31	PCK2	D29			

- Offers a configurable frame sync and data length
- Receiver and transmitter can be programmed to start automatically or on detection of different event on the frame sync signal
- Receiver and transmitter include a data signal, a clock signal and a frame synchronization signal

10.11 Timer Counter

- Three 16-bit Timer Counter Channels
 - Two output compare or one input capture per channel
- Wide range of functions including:
 - Frequency measurement
 - Event counting
 - Interval measurement
 - Pulse generation
 - Delay timing
 - Pulse Width Modulation
 - Up/down capabilities
- Each channel is user-configurable and contains:
 - Three external clock inputs
 - Five internal clock inputs, as defined in [Table 10-4](#)

Table 10-4. Timer Counter Clocks Assignment

TC Clock input	Clock
TIMER_CLOCK1	MCK/2
TIMER_CLOCK2	MCK/8
TIMER_CLOCK3	MCK/32
TIMER_CLOCK4	MCK/128
TIMER_CLOCK5	MCK/1024

- Two multi-purpose input/output signals
- Two global registers that act on all three TC channels

10.12 PWM Controller

- Four channels, one 16-bit counter per channel
- Common clock generator, providing thirteen different clocks
 - One Modulo n counter providing eleven clocks
 - Two independent linear dividers working on modulo n counter outputs
- Independent channel programming
 - Independent enable/disable commands
 - Independent clock selection
 - Independent period and duty cycle, with double buffering
 - Programmable selection of the output waveform polarity
 - Programmable center or left aligned output waveform

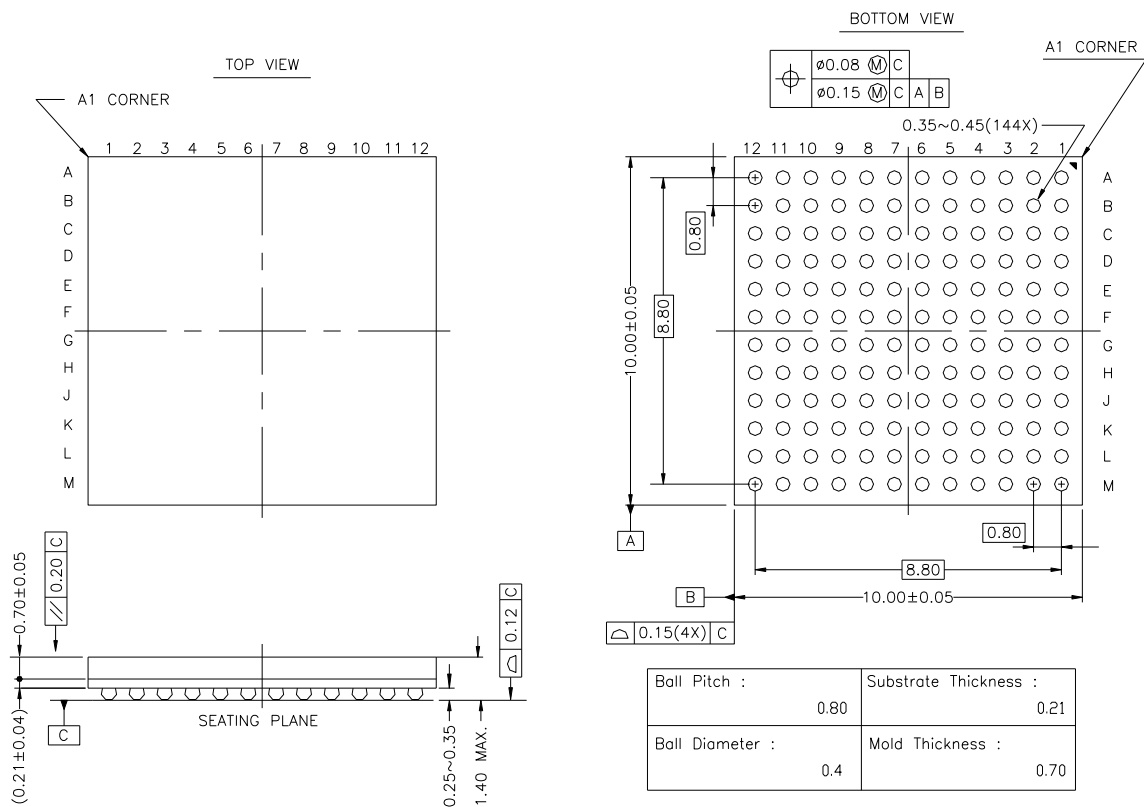
10.13 USB Device Port

- USB V2.0 full-speed compliant, 12 Mbits per second.
- Embedded USB V2.0 full-speed transceiver
- Embedded 2688-byte dual-port RAM for endpoints
- Eight endpoints
 - Endpoint 0: 64bytes
 - Endpoint 1 and 2: 64 bytes ping-pong
 - Endpoint 3: 64 bytes
 - Endpoint 4 and 5: 512 bytes ping-pong
 - Endpoint 6 and 7: 64 bytes ping-pong
 - Ping-pong Mode (two memory banks) for Isochronous and bulk endpoints
- Suspend/resume logic
- Integrated Pull-up on DDP

10.14 Analog-to-Digital Converter

- 8-channel ADC
- 10-bit 384 Ksamples/sec. or 8-bit 583 Ksamples/sec. Successive Approximation Register ADC
- ± 2 LSB Integral Non Linearity, ± 1 LSB Differential Non Linearity
- Integrated 8-to-1 multiplexer, offering eight independent 3.3V analog inputs
- External voltage reference for better accuracy on low voltage inputs
- Individual enable and disable of each channel
- Multiple trigger sources
 - Hardware or software trigger
 - External trigger pin
 - Timer Counter 0 to 2 outputs TIOA0 to TIOA2 trigger
- Sleep Mode and conversion sequencer
 - Automatic wakeup on trigger and back to sleep mode after conversions of all enabled channels
- Each analog input shared with digital signals

Figure 11-2. 144-ball LFBGA Package Drawing



All dimensions are in mm

12. Ordering Information

Table 12-1. Ordering Information

Ordering Code	MRL	Package	Package Type	Temperature Operating Range
AT91SAM7SE512B-AU	B	LQFP128	Green	Industrial (-40° C to 85° C)
AT91SAM7SE256B-AU	B	LQFP128	Green	Industrial (-40° C to 85° C)
AT91SAM7SE32B-AU	B	LQFP128	Green	Industrial (-40° C to 85° C)
AT91SAM7SE512B-CU	B	LFBGA144	Green	Industrial (-40° C to 85° C)
AT91SAM7SE256B-CU	B	LFBGA144	Green	Industrial (-40° C to 85° C)
AT91SAM7SE32B-CU	B	LFBGA144	Green	Industrial (-40° C to 85° C)
AT91SAM7SE512-AU	A	LQFP128	Green	Industrial (-40° C to 85° C)
AT91SAM7SE256-AU	A	LQFP128	Green	Industrial (-40° C to 85° C)
AT91SAM7SE32-AU	A	LQFP128	Green	Industrial (-40° C to 85° C)
AT91SAM7SE512-CU	A	LFBGA144	Green	Industrial (-40° C to 85° C)
AT91SAM7SE256-CU	A	LFBGA144	Green	Industrial (-40° C to 85° C)
AT91SAM7SE32-CU	A	LFBGA144	Green	Industrial (-40° C to 85° C)

Revision History

Doc. Rev	Comments	Change Request Ref.
	First issue	
6222AS	Revised Memories with condensed mapping. Added Package Outlines and 144-ball LFBGA pin and ordering information.	#2709
6222BS	Section 12. "Ordering Information" on page 45 ordering information code reference changed	#3699
6222CS	Section 6.1 "JTAG Port Pins" , Section 6.3 "Reset Pin" , Section 6.5 "SDCK Pin" , removed statement: "not 5V tolerant" Section 7.6 "SDRAM Controller" , Mobile SDRAM controller added to SDRAMC features INL and DNL updated in Section 10.14 "Analog-to-Digital Converter" "Features" on page 2, Fully Static Operation; added, up to 55 MHz at 1.8V and 85°C worst case conditions Section 7.1 "ARM7TDMI Processor" , Runs at up to 55 MHz, providing 0.9 MIPS/MHz (core supplied with 1.8V) Section 7.8 "Peripheral DMA Controller" PDC priority list added Section 7.5 "Static Memory Controller" , Multiple device adaptability includes: compliant w/PSRAM in synchronous operations.	#3826 #4005 #3924 #3833 review
6222DS	Figure 8-1 "SAM7SE Memory Mapping" Compact Flash not shown w/EBI Chip Select 5. Compact Flash is shown with EBI Chip Select 2. Section 8.1.2.1 "Flash Overview" , updated AT91SAM7SE32 ..."reads as 8192 32-bit words." Section 6. "I/O Lines Considerations" , "JTAG Port Pins" , "Test Pin" , "Reset Pin" , "ERASE Pin" descriptions updated	4804 4512 5062
6222ES	Section 10.11 "Timer Counter" ,the TC has two output compare and one input capture per channel.	4209
6222FS	Features: "Mode for General Purpose Two-wire UART Serial Communication" added to "Debug Unit (DBGU)" . Signal Description: Table 3-1, "Signal Description List" , AD0-AD3 and AD4-AD7 comments reversed. System Controller: Figure 9-1 "System Controller Block Diagram" , 'periph_nreset' changed into 'power_on_reset' for RTT.	5846 5271 5222
6222GS	MRL B Ordering Codes added to Table 12-1, "Ordering Information" 'Product Description' changed to 'AT91SAM ARM-based Flash MCU' on the first page. 'AT91SAM' product prefix changed to 'SAM', except for Chip ID and ordering codes.	7749 rfo



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