Microchip Technology - AT91SAM7SE512B-CU Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	55MHz
Connectivity	EBI/EMI, I²C, SPI, SSC, UART/USART, USB
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	88
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 1.95V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LFBGA
Supplier Device Package	144-LFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at91sam7se512b-cu

- Provides Reset or Interrupt Signals to the System
- Counter May Be Stopped While the Processor is in Debug State or in Idle Mode

- Real-time Timer (RTT)
  - 32-bit Free-running Counter with Alarm
  - Runs Off the Internal RC Oscillator
- Three Parallel Input/Output Controllers (PIO)
  - Eighty-eight Programmable I/O Lines Multiplexed with up to Two Peripheral I/Os
  - Input Change Interrupt Capability on Each I/O Line
  - Individually Programmable Open-drain, Pull-up Resistor and Synchronous Output
  - Schmitt Trigger on All inputs
- Eleven Peripheral DMA Controller (PDC) Channels
- One USB 2.0 Full Speed (12 Mbits per second) Device Port
  - On-chip Transceiver, Eight Endpoints, 2688-byte Configurable Integrated FIFOs
- One Synchronous Serial Controller (SSC)
  - Independent Clock and Frame Sync Signals for Each Receiver and Transmitter
  - I^2S Analog Interface Support, Time Division Multiplex Support
  - High-speed Continuous Data Stream Capabilities with 32-bit Data Transfer
- Two Universal Synchronous/Asynchronous Receiver Transmitters (USART)
  - Individual Baud Rate Generator, IrDA® Infrared Modulation/Demodulation
  - Support for ISO7816 T0/T1 Smart Card, Hardware Handshaking, RS485 Support
  - Full Modem Line Support on USART1
- One Master/Slave Serial Peripheral Interfaces (SPI)
  - 8- to 16-bit Programmable Data Length, Four External Peripheral Chip Selects
- One Three-channel 16-bit Timer/Counter (TC)
  - Three External Clock Inputs, Two Multi-purpose I/O Pins per Channel
  - Double PWM Generation, Capture/Waveform Mode, Up/Down Capability
- One Four-channel 16-bit PWM Controller (PWMC)
- One Two-wire Interface (TWI)
  - Master, Multi-Master and Slave Mode Support, All Two-wire Atmel EEPROMs Supported
  - General Call Supported in Slave Mode
- One 8-channel 10-bit Analog-to-Digital Converter, Four Channels Multiplexed with Digital I/Os
- SAM-BA®
  - Default Boot program
  - Interface with SAM-BA Graphic User Interface
- IEEE® 1149.1 JTAG Boundary Scan on All Digital Pins
- Four High-current Drive I/O lines, Up to 16 mA Each
- Power Supplies
  - Embedded 1.8V Regulator, Drawing up to 100 mA for the Core and External Components
  - 1.8V or 3,3V VDDIO I/O Lines Power Supply, Independent 3.3V VDDFLASH Flash Power Supply
  - 1.8V VDDCORE Core Power Supply with Brownout Detector
- Fully Static Operation:
  - Up to 55 MHz at 1.8V and 85° C Worst Case Conditions
  - Up to 48 MHz at 1.65V and 85° C Worst Case Conditions
- Available in a 128-lead LQFP Green Package, or a 144-ball LFBGA RoHS-compliant Package

4. Package

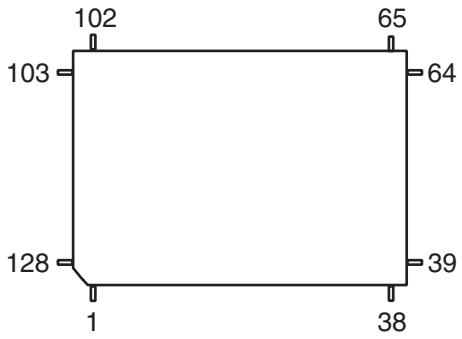
The SAM7SE512/256/32 is available in:

- 20 x 14 mm 128-lead LQFP package with a 0.5 mm lead pitch.
- 10x 10 x 1.4 mm 144-ball LFBGA package with a 0.8 mm lead pitch

4.1 128-lead LQFP Package Outline

Figure 4-1 shows the orientation of the 128-lead LQFP package and a detailed mechanical description is given in the Mechanical Characteristics section of the full datasheet.

Figure 4-1. 128-lead LQFP Package Outline (Top View)



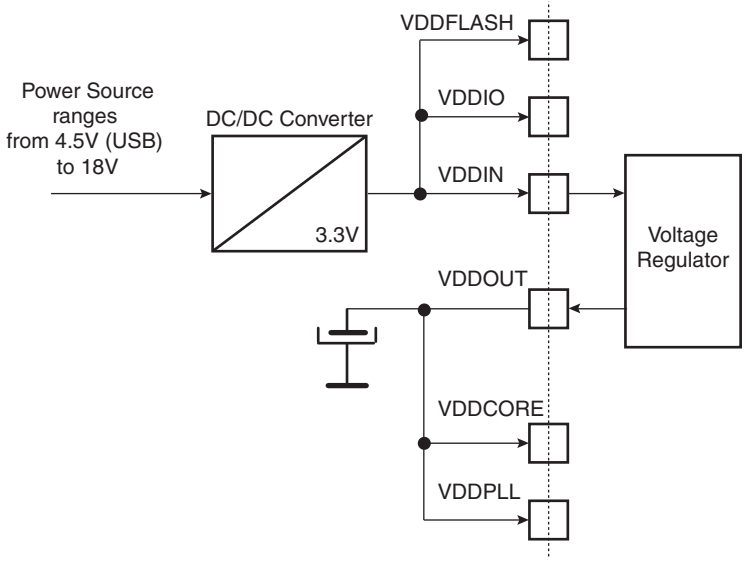
- One external 2.2 µF (or 3.3 µF) X7R capacitor should be connected between VDDOUT and GND.

Adequate input supply decoupling is mandatory for VDDIN in order to improve startup stability and reduce source voltage drop. The input decoupling capacitor should be placed close to the chip. For example, two capacitors can be used in parallel: 100 nF NPO and 4.7 µF X7R.

5.4 Typical Powering Schematics

The SAM7SE512/256/32 supports a 3.3V single supply mode. The internal regulator input connected to the 3.3V source and its output feeds VDDCORE and the VDDPLL. Figure 5-1 shows the power schematics to be used for USB bus-powered systems.

Figure 5-1. 3.3V System Single Power Supply Schematic



6. /O Lines Considerations

6.1 JTAG Port Pins

TMS, TDI and TCK are Schmitt trigger inputs. TMS, TDI and TCK do not integrate a pull-up resistor.

TDO is an output, driven at up to VDDIO, and has no pull-up resistor.

The JTAGSEL pin is used to select the JTAG boundary scan when asserted at a high level. The JTAGSEL pin integrates a permanent pull-down resistor of about 15 kΩ.

To eliminate any risk of spuriously entering the JTAG boundary scan mode due to noise on JTAGSEL, it should be tied externally to GND if boundary scan is not used, or put in place an external low value resistor (such as 1 kΩ).

6.2 Test Pin

The TST pin is used for manufacturing test or fast programming mode of the SAM7SE512/256/32 when asserted high. The TST pin integrates a permanent pull-down resistor of about 15 kΩ to GND.

To eliminate any risk of entering the test mode due to noise on the TST pin, it should be tied to GND if the FFPI is not used, or put in place an external low value resistor (such as 1 kΩ).

To enter fast programming mode, the TST pin and the PA0 and PA1 pins should be tied high and PA2 tied low.

Driving the TST pin at a high level while PA0 or PA1 is driven at 0 leads to unpredictable results.

6.3 Reset Pin

The NRST pin is bidirectional with an open-drain output buffer. It is handled by the on-chip reset controller and can be driven low to provide a reset signal to the external components or asserted low externally to reset the microcontroller. There is no constraint on the length of the reset pulse, and the reset controller can guarantee a minimum pulse length. This allows connection of a simple push-button on the NRST pin as system user reset, and the use of the NRST signal to reset all the components of the system.

An external power-on reset can drive this pin during the start-up instead of using the internal power-on reset circuit.

The NRST pin integrates a permanent pull-up of about 100 kΩ resistor to VDDIO.

This pin has Schmitt trigger input.

6.4 ERASE Pin

The ERASE pin is used to re-initialize the Flash content and some of its NVM bits. It integrates a permanent pull-down resistor of about 15 kΩ to GND.

To eliminate any risk of erasing the Flash due to noise on the ERASE pin, it should be tied externally to GND, which prevents erasing the Flash from the application, or put in place an external low value resistor (such as 1 kΩ).

This pin is debounced by the RC oscillator to improve the glitch tolerance. When the pin is tied to high during less than 100 ms, ERASE pin is not taken into account. The pin must be tied high during more than 220 ms to perform the re-initialization of the Flash.

7. Processor and Architecture

7.1 ARM7TDMI Processor

- RISC processor based on ARMv4T Von Neumann architecture
  - Runs at up to 55 MHz, providing 0.9 MIPS/MHz (core supplied with 1.8V)
- Two instruction sets
  - ARM® high-performance 32-bit instruction set
  - Thumb® high code density 16-bit instruction set
- Three-stage pipeline architecture
  - Instruction Fetch (F)
  - Instruction Decode (D)
  - Execute (E)

7.2 Debug and Test Features

- EmbeddedICE™ (Integrated embedded in-circuit emulator)
  - Two watchpoint units
  - Test access port accessible through a JTAG protocol
  - Debug communication channel
- Debug Unit
  - Two-pin UART
  - Debug communication channel interrupt handling
  - Chip ID Register
- IEEE1149.1 JTAG Boundary-scan on all digital pins

7.3 Memory Controller

- Programmable Bus Arbiter
  - Handles requests from the ARM7TDMI and the Peripheral DMA Controller
- Address decoder provides selection signals for
  - Four internal 1 Mbyte memory areas
  - One 256-Mbyte embedded peripheral area
  - Eight external 256-Mbyte memory areas
- Abort Status Registers
  - Source, Type and all parameters of the access leading to an abort are saved
  - Facilitates debug by detection of bad pointers
- Misalignment Detector
  - Alignment checking of all data accesses
  - Abort generation in case of misalignment
- Remap Command
  - Remaps the SRAM in place of the embedded non-volatile memory
  - Allows handling of dynamic exception vectors
- 16-area Memory Protection Unit (Internal Memory and peripheral protection only)

- Multiple device adaptability
  - Compliant with LCD Module
  - Compliant with PSRAM in synchronous operations
  - Programmable Setup Time Read/Write
  - Programmable Hold Time Read/Write
- Multiple Wait State Management
  - Programmable Wait State Generation
  - External Wait Request
  - Programmable Data Float Time

7.6 SDRAM Controller

- Numerous configurations supported
  - **2K, 4K, 8K Row Address Memory Parts**
  - **SDRAM with two or four Internal Banks**
  - **SDRAM with 16- or 32-bit Data Path**
- Programming facilities
  - **Word, half-word, byte access**
  - **Automatic page break when Memory Boundary has been reached**
  - **Multibank Ping-pong Access**
  - **Timing parameters specified by software**
  - **Automatic refresh operation, refresh rate is programmable**
- **Energy-saving capabilities**
  - **Self-refresh, and Low-power Modes supported**
- Error detection
  - **Refresh Error Interrupt**
- **SDRAM Power-up Initialization by software**
- **Latency is set to two clocks (CAS Latency of 1, 3 Not Supported)**
- **Auto Precharge Command not used**
- Mobile SDRAM supported (except for low-power extended mode and deep power-down mode)

7.7 Error Corrected Code Controller

- Tracking the accesses to a NAND Flash device by triggering on the corresponding chip select
- Single bit error correction and 2-bit Random detection.
- Automatic Hamming Code Calculation while writing
  - ECC value available in a register
- Automatic Hamming Code Calculation while reading
  - Error Report, including error flag, correctable error flag and word address being detected erroneous
  - Supports 8- or 16-bit NAND Flash devices with 512-, 1024-, 2048- or 4096-byte pages

7.8 Peripheral DMA Controller

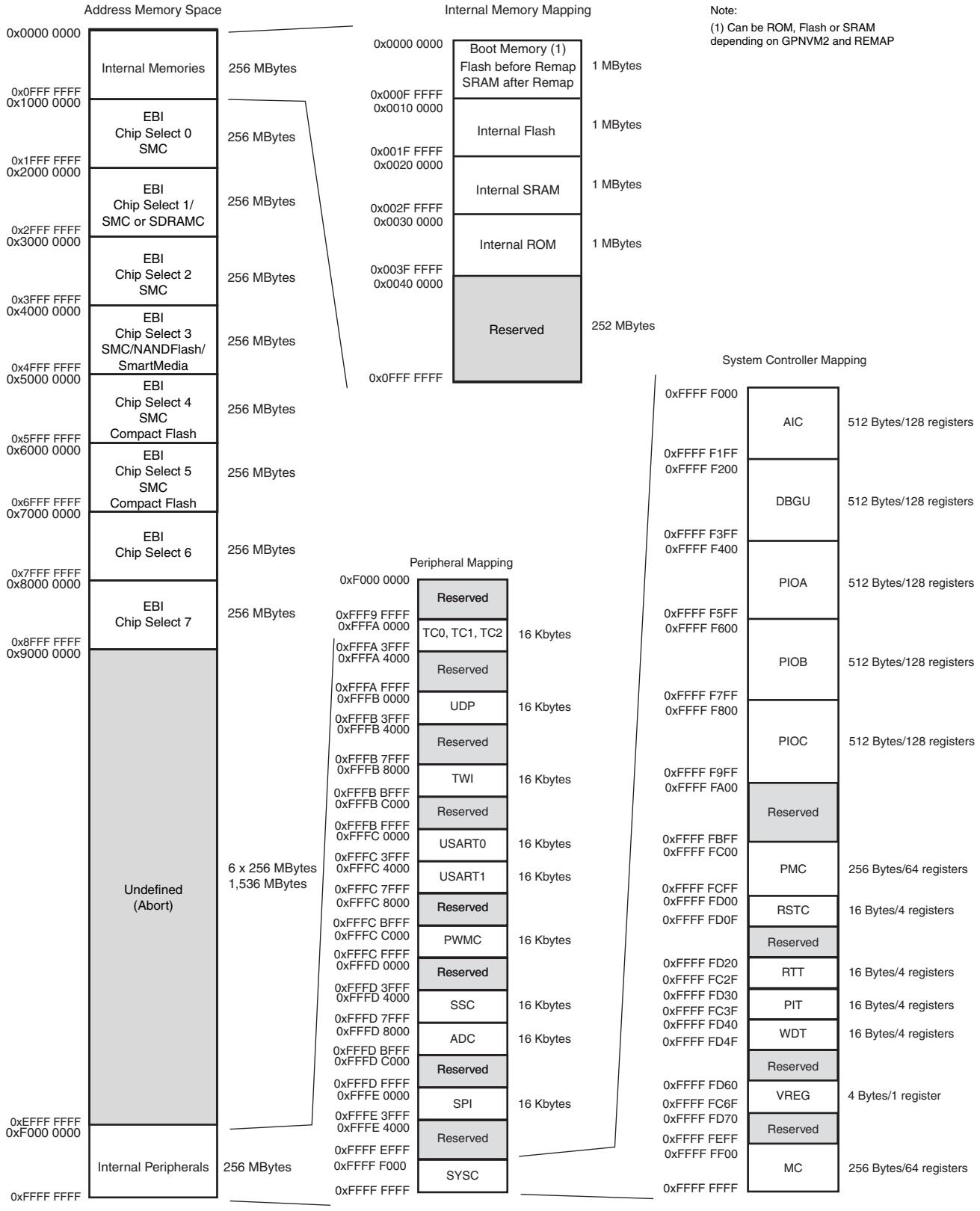
- Handles data transfer between peripherals and memories
- Eleven channels
  - Two for each USART
  - Two for the Debug Unit
  - Two for the Serial Synchronous Controller
  - Two for the Serial Peripheral Interface
  - One for the Analog-to-digital Converter
- Low bus arbitration overhead
  - One Master Clock cycle needed for a transfer from memory to peripheral
  - Two Master Clock cycles needed for a transfer from peripheral to memory
- Next Pointer management for reducing interrupt latency requirements
- Peripheral DMA Controller (PDC) priority is as follows (from the highest priority to the lowest):

Receive	DBGU
Receive	USART0
Receive	USART1
Receive	SSC
Receive	ADC
Receive	SPI
Transmit	DBGU
Transmit	USART0
Transmit	USART1
Transmit	SSC
Transmit	SPI

8. Memories

- 512 Kbytes of Flash Memory (SAM7SE512)
  - dual plane
  - two contiguous banks of 1024 pages of 256 bytes
  - Fast access time, 30 MHz single-cycle access in Worst Case conditions
  - Page programming time: 6 ms, including page auto-erase
  - Page programming without auto-erase: 3 ms
  - Full chip erase time: 15 ms
  - 10,000 write cycles, 10-year data retention capability
  - 32 lock bits, each protecting 32 lock regions of 64 pages
  - Protection Mode to secure contents of the Flash
- 256 Kbytes of Flash Memory (SAM7SE256)
  - single plane
  - one bank of 1024 pages of 256 bytes
  - Fast access time, 30 MHz single-cycle access in Worst Case conditions
  - Page programming time: 6 ms, including page auto-erase
  - Page programming without auto-erase: 3 ms
  - Full chip erase time: 15 ms
  - 10,000 cycles, 10-year data retention capability
  - 16 lock bits, each protecting 16 lock regions of 64 pages
  - Protection Mode to secure contents of the Flash
- 32 Kbytes of Flash Memory (SAM7SE32)
  - single plane
  - one bank of 256 pages of 128 bytes
  - Fast access time, 30 MHz single-cycle access in Worst Case conditions
  - Page programming time: 6 ms, including page auto-erase
  - Page programming without auto-erase: 3 ms
  - Full chip erase time: 15 ms
  - 10,000 cycles, 10-year data retention capability
  - 8 lock bits, each protecting 8 lock regions of 32 pages
  - Protection Mode to secure contents of the Flash
- 32 Kbytes of Fast SRAM (SAM7SE512/256)
  - Single-cycle access at full speed
- 8 Kbytes of Fast SRAM (SAM7SE32)
  - Single-cycle access at full speed

Figure 8-1. SAM7SE Memory Mapping



A first level of address decoding is performed by the Memory Controller, i.e., by the implementation of the Advanced System Bus (ASB) with additional features.

Decoding splits the 4G bytes of address space into 16 areas of 256M bytes. The areas 1 to 8 are directed to the EBI that associates these areas to the external chip selects NC0 to NCS7. The area 0 is reserved for the addressing of the internal memories, and a second level of decoding provides 1M byte of internal memory area. The area 15 is reserved for the peripherals and provides access to the Advanced Peripheral Bus (APB).

Other areas are unused and performing an access within them provides an abort to the master requesting such an access.

8.1 Embedded Memories

8.1.1 Internal Memories

8.1.1.1 Internal SRAM

The SAM7SE512/256 embeds a high-speed 32-Kbyte SRAM bank. The SAM7SE32 embeds a high-speed 8-Kbyte SRAM bank. After reset and until the Remap Command is performed, the SRAM is only accessible at address 0x0020 0000. After Remap, the SRAM also becomes available at address 0x0.

8.1.1.2 Internal ROM

The SAM7SE512/256/32 embeds an Internal ROM. At any time, the ROM is mapped at address 0x30 0000. The ROM contains the FFPI and the SAM-BA boot program.

8.1.1.3 Internal Flash

- The SAM7SE512 features two banks of 256 Kbytes of Flash.
- The SAM7SE256 features one bank of 256 Kbytes of Flash.
- The SAM7SE32 features one bank of 32 Kbytes of Flash.

At any time, the Flash is mapped to address 0x0010 0000.

A general purpose NVM (GPNVM) bit is used to boot either on the ROM (default) or from the Flash.

This GPNVM bit can be cleared or set respectively through the commands “Clear General-purpose NVM Bit” and “Set General-purpose NVM Bit” of the EFC User Interface.

Setting the GPNVM bit 2 selects the boot from the Flash, clearing it selects the boot from the ROM. Asserting ERASE clears the GPNVM bit 2 and thus selects the boot from the ROM by default.

Figure 8-2. Internal Memory Mapping with GPNVM Bit 2 = 0 (default)

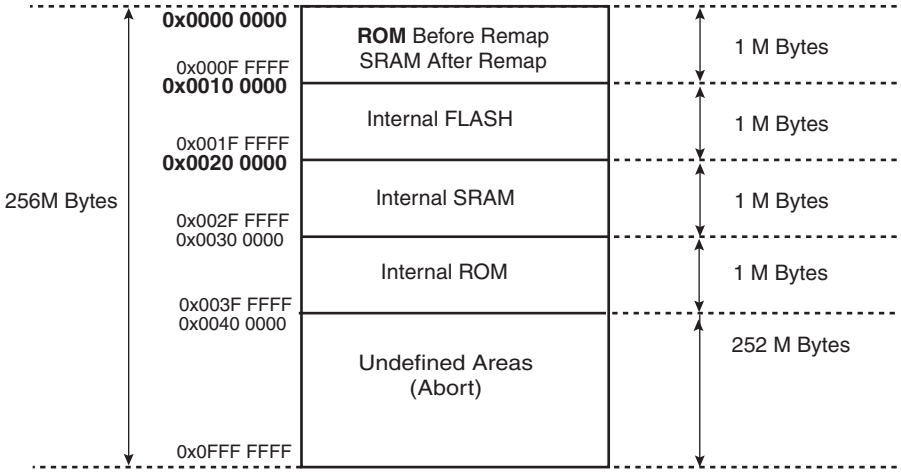
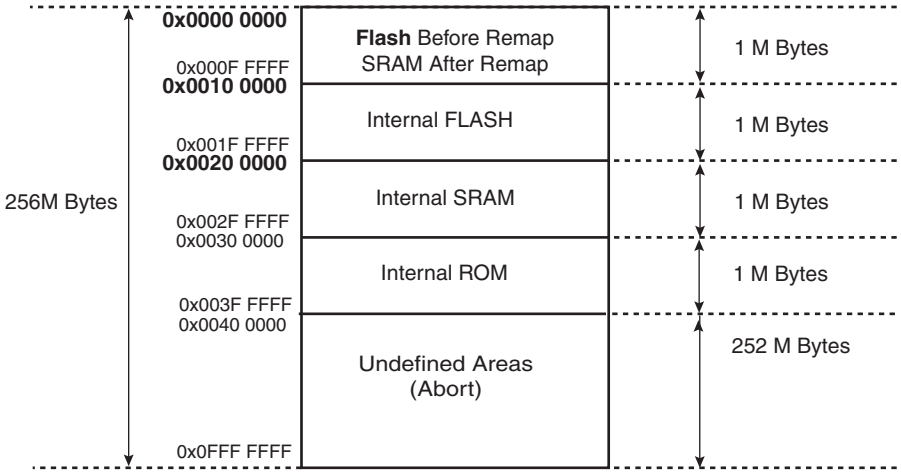


Figure 8-3. Internal Memory Mapping with GPNVM Bit 2 = 1



8.1.2 Embedded Flash

8.1.2.1 Flash Overview

The Flash of the SAM7SE512 is organized in two banks (dual plane) of 1024 pages of 256 bytes. It reads as 131,072 32-bit words.

The Flash of the SAM7SE256 is organized in 1024 pages (single plane) of 256 bytes. It reads as 65,536 32-bit words.

The Flash of the SAM7SE32 is organized in 256 pages (single plane) of 128 bytes. It reads as 8192 32-bit words.

The Flash of the SAM7SE32 contains a 128-byte write buffer, accessible through a 32-bit interface.

The Flash of the SAM7SE512/256 contains a 256-byte write buffer, accessible through a 32-bit interface.

9. System Controller

The System Controller manages all vital blocks of the microcontroller: interrupts, clocks, power, time, debug and reset.

The System Controller peripherals are all mapped to the highest 4 Kbytes of address space, between addresses 0xFFFF F000 and 0xFFFF FFFF.

Figure 9-1 on page 29 shows the System Controller Block Diagram.

Figure 8-1 on page 22 shows the mapping of the User Interface of the System Controller peripherals. Note that the Memory Controller configuration user interface is also mapped within this address space.

- Synchronous output, provides Set and Clear of several I/O lines in a single write

9.10 Voltage Regulator Controller

The purpose of this controller is to select the Power Mode of the Voltage Regulator between Normal Mode (bit 0 is cleared) or Standby Mode (bit 0 is set).

10. Peripherals

10.1 User Interface

The User Peripherals are mapped in the 256 MBytes of the address space between 0xF000 0000 and 0xFFFF EFFF. Each peripheral is allocated 16 Kbytes of address space.

A complete memory map is presented in Figure 8-1 on page 22.

10.2 Peripheral Identifiers

The SAM7SE512/256/32 embeds a wide range of peripherals. Table 10-1 defines the Peripheral Identifiers of the SAM7SE512/256/32. Unique peripheral identifiers are defined for both the Advanced Interrupt Controller and the Power Management Controller.

Table 10-1. Peripheral Identifiers

Peripheral ID	Peripheral Mnemonic	Peripheral Name	External Interrupt
0	AIC	Advanced Interrupt Controller	FIQ
1	SYSC[1]		
2	PIOA	Parallel I/O Controller A	
3	PIOB	Parallel I/O Controller B	
4	PIOC	Parallel I/O Controller C	
5	SPI	Serial Peripheral Interface 0	
6	US0	USART 0	
7	US1	USART 1	
8	SSC	Synchronous Serial Controller	
9	TWI	Two-wire Interface	
10	PWMC	PWM Controller	
11	UDP	USB Device Port	
12	TC0	Timer/Counter 0	
13	TC1	Timer/Counter 1	
14	TC2	Timer/Counter 2	
15	ADC[1]	Analog-to Digital Converter	
16-28	reserved		
29	AIC	Advanced Interrupt Controller	IRQ0
30	AIC	Advanced Interrupt Controller	IRQ1

Note: 1. Setting SYSC and ADC bits in the clock set/clear registers of the PMC has no effect. The System Controller is continuously clocked. The ADC clock is automatically started for the first conversion. In Sleep Mode the ADC clock is automatically stopped after each conversion.

10.4 PIO Controller A Multiplexing

Table 10-2. Multiplexing on PIO Controller A

PIO Controller A				Application Usage	
I/O Line	**Peripheral A**	**Peripheral B**	**Comments**	**Function**	**Comments**
PA0	PWM0	A0/NBS0	High-Drive		
PA1	PWM1	A1/NBS2	High-Drive		
PA2	PWM2	A2	High-Drive		
PA3	TWD	A3	High-Drive		
PA4	TWCK	A4			
PA5	RXD0	A5			
PA6	TXD0	A6			
PA7	RTS0	A7			
PA8	CTS0	A8			
PA9	DRXD	A9			
PA10	DTXD	A10			
PA11	NPCS0	A11			
PA12	MISO	A12			
PA13	MOSI	A13			
PA14	SPCK	A14			
PA15	TF	A15			
PA16	TK	A16/BA0			
PA17	TD	A17/BA1	AD0		
PA18	RD	NBS3/CFIOW	AD1		
PA19	RK	NCS4/CFCS0	AD2		
PA20	RF	NCS2/CFCS1	AD3		
PA21	RXD1	NCS6/CFCE2			
PA22	TXD1	NCS5/CFCE1			
PA23	SCK1	NWR1/NBS1/CFIOR			
PA24	RTS1	SDA10			
PA25	CTS1	SDCKE			
PA26	DCD1	NCS1/SDCS			
PA27	DTR1	SDWE			
PA28	DSR1	CAS			
PA29	RI1	RAS			
PA30	IRQ1	D30			
PA31	NPCS1	D31			

10.6 PIO Controller C Multiplexing

Multiplexing on PIO Controller C

PIO Controller C				Application Usage	
I/O Line	Peripheral A	Peripheral B	Comments	Function	Comments
PC0	D0				
PC1	D1				
PC2	D2				
PC3	D3				
PC4	D4				
PC5	D5				
PC6	D6				
PC7	D7				
PC8	D8	RTS1			
PC9	D9	DTR1			
PC10	D10	PCK0			
PC11	D11	PCK1			
PC12	D12	PCK2			
PC13	D13				
PC14	D14	NPCS1			
PC15	D15	NCS3/NANDCS			
PC16	A18	NWAIT			
PC17	A19	NANDOE			
PC18	A20	NANDWE			
PC19	A21/NANDALE				
PC20	A22/REG/NANDCLE	NCS7			
PC21		NWR0/NWE/CFWE			
PC22		NRD/CFOE			
PC23	CFRNW	NCS0			

10.7 Serial Peripheral Interface

- Supports communication with external serial devices
  - Four chip selects with external decoder allow communication with up to 15 peripherals
  - Serial memories, such as DataFlash® and 3-wire EEPROMs
  - Serial peripherals, such as ADCs, DACs, LCD Controllers, CAN Controllers and Sensors
  - External co-processors
- Master or slave serial peripheral bus interface

- 8- to 16-bit programmable data length per chip select
- Programmable phase and polarity per chip select
- Programmable transfer delays per chip select, between consecutive transfers and between clock and data
- Programmable delay between consecutive transfers
- Selectable mode fault detection
- Maximum frequency at up to Master Clock

10.8 Two Wire Interface

- Master, Multi-Master and Slave Mode Operation
- Compatibility with standard two-wire serial memories
- One, two or three bytes for slave address
- Sequential read/write operations
- Bit Rate: Up to 400 Kbit/s
- General Call Supported in Slave Mode

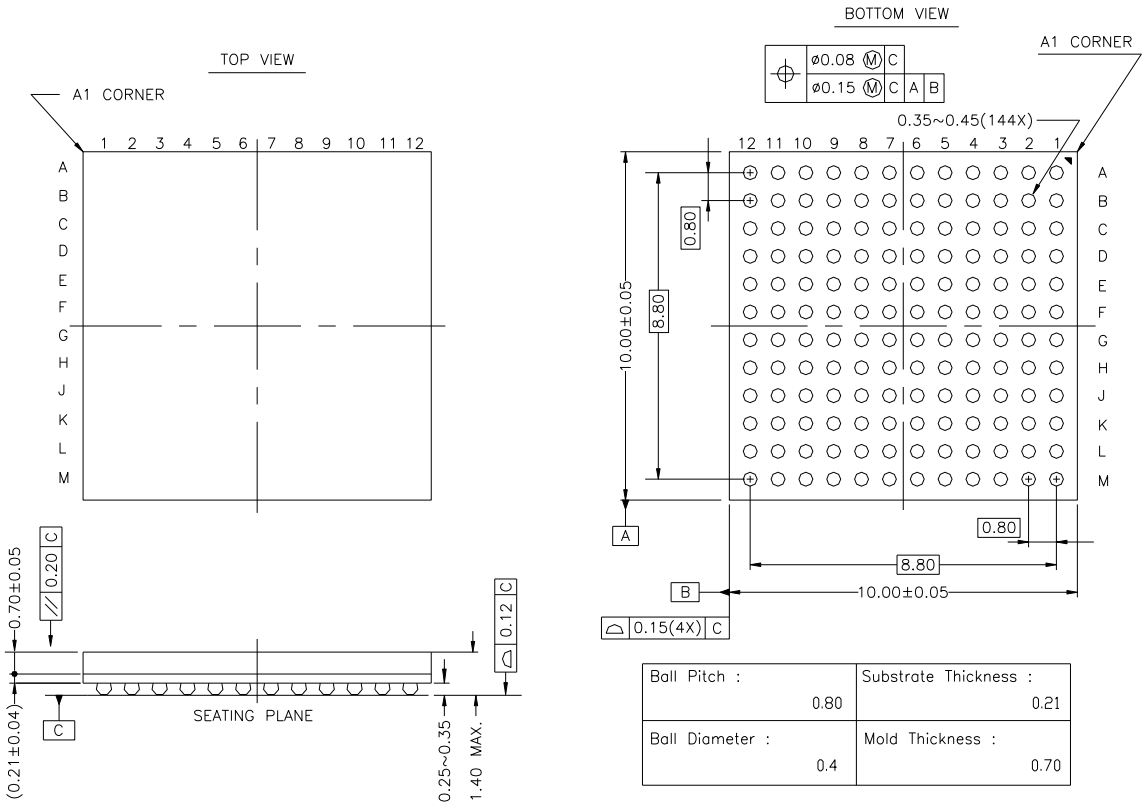
10.9 USART

- Programmable Baud Rate Generator
- 5- to 9-bit full-duplex synchronous or asynchronous serial communications
  - 1, 1.5 or 2 stop bits in Asynchronous Mode
  - 1 or 2 stop bits in Synchronous Mode
  - Parity generation and error detection
  - Framing error detection, overrun error detection
  - MSB or LSB first
  - Optional break generation and detection
  - By 8 or by 16 over-sampling receiver frequency
  - Hardware handshaking RTS - CTS
  - Modem Signals Management DTR-DSR-DCD-RI on USART1
  - Receiver time-out and transmitter timeguard
  - Multi-drop Mode with address generation and detection
- RS485 with driver control signal
- ISO7816, T = 0 or T = 1 Protocols for interfacing with smart cards
  - NACK handling, error counter with repetition and iteration limit
- IrDA® modulation and demodulation
  - Communication at up to 115.2 Kbps
- Test Modes
  - Remote Loopback, Local Loopback, Automatic Echo

10.10 Serial Synchronous Controller

- Provides serial synchronous communication links used in audio and telecom applications
- Contains an independent receiver and transmitter and a common clock divider

Figure 11-2. 144-ball LFBGA Package Drawing



All dimensions are in mm

12. Ordering Information

Table 12-1. Ordering Information

Ordering Code	MRL	Package	Package Type	Temperature Operating Range
AT91SAM7SE512B-AU	B	LQFP128	Green	Industrial (-40· C to 85· C)
AT91SAM7SE256B-AU	B	LQFP128	Green	Industrial (-40· C to 85· C)
AT91SAM7SE32B-AU	B	LQFP128	Green	Industrial (-40· C to 85· C)
AT91SAM7SE512B-CU	B	LFBGA144	Green	Industrial (-40· C to 85· C)
AT91SAM7SE256B-CU	B	LFBGA144	Green	Industrial (-40· C to 85· C)
AT91SAM7SE32B-CU	B	LFBGA144	Green	Industrial (-40· C to 85· C)
AT91SAM7SE512-AU	A	LQFP128	Green	Industrial (-40· C to 85· C)
AT91SAM7SE256-AU	A	LQFP128	Green	Industrial (-40· C to 85· C)
AT91SAM7SE32-AU	A	LQFP128	Green	Industrial (-40· C to 85· C)
AT91SAM7SE512-CU	A	LFBGA144	Green	Industrial (-40· C to 85· C)
AT91SAM7SE256-CU	A	LFBGA144	Green	Industrial (-40· C to 85· C)
AT91SAM7SE32-CU	A	LFBGA144	Green	Industrial (-40· C to 85· C)

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