Infineon Technologies - S6E2DF5G0AGE20000 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	160MHz
Connectivity	CSIO, EBI/EMI, I²C, LINbus, SD, SPI, UART/USART, USB
Peripherals	DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	98
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	36K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 24x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	120-LQFP
Supplier Device Package	120-LQFP (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e2df5g0age20000

1. Product Lineup

Memory Size

Product Name		S6E2D55G0A S6E2D55J0A	S6E2D55GJA
On-chip Flash memory		384 Kbytes	
On-chip SRAM	SRAM	36 Kbytes	
	SRAM0	32 Kbytes	
	SRAM2	4 Kbytes	
VRAM for GDC		512 Kbytes	
VFLASH for GDC		-	2 Mbytes

Function

Product Name			S6E2D55G0A	S6E2D55J0A	S6E2D55GJA
Pin count			120/161	176	120
CPU			Cortex-M4F, MPU, NVIC 128ch.		
		Freq.	160 MHz		
Power supply voltage range			2.7 V to 3.6 V		
USB2.0 (Device/Host)			1ch.		
CAN-FD (non-ISO CAN FD)			1ch.		
DMAC			8ch.		
DSTC			128ch.		
GDC unit	Graphics・Display controller		1 unit		
	High-Speed Quad SPI		1ch.		(VFLASH only)
	Hyper Bus Interface		1 unit		-
	SDRAM-IF		-	1ch.	-
External Bus Interface			Addr:25-bit (Max), Data: 8-/16-bit, CS:2 (Max) SRAM, NOR Flash, NAND Flash, SDRAM		
Multi-function Serial Interface (UART/CSIO/LIN/I^{2}C)			8ch. (Max)		
Base Timer (PWC/Reload timer/PWM/PPG)			8ch. (Max)		
MF Timer	A/D activation compare	6ch.	1 unit		
	Input capture	4ch.			
	Free-run timer	3ch.			
	Output compare	6ch.			
	Waveform generator	3ch.			
	PPG	3ch.			
I^{2}S			2 units		
QPRC			1ch.		
Dual Timer			1 unit		
Real-Time Clock			1 unit		
Watch Counter			1 unit		
CRC Accelerator			Yes(Fixed, Programmable)		
Watchdog Timer			1ch. (SW) + 1ch. (HW)		
External Interrupts			16 pins (Max)+ NMI × 1		
I/O ports			98 pins (Max)	154 pins (Max)	90 pins (Max)
12-bit A/D converter			24ch. (2 units)		
CSV (Clock Super Visor)			Yes		
LVD (Low-Voltage Detector)			2ch.		
Built-in CR		High-speed	4 MHz		
		Low-speed	100 kHz		
Debug Function			SWJ-DP/ETM		
Unique ID			Yes		

Pin No.				Pin name	I/O circuit type	Pin state type
LQFP176	LQFP120 Ex-LQFP120	LQFP120 (S6E2D55GJA)	FBGA161			
51	33	33	M3	P21 I2SMCLK1_0 MAD05_0	E	I
52	34	34	L4	P22 CROUT_0 SIN0_0 INT08_0 I2SDO1_0 MAD04_0	E	K
53	35	35	M4	P23 SOT0_0 (SDA0_0) TIOA6_1 I2SWS1_0 MAD03_0	E	I
54	36	36	K5	P24 SCK0_0 (SCL0_0) TIOB6_1 I2SDI1_0 MAD02_0	E	I
55	37	37	L5	P25 I2SCK1_0 MAD01_0	E	I
56	—	—	—	PB4 GE_SDDQ15	L	I
57	—	—	—	PB5 GE_SDDQ14	L	I
58	—	—	—	PB6 GE_SDDQ13	L	I
59	—	—	—	PB7 GE_SDDQ12	L	I
60	38	38	N2	C	—	—
61	39	39	N3	VSS	—	—
62	40	40	N4	VCC	—	—
63	41	41	M5	P26 RTCCO_1 SUBOUT_1 MAD00_0	E	I
64	42	42	N5	P27 ADTG_1 CROUT_1 MRDY_0	E	I

Pin No.				Pin name	I/O circuit type	Pin state type
LQFP176	LQFP120 Ex-LQFP120	LQFP120 (S6E2D55GJA)	FBGA161			
101	67	67	J11	P11 AN01 SOT1_0 (SDA1_0) TIOB0_0 BIN0_0 MADATA01_0	F	L
102	68	68	H10	P12 AN02 SCK1_0 (SCL1_0) TIOA1_0 ZIN0_0 MADATA02_0	F	L
103	69	69	H11	P13 AN03 SIN2_0 TIOB1_0 INT10_0 FRCK0_1 MADATA03_0	F	M
104	70	70	H12	P14 AN04 SOT2_0 (SDA2_0) TIOA2_0 DTTI0X_1 MADATA04_0	F	L
105	71	71	H13	P15 AN05 SCK2_0 (SCL2_0) TIOB2_0 INT11_0 IC00_1 MADATA05_0	F	M
106	72	72	G10	P16 AN06 SIN3_0 TIOA3_0 INT12_0 IC01_1 MADATA06_0	F	M

Pin No.				Pin name	I/O circuit type	Pin state type
LQFP176	LQFP120 Ex-LQFP120	LQFP120 (S6E2D55GJA)	FBGA161			
107	73	73	G11	P17 AN07 SOT3_0 (SDA3_0) TIOB3_0 IC02_1 MADATA07_0	F	L
108	74	74	G12	P18 AN08 SCK3_0 (SCL3_0) TIOA4_0 IC03_1 MADATA08_0	F	L
109	75	75	G13	P19 AN09 SIN5_0 TIOB4_0 INT13_0 AIN0_2 RTO00_1 (PPG00_1) MADATA09_0	F	M
110	76	76	F10	P1A AN10 SOT5_0 (SDA5_0) TIOA5_0 BIN0_2 RTO01_1 (PPG00_1) MADATA10_0	F	L
111	77	77	F11	P1B AN11 SCK5_0 (SCL5_0) TIOB5_0 ZIN0_2 RTO02_1 (PPG02_1) MADATA11_0	F	L
112	–	–	–	PC6 GE_SDBA1	K	I

Module	Pin Name	Function	Pin No.			
			LQFP176	LQFP120 Ex-LQFP120	LQFP120 (S6E2D55GJA)	FBGA161
External Bus	MAD00_0	External bus interface address bus	63	41	41	M5
	MAD01_0		55	37	37	L5
	MAD02_0		54	36	36	K5
	MAD03_0		53	35	35	M4
	MAD04_0		52	34	34	L4
	MAD05_0		51	33	33	M3
	MAD06_0		10	6	6	D1
	MAD07_0		9	5	5	D2
	MAD08_0		8	4	4	D3
	MAD09_0		7	3	3	C2
	MAD10_0		6	2	2	C3
	MAD11_0		156	104	104	A8
	MAD12_0		155	103	103	B8
	MAD13_0		154	102	102	C8
	MAD14_0		153	101	101	A9
	MAD15_0		152	100	100	B9
	MAD16_0		151	99	99	C9
	MAD17_0		150	98	98	D9
	MAD18_0		149	97	97	C10
	MAD19_0		125	87	87	D13
	MAD20_0		124	86	86	D12
	MAD21_0		123	85	85	D11
	MAD22_0		122	84	84	D10
	MAD23_0		121	83	83	E13
	MAD24_0		141	94	94	C11
	MCSX0_0	External bus interface chip select output pin	65	43	43	K7
	MCSX8_0		158	106	106	B7
	MADATA00_0	External bus interface data bus	100	66	66	K11
	MADATA01_0		101	67	67	J11
	MADATA02_0		102	68	68	H10
	MADATA03_0		103	69	69	H11
	MADATA04_0		104	70	70	H12
	MADATA05_0		105	71	71	H13
	MADATA06_0		106	72	72	G10
	MADATA07_0		107	73	73	G11
	MADATA08_0		108	74	74	G12
	MADATA09_0		109	75	75	G13
	MADATA10_0		110	76	76	F10
	MADATA11_0		111	77	77	F11
	MADATA12_0		116	78	78	F12
	MADATA13_0		117	79	79	F13
	MADATA14_0		118	80	80	E10
	MADATA15_0		119	81	81	E11

Module	Pin Name	Function	Pin No.			
			LQFP176	LQFP120 Ex-LQFP120	LQFP120 (S6E2D55GJA)	FBGA161
Multi-function serial 7	SIN7_0	Multi-function serial interface ch.7 input pin	8	4	4	D3
	SOT7_0 (SDA7_0)	Multi-function serial interface ch.7 output pin. This pin operates as SOT7 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA7 when it is used in an I^2C (operation mode 4).	9	5	5	D2
	SCK7_0 (SCL7_0)	Multi-function serial interface ch.7 clock I/O pin. This pin operates as SCK7 when it is used in a CSIO (operation mode 2) and as SCL7 when it is used in an I^2C (operation mode 4).	10	6	6	D1
	SCS70_0	Multi-function serial interface ch.7 chip select 0 input/output pin	7	3	3	C2
Multi-function Timer 0	DTTI0X_0	Input signal controlling wave form generator outputs RTO00 to RTO05 of Multi-function timer 0.	27	17	17	F1
	DTTI0X_1		104	70	70	H12
	FRCK0_0	16-bit free-run timer ch.0 external clock input pin	20	10	10	E2
	FRCK0_1		103	69	69	H11
	IC00_0	16-bit input capture input pin of Multi-function timer 0. ICxx describes channel number.	26	16	16	F2
	IC00_1		105	71	71	H13
	IC01_0		25	15	15	F3
	IC01_1		106	72	72	G10
	IC02_0		22	12	12	F4
	IC02_1		107	73	73	G11
	IC03_0		21	11	11	E1
	IC03_1		108	74	74	G12
	RTO00_0 (PPG00_0)	Wave form generator output pin of Multi-function timer 0. This pin operates as PPG00 when it is used in PPG0 output modes.	6	2	2	C3
	RTO00_1 (PPG00_1)		109	75	75	G13
	RTO01_0 (PPG00_0)	Wave form generator output pin of Multi-function timer 0. This pin operates as PPG00 when it is used in PPG0 output modes.	7	3	3	C2
	RTO01_1 (PPG00_1)		110	76	76	F10
	RTO02_0 (PPG02_0)	Wave form generator output pin of Multi-function timer 0. This pin operates as PPG02 when it is used in PPG0 output modes.	8	4	4	D3
	RTO02_1 (PPG02_1)		111	77	77	F11
	RTO03_0 (PPG02_0)	Wave form generator output pin of Multi-function timer 0. This pin operates as PPG02 when it is used in PPG0 output modes.	9	5	5	D2
	RTO03_1 (PPG02_1)		116	78	78	F12

Table 12-9 Typical and Maximum Current Consumption in Stop Mode, Timer Mode and RTC Mode

Parameter	Symbol	Pin Name	Conditions	Frequency (MHz)	Value		Unit	Remarks
					Typ*1	Max*2		
Power supply current	I_{CCH}	VCC	Stop mode	-	0.41	2.07	mA	*3, *4 T_A=+25°C
					-	21.35	mA	*3, *4 T_A=+85°C
					-	30.57	mA	*3, *4 T_A=+105°C
	I_{CCT}		Timer mode (built-in High-speed CR)	4 MHz	1.14	2.8	mA	*3, *4 T_A=+25°C
					-	22.08	mA	*3, *4 T_A=+85°C
					-	31.3	mA	*3, *4 T_A=+105°C
			Timer mode *5 (Sub oscillation)	32 kHz	0.43	2.09	mA	*3, *4 T_A=+25°C
					-	21.37	mA	*3, *4 T_A=+85°C
					-	30.59	mA	*3, *4 T_A=+105°C
			Timer mode (built-in Low-speed CR)	100 kHz	0.43	2.09	mA	*3, *4 T_A=+25°C
					-	21.37	mA	*3, *4 T_A=+85°C
					-	30.59	mA	*3, *4 T_A=+105°C
	I_{CCR}		RTC mode (Sub oscillation)	32 kHz	0.41	2.07	mA	*3, *4 T_A=+25°C
					-	21.35	mA	*3, *4 T_A=+85°C
					-	30.57	mA	*3, *4 T_A=+105°C

*1: V_{CC}=3.3 V

*2: V_{CC}=3.6 V

*3: When all ports are fixed.

*4: When LVD is OFF

*5: When using the crystal oscillator of 32 kHz (including the current consumption of the oscillation circuit)

Table 12-11 Typical and Maximum Current Consumption in Low-voltage Detection Circuit, Main Flash Memory Write/erase, VFLASH Memory

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Low-voltage detection circuit (LVD) power supply current	I_{CCLVD}	VCC	At operation	-	4	7	µA	For occurrence of interrupt
Main flash memory write/erase current	$I_{CCFLASH}$		At Write/Erase	-	13.4	15.8	mA	
VFLASH memory Standby current	$I_{CCVFLASH}$		At Standby	-	15	35	µA	
VFLASH memory Read current			At Read	-	9	14	mA	40MHz
					13	20		80MHz
VFLASH memory write/erase current			At Write/Erase	-	20	25	mA	

Peripheral Current Dissipation

Clock system	Peripheral		Unit	Frequency (MHz)			Unit	Remarks
				40	80	160		
HCLK	GPIO		All ports	0.30	0.60	1.19	mA	T_A=+25°C, V_{CC}=3.3 V
	DMAC		-	0.99	1.95	3.82		
	DSTC		-	0.41	0.83	1.61		
	External bus I/F		-	0.18	0.35	0.70		
	CAN-FD		1ch.	0.54	1.07	2.13		
	USB		1ch.	0.47	0.93	1.85		
	I^2S		1 unit	0.36	0.71	1.42		
	Programmable CRC		-	0.04	0.09	0.18		
PCLK1	Base timer		4ch.	0.20	0.39	0.76	mA	T_A=+25°C, V_{CC}=3.3 V
	Multi-functional timer/PPG		1unit/4ch.	0.61	1.21	2.40		
	Quadrature position/Revolution counter		1ch.	0.04	0.09	0.18		
	A/DC		1 unit	0.25	0.50	1.00		
PCLK2	Multi-function serial		1ch.	0.44	0.88	-	mA	T_A=+25°C, V_{CC}=3.3 V
GECLK	GDC unit	GDC	1 unit	31	57	109	mA	T_A=+25°C, V_{CC}=3.3 V
		High-Speed Quad SPI	1ch.	1.1	2.3	-		
		HyperBus I/F	1 unit	0.6	1.2	-		
		SDRAM-IF	1ch.	2.3	4.6	-		

12.3.2 Pin Characteristics

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
H level input voltage (hysteresis input)	V_{IHS}	CMOS hysteresis input pin, MD0, MD1	-	V_{CC}×0.8	-	V_{CC} + 0.3	V	
		5 V tolerant input pin	-	V_{CC}×0.8	-	V_{SS} + 5.5	V	
		Input pin doubled as I^2C Fm+	-	V_{CC}×0.7	-	V_{SS} + 5.5	V	
		TTL Schmitt input pin	-	2.0	-	V_{CC}+0.3	V	
L level input voltage (hysteresis input)	V_{ILS}	CMOS hysteresis input pin, MD0, MD1	-	V_{SS} - 0.3	-	V_{CC}×0.2	V	
		5 V tolerant input pin	-	V_{SS} - 0.3	-	V_{CC}×0.2	V	
		Input pin doubled as I^2C Fm+	-	V_{SS}	-	V_{CC}×0.3	V	
		TTL Schmitt input pin	-	V_{SS} - 0.3	-	0.8	V	
H level output voltage	V_{OH}	2 mA type	I_{OH} = - 2 mA	V_{CC} - 0.5	-	V_{CC}	V	
		4 mA type	I_{OH} = - 4 mA	V_{CC} - 0.5	-	V_{CC}	V	
		8 mA type	I_{OH} = - 8 mA	V_{CC} - 0.5	-	V_{CC}	V	
		11 mA type	I_{OH} = - 11 mA	V_{CC} - 0.5	-	V_{CC}	V	High-speed IO
		The pin doubled as USB I/O	I_{OH} = - 13.0 mA	V_{CC} - 0.4	-	V_{CC}	V	
		The pin doubled as I^2C Fm+	I_{OH} = - 3 mA	V_{CC} - 0.5	-	V_{CC}	V	At GPIO
L level output voltage	V_{OL}	2 mA type	I_{OL} = 2 mA	V_{SS}	-	0.4	V	
		4 mA type	I_{OL} = 4 mA	V_{SS}	-	0.4	V	
		8 mA type	I_{OL} = 8 mA	V_{SS}	-	0.4	V	
		11 mA type	I_{OL} = 11 mA	V_{SS}	-	0.4	V	
		The pin doubled as USB I/O	I_{OL} = 10.5 mA	V_{SS}	-	0.4	V	
		The pin doubled as I^2C Fm+	I_{OL} = 3 mA	V_{SS}	-	0.4	V	At GPIO
			I_{OL} = 20 mA					At I^2C Fm+
Input leak current	I_{IL}	-	-	- 5	-	+ 5	µA	
Pull-up resistor value	R_{PU}	Pull-up pin	-	30	80	200	kΩ	
			-	15	33	70		High-speed IO
Input capacitance	C_{IN}	Other than VCC, VBAT, VSS, AVCC, AVSS, AVRH	-	-	5	15	pF	

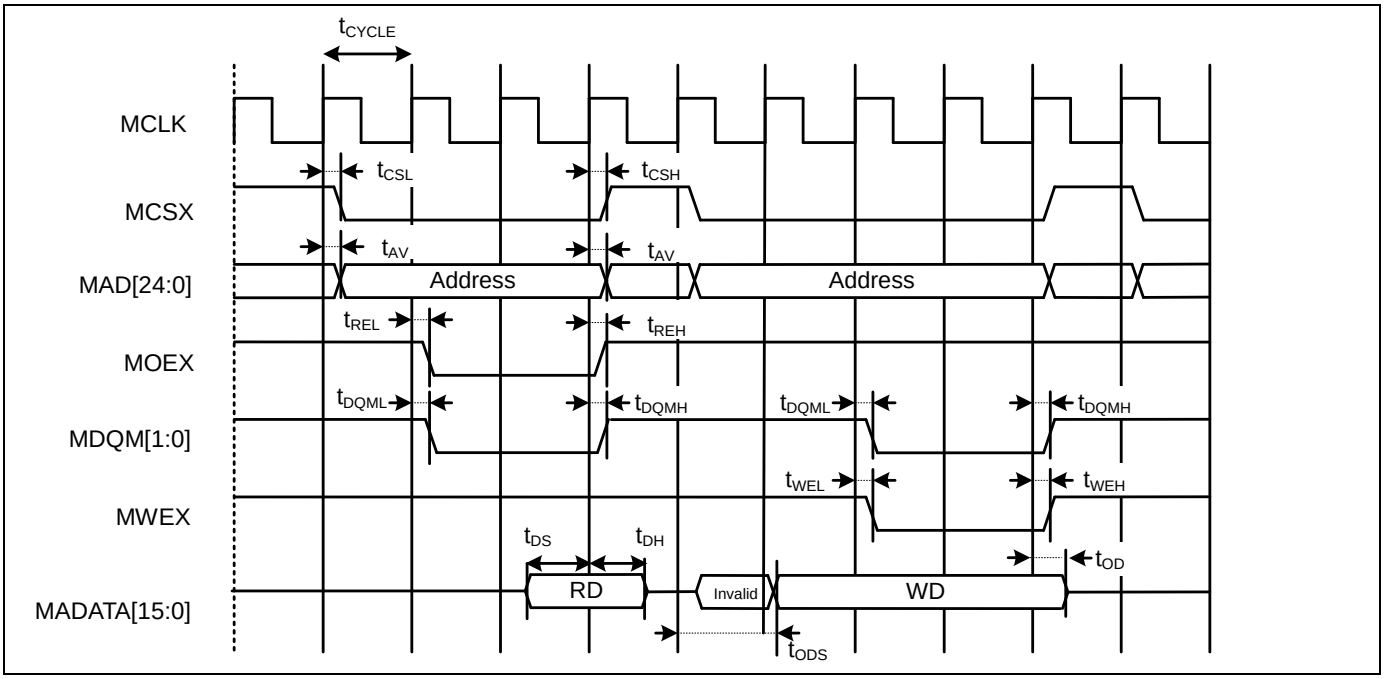
Separate Bus Access Synchronous SRAM Mode

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Address delay time	t_{AV}	MCLK, MAD[24:0]	-	1	9	ns	
MCSX delay time	t_{CSL}	MCLK, MCSX	-	1	9	ns	
	t_{CSH}		-	1	9	ns	
MOEX delay time	t_{REL}	MCLK, MOEX	-	1	9	ns	
	t_{REH}		-	1	9	ns	
Data set up →MCLK ↑ time	t_{DS}	MCLK, MADATA[15:0]	-	19	-	ns	
MCLK ↑ → Data hold time	t_{DH}	MCLK, MADATA[15:0]	-	0	-	ns	
MWEX delay time	t_{WEL}	MCLK, MWEX	-	1	9	ns	
	t_{WEH}		-	1	9	ns	
MDQM[1:0] delay time	t_{DQML}	MCLK, MDQM[1:0]	-	1	9	ns	
	t_{DQMH}		-	1	9	ns	
MCLK ↑ → Data output time	t_{ODS}	MCLK, MADATA[15:0]	-	MCLK+1	MCLK+18	ns	
MCLK ↑ → Data hold time	t_{OD}	MCLK, MADATA[15:0]	-	1	18	ns	

Note:

- *When the external load capacitance C_L = 30 pF*



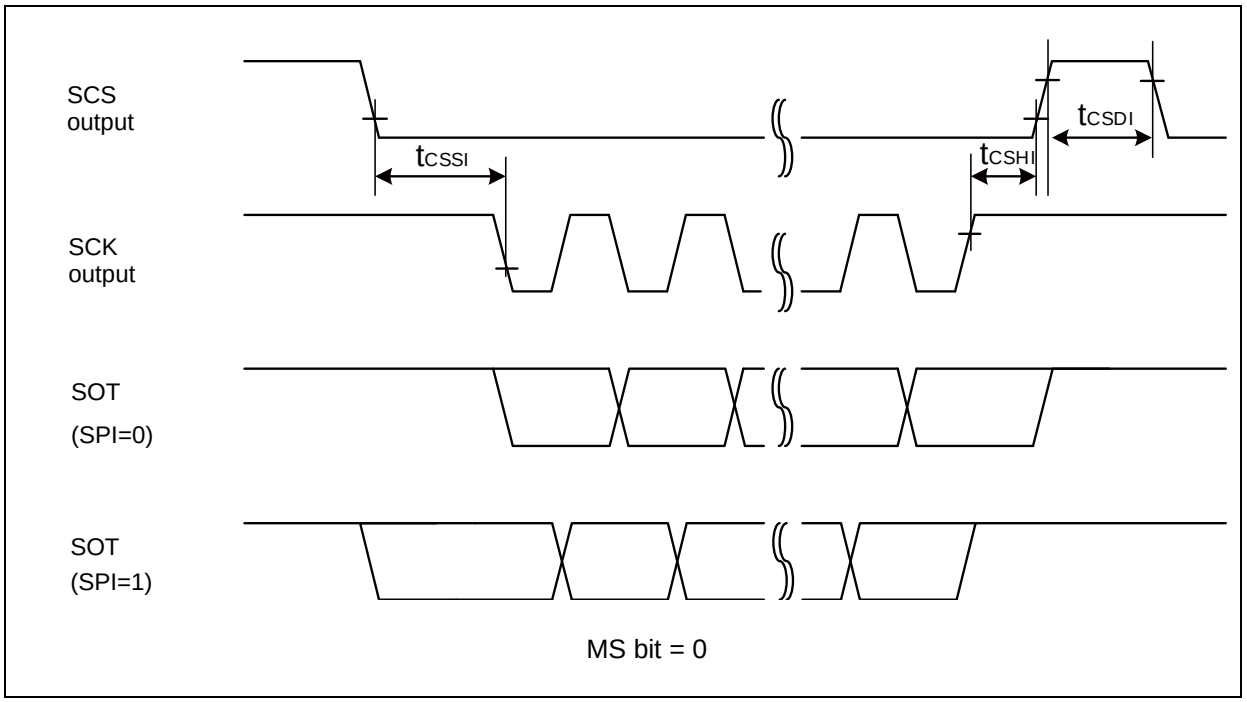
Synchronous Serial (SPI = 1, SCINV = 1)

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Baud rate	-	-	-	-	8	Mbps
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	ns
SCK↓→SOT delay time	t_{SLOVI}	SCKx, SOTx		- 30	+ 30	ns
SIN→SCK↑ setup time	t_{IVSHI}	SCKx, SINx		50	-	ns
SCK↑→SIN hold time	t_{SHIXI}	SCKx, SINx		0	-	ns
SOT→SCK↑ delay time	t_{SOVHI}	SCKx, SOTx		$2t_{CYCP}$ - 30	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ - 10	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	ns
SCK↓→SOT delay time	t_{SLOVE}	SCKx, SOTx		-	50	ns
SIN→SCK↑ setup time	t_{IVSHE}	SCKx, SINx		10	-	ns
SCK↑→SIN hold time	t_{SHIXE}	SCKx, SINx		20	-	ns
SCK falling time	t_F	SCKx		-	5	ns
SCK rising time	t_R	SCKx		-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which multi-function serial is connected to, see 8. Block Diagram in this data sheet.
- *These characteristics only guarantee the same relocate port number.*
  For example, the combination of SCKx_0 and SOTx_1 is not guaranteed.
- *When the external load capacitance C_L = 30 pF.*



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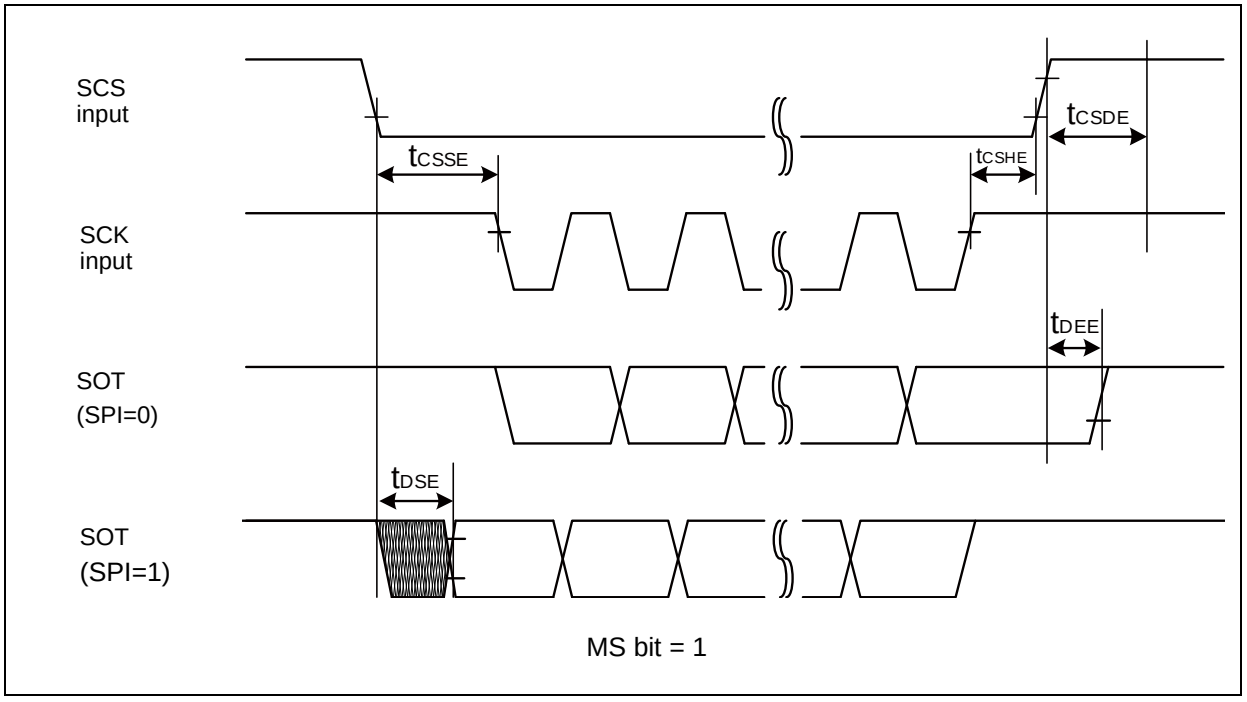
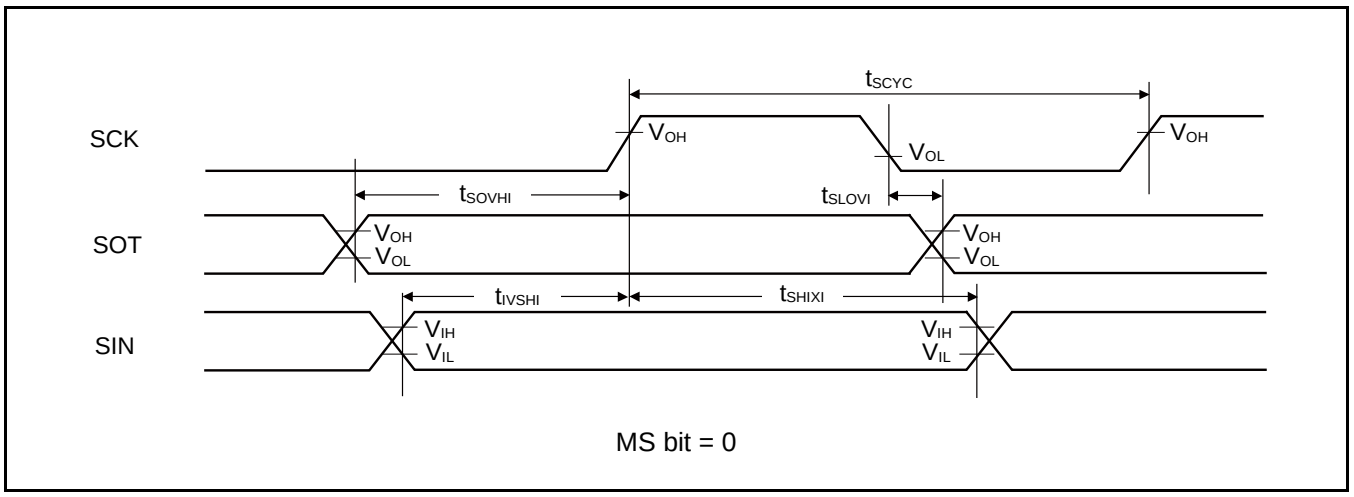
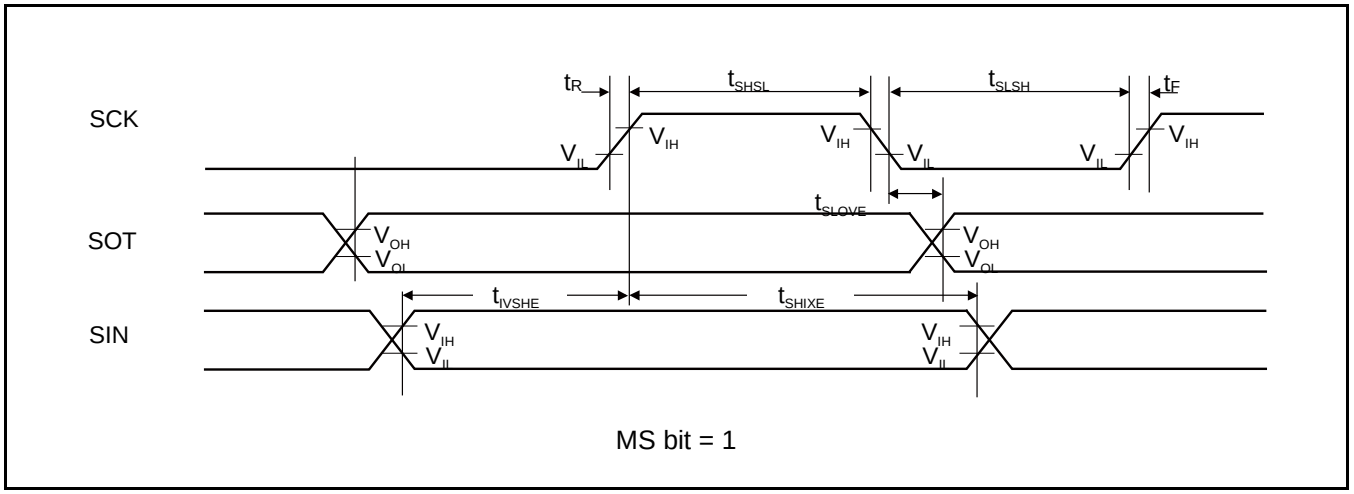


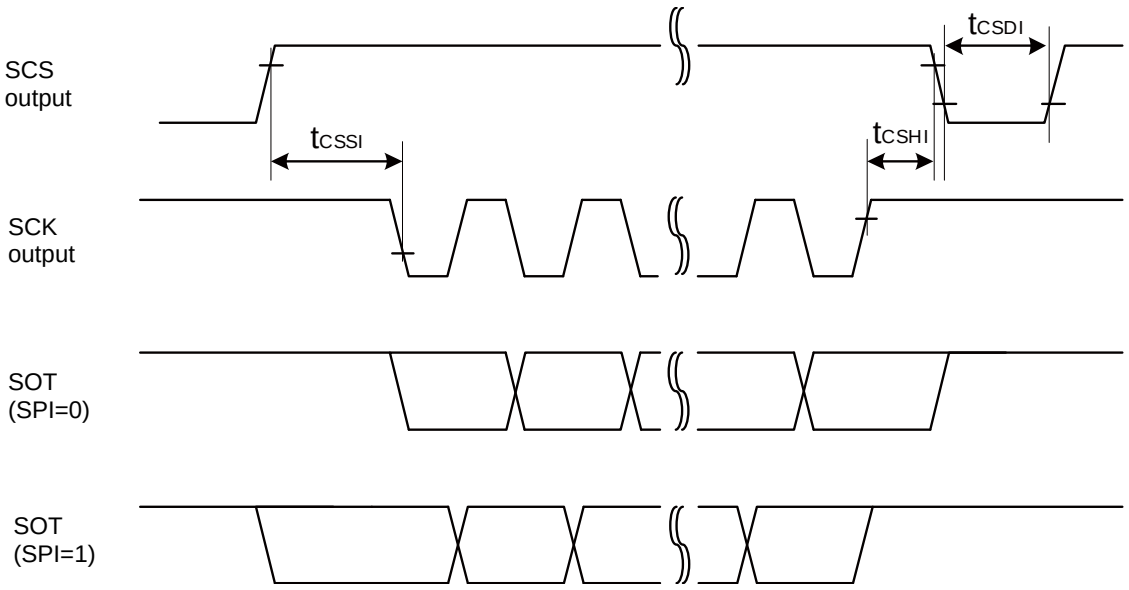
MS bit = 1



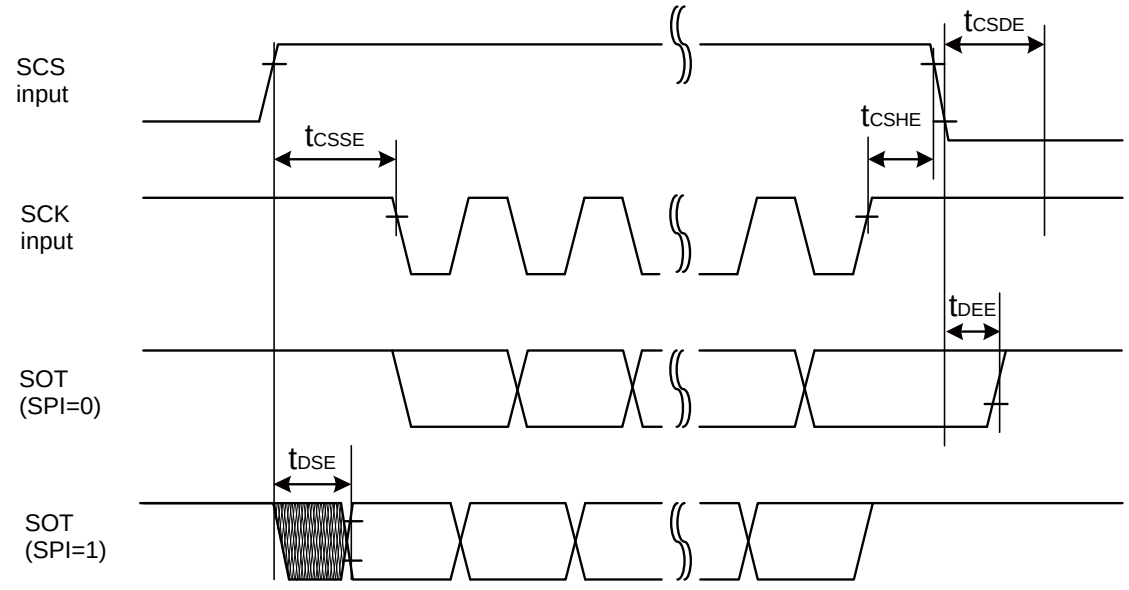
MS bit = 0



MS bit = 1



MS bit = 0



MS bit = 1

12.4.13 External Input Timing

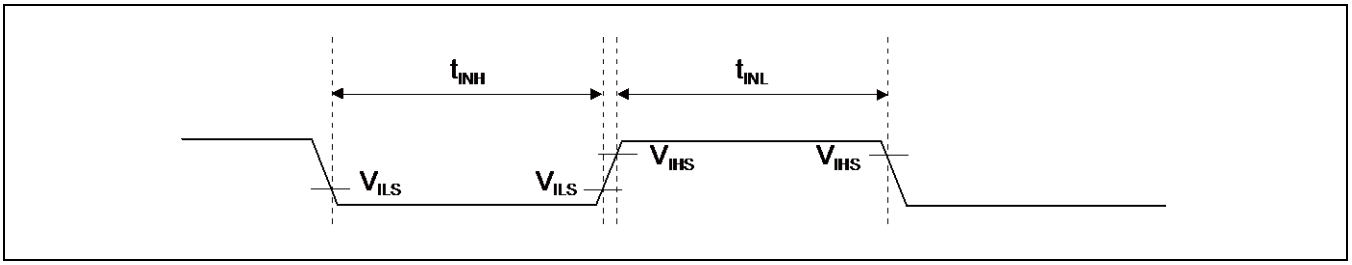
(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{INH}, t_{INL}	ADTG	-	$2t_{CYCP}$*1	-	ns	A/D converter trigger input
		FRCK0					Free-run timer input clock
		IC0x					Input capture
		DTTI0X	-	$2t_{CYCP}$*1	-	ns	Waveform generator
		INTxx, NMIX	-	$2t_{CYCP}$ + 100(*1)	-	ns	External interrupt, NMI
				500(*2)	-	ns	
		WKUPx	-	500(*3)	-	ns	Deep standby wake up

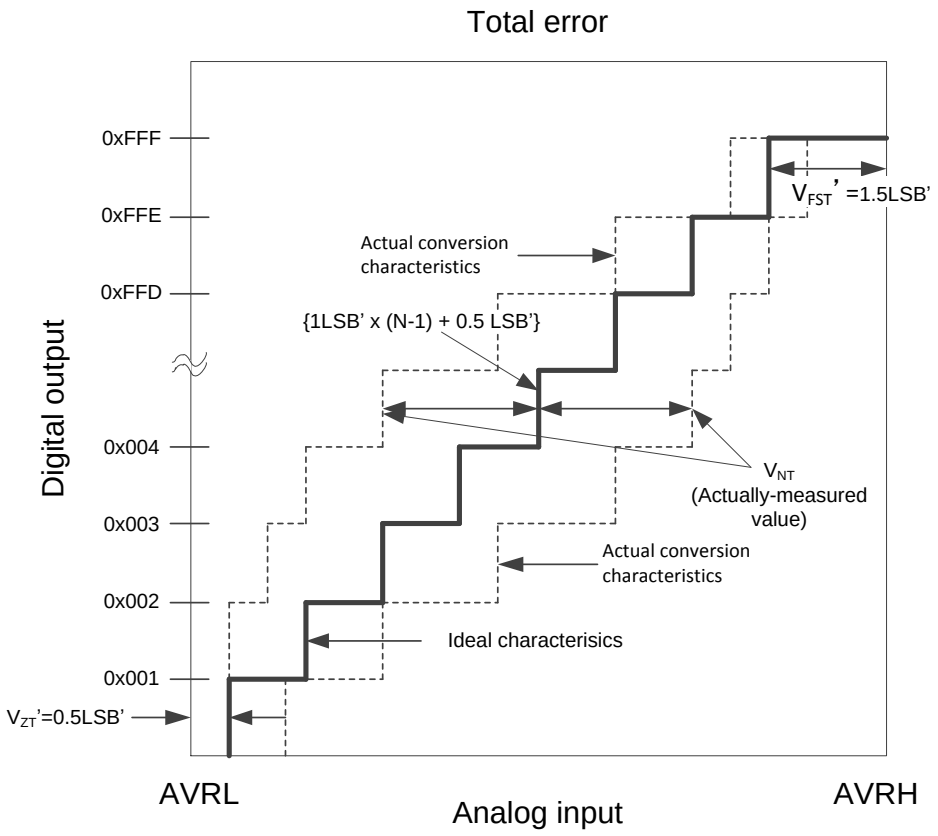
(*1): t_{CYCP} indicates the APB bus clock cycle time except stop when in Stop mode, in timer mode. About the APB bus number which the Multi-function Timer and External interrupt are connected to, see 8. Block Diagram in this data sheet.

(*2): When in Stop mode, in timer mode.

(*3): When in deep standby RTC mode, in deep standby Stop mode.



■Total error: A difference between actual value and theoretical value.
The overall error includes zero-transition voltage, full-scale transition voltage and linearity error.



$$\text{Total error of digital output N} = \frac{V_{NT} - \{1\ LSB' \times (N-1) + 0.5\ LSB'\}}{1\ LSB'} \quad [LSB]$$

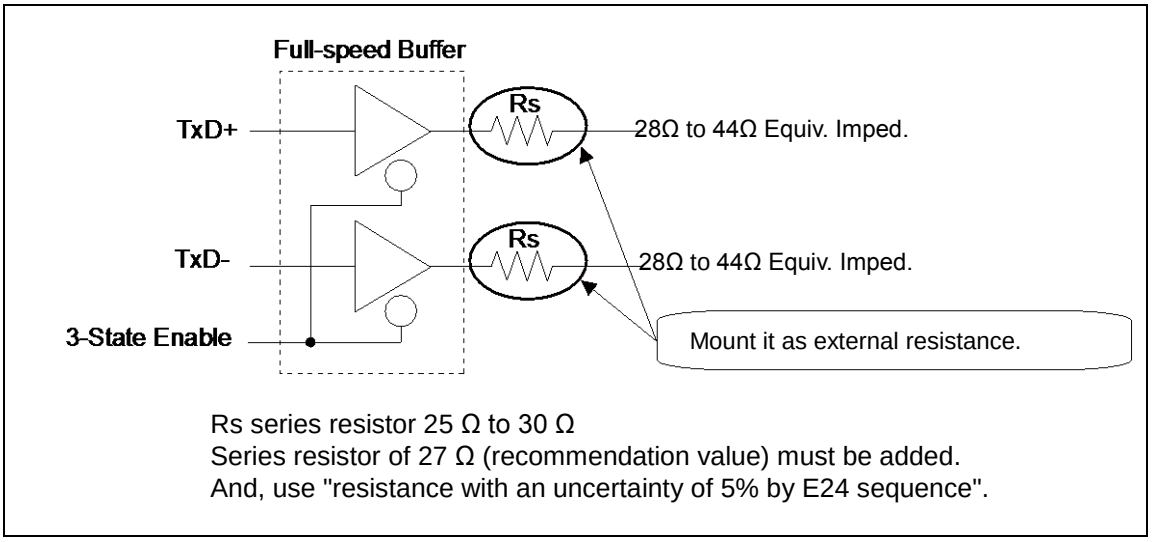
$$1\ LSB'\ (\text{ideal value}) = \frac{AVRH - AVRL}{4096} \quad [V]$$

V_{ZT}' (ideal value) = AVRL + 0.5 LSB' [V]

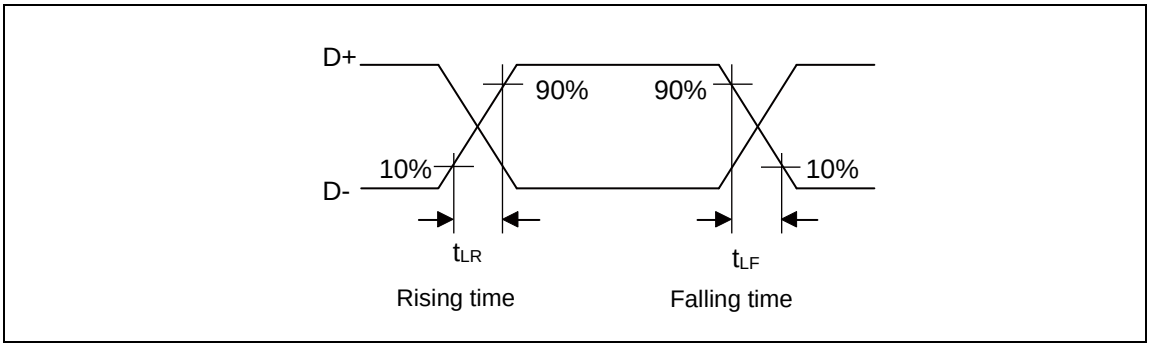
V_{FST}' (ideal value) = AVRH - 1.5 LSB' [V]

V_{NT}': A voltage for causing transition of digital output from (N-1) to N

*6: USB Full-speed connection is performed via twist pair cable shield with 90 Ω ± 15 % characteristic impedance (Differential Mode).
USB standard defines that output impedance of USB driver must be in range from 28 Ω to 44 Ω. So, discrete series resistor (Rs) addition is defined in order to satisfy the above definition and keep balance.
When using this USB I/O, use it with 25 Ω to 30 Ω (recommendation value 27 Ω) Series resistor Rs.



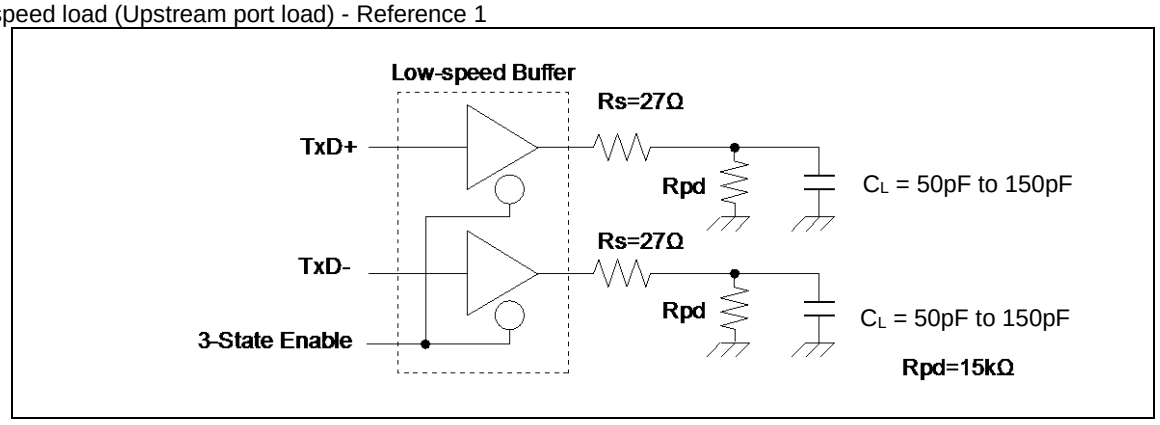
*7: They indicate rising time (t_{LR}) and Falling time (t_{LF}) of the Low-speed differential data signal.
They are defined by the time between 10 % and 90 % of the output signal voltage.



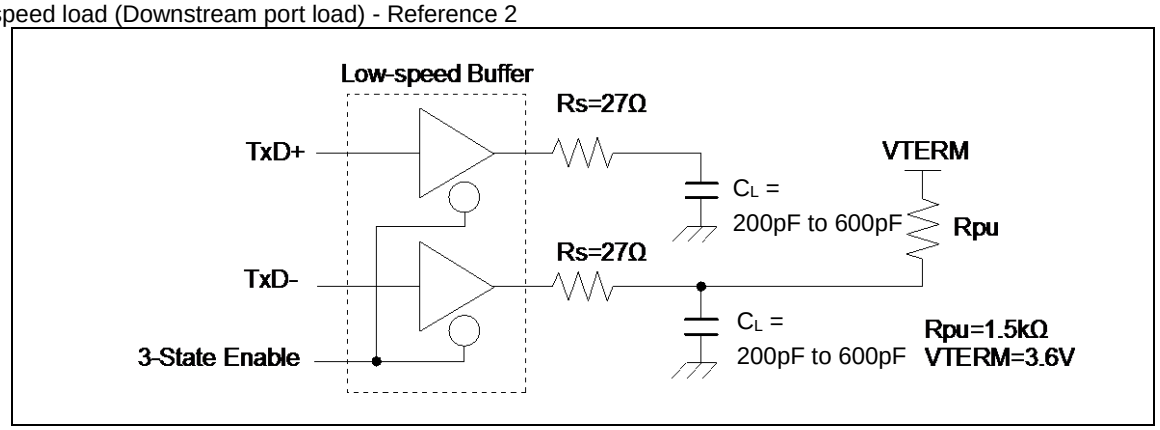
Note:

- *See Low-speed load (Compliance load) for conditions of external load.*

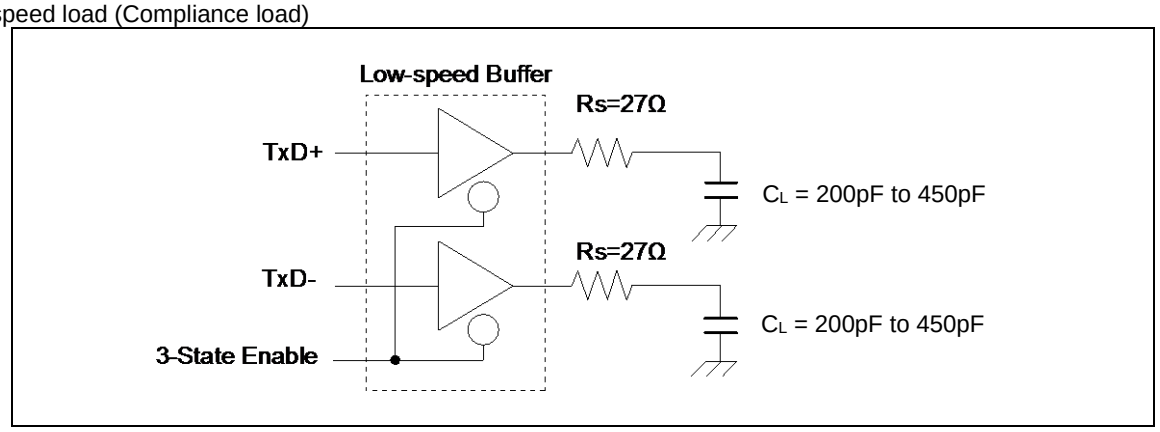
■Low-speed load (Upstream port load) - Reference 1



■Low-speed load (Downstream port load) - Reference 2



■Low-speed load (Compliance load)



12.10 Standby Recovery Time

12.10.1 Recovery Cause: Interrupt/WKUP

The time from recovery cause reception of the internal circuit to the program operation start is shown.

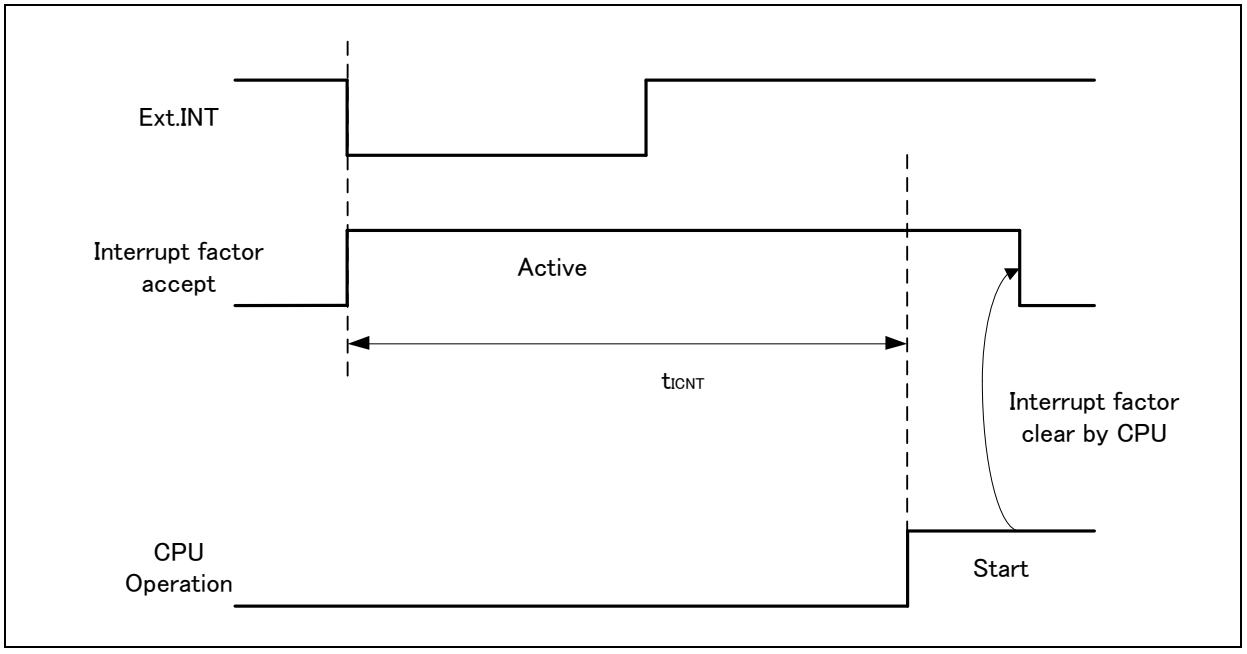
Recovery Count Time

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Value		Unit	Remarks
		Typ	Max*		
Sleep mode	t_{ICNT}	HCLK×1		µs	
High-speed CR Timer mode Main Timer mode PLL Timer mode		40	80	µs	
Low-speed CR timer mode		450	900	µs	
Sub timer mode		896	1136	µs	
RTC mode Stop mode (High-speed CR /Main/PLL run mode return)		316	581	µs	
RTC mode Stop mode (Low-speed CR/sub run mode return)		270	540	µs	
Deep standby RTC mode		365	667	µs	without RAM retention
Deep standby Stop mode		365	667	µs	with RAM retention

*: The maximum value depends on the built-in CR accuracy.

Example of standby recovery operation (when in external interrupt recovery*)



*: External interrupt is set to detecting fall edge.

Document History

Document Title: S6E2D5 Series 32-bit ARM® Cortex®-M4F, FM4 Microcontroller
Document Number: 002-03982

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	–	AKIH	04/21/2015	New Spec
*A	5040094	AKIH	01/14/2016	Updated to Cypress template
*B	5123103	SHOY	03/04/2016	Added CCS/CCB settings in 7. HandlingDevices (Page58) and Table 12-10 Typical…*6,*7 (page 85). Changed PN: S6E2DH5G0AGZ20000 to S6E2DH5G0AGE20000 in 13. Ordering… (Page 172). Changed “GE_SPCSX_0” to “GE_SPCSX0” in 3. PinAssignment (Page 9, 11), 4. PinDescriptions (Page16, 42), 8. BlockDiagram (Page 61) and 12.4.21 GDC: … (Page 154,155) Changed “GE_HBCSX_0” to “GE_HBCSX0” in 3. PinAssignment (Page 9, 11), 4. PinDescriptions (Page 16, 42) , 8. BlockDiagram (Page 61) and 12.4.22 GDC: ... (Page 156,157) Changed “GE_HBCSX_1” to “GE_HBCSX1” in 3. PinAssignment (Page 9, 11), 4. PinDescriptions (Page 14, 42), 8. BlockDiagram (Page 61) and 12.4.22 GDC: … (Page 156,157) Updated VFLASH memory Standby current value to 35uA in Table 12-11 Typical… (Page 86). Changed “Ex_LQFP” to “Ex-LQFP” in 2. Packages (Page 8), 4. Pin Descriptions (Page 13 to 46), 12.2 Recommended… (Page 74) and 13. Ordering… (Page 172). Changed “VMAKEUP” to “VWAKEUP” in 8. BlockDiagram (Page 61). Changed “HW flow control (ch. 4, 5)” to “HW flow control (ch. 4)” in 8. BlockDiagram (Page 61). Added “(N.C.): Do not connect anything” in 3. Pin Assignment (Page 10). Added the Note in 4. Pin Descriptions (Page 46). Added Function of PNL_TSIG in 4. Pin Descriptions (Page 43). Changed “PFBGA” to “FBGA” in 12.2 Recommended… (Page 74) and 13. Ordering… (Page 172). New added errata in 15. Errata (Page 177 to 178).
*C	5634638	YSKA	02/21/2017	Changed an explanation from “from 01 to 99” to “from 00 to 99” in Real-Time Clock (RTC) (Page 3) of Features. Added an explanation in Notes on Power-on (Page 60) of 7. Handling Devices. Changed “VBAT Power-on Reset” to “Power-on Reset” in List of VBAT Domain Pin Status (Page 71) of 11. Pin Status in Each CPU State, and Added Remark *1. Added Remark *8 in Table 12-10 Typical and Maximum Current Consumption in Deep Standby Stop Mode, Deep Standby RTC Mode and VBAT (Page 85). Changed Parameter “Power supply rising time (t_{VCCR})” to “Power ramp rate (dV/dt)” in 12.4.8 Power-on Reset Timing (Page 92), Changed the minimum to 0.6mV/µs, Changed the maximum to 1000mV/µs, and Added Remarks and Note. Deleted setting value “SPI=1” and “MS=0” at using chip select in 12.4.12 CSIO Timing, and Added “MS bit = 0” and “MS bit = 1” on the Figure (P113-120, P129-136).