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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	160MHz
Connectivity	CSIO, EBI/EMI, I²C, LINbus, SD, SPI, UART/USART, USB
Peripherals	DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	90
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	36K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 24x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	120-LQFP
Supplier Device Package	120-LQFP (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e2df5gjamv20000

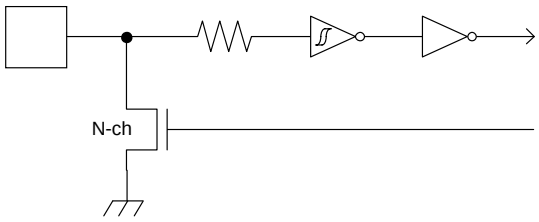
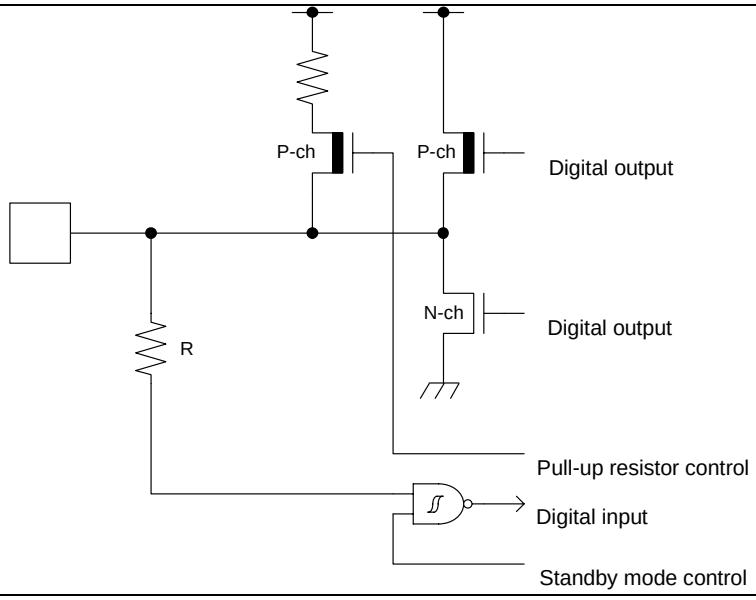
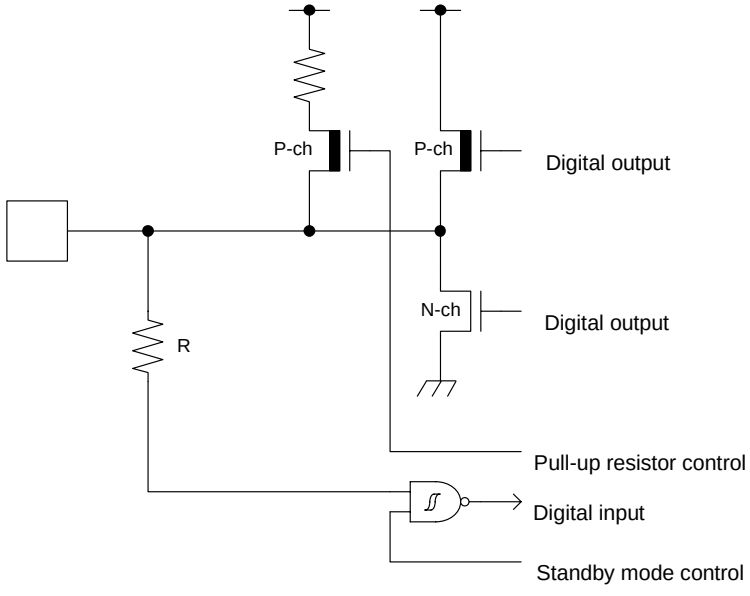
Pin No.				Pin name	I/O circuit type	Pin state type
LQFP176	LQFP120 Ex-LQFP120	LQFP120 (S6E2D55GJA)	FBGA161			
65	43	43	K7	P50 WKUP1 MCSX0_0	D	P
66	44	44	L7	P51 TIOB0_1 PNL_PWE PNL_TSIG4	E	I
67	45	45	K8	P52 TIOB1_1 PNL_DCLK	D	I
68	46	46	L8	P53 TIOB2_1 PNL_DEN PNL_TSIG2	E	I
69	47	47	K9	P54 TIOB3_1 PNL_LE PNL_TSIG3	E	I
70	48	48	L9	P55 TIOB4_1 PNL_LH_SYNC PNL_TSIG0	E	I
71	49	49	L10	P56 TIOB5_1 PNL_FV_SYNC PNL_TSIG1	E	I
72	–	–	–	PB8 GE_SDDQ11	L	I
73	–	–	–	PB9 GE_SDDQ10	L	I
74	–	–	–	PBA GE_SDDQ9	L	I
75	–	–	–	PBB GE_SDDQ8	L	I
76	–	–	–	PBC GE_SDDQ7	L	I
77	–	–	–	PBD GE_SDDQ6	L	I
78	50	50	M8	INITX	B	C
79	51	51	N7	P46 X0A	P	S
80	52	52	N9	P47 X1A	Q	T

Module	Pin Name	Function	Pin No.			
			LQFP176	LQFP120 Ex-LQFP120	LQFP120 (S6E2D55GJA)	FBGA161
GPIO	PB0	General-purpose I/O port B	47	–	–	–
	PB1		48	–	–	–
	PB2		49	–	–	–
	PB3		50	–	–	–
	PB4		56	–	–	–
	PB5		57	–	–	–
	PB6		58	–	–	–
	PB7		59	–	–	–
	PB8		72	–	–	–
	PB9		73	–	–	–
	PBA		74	–	–	–
	PBB		75	–	–	–
	PBC		76	–	–	–
	PBD		77	–	–	–
	PC0	General-purpose I/O port C	94	–	–	–
	PC1		95	–	–	–
	PC2		96	–	–	–
	PC3		97	–	–	–
	PC4		98	–	–	–
	PC5		99	–	–	–
	PC6		112	–	–	–
	PC7		113	–	–	–
	PC8		114	–	–	–
	PC9		115	–	–	–
	PCA		126	–	–	–
	PCB		127	–	–	–
	PCC		128	–	–	–
	PCD		129	–	–	–
	PD0	General-purpose I/O port D	134	–	–	–
	PD1		135	–	–	–
	PD2		136	–	–	–
	PD3		137	–	–	–
	PD4		138	–	–	–
	PD5		144	–	–	–
	PD6		145	–	–	–
	PD7		146	–	–	–
	PD8		147	–	–	–
	PD9		148	–	–	–
	PDA		166	–	–	–
	PDB		167	–	–	–
	PDC		168	–	–	–
	PDD		169	–	–	–

Module	Pin Name	Function	Pin No.			
			LQFP176	LQFP120 Ex-LQFP120	LQFP120 (S6E2D55GJA)	FBGA161
Multi-function serial 7	SIN7_0	Multi-function serial interface ch.7 input pin	8	4	4	D3
	SOT7_0 (SDA7_0)	Multi-function serial interface ch.7 output pin. This pin operates as SOT7 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA7 when it is used in an I^2C (operation mode 4).	9	5	5	D2
	SCK7_0 (SCL7_0)	Multi-function serial interface ch.7 clock I/O pin. This pin operates as SCK7 when it is used in a CSIO (operation mode 2) and as SCL7 when it is used in an I^2C (operation mode 4).	10	6	6	D1
	SCS70_0	Multi-function serial interface ch.7 chip select 0 input/output pin	7	3	3	C2
Multi-function Timer 0	DTTI0X_0	Input signal controlling wave form generator outputs RTO00 to RTO05 of Multi-function timer 0.	27	17	17	F1
	DTTI0X_1		104	70	70	H12
	FRCK0_0	16-bit free-run timer ch.0 external clock input pin	20	10	10	E2
	FRCK0_1		103	69	69	H11
	IC00_0	16-bit input capture input pin of Multi-function timer 0. ICxx describes channel number.	26	16	16	F2
	IC00_1		105	71	71	H13
	IC01_0		25	15	15	F3
	IC01_1		106	72	72	G10
	IC02_0		22	12	12	F4
	IC02_1		107	73	73	G11
	IC03_0		21	11	11	E1
	IC03_1		108	74	74	G12
	RTO00_0 (PPG00_0)	Wave form generator output pin of Multi-function timer 0. This pin operates as PPG00 when it is used in PPG0 output modes.	6	2	2	C3
	RTO00_1 (PPG00_1)		109	75	75	G13
	RTO01_0 (PPG00_0)	Wave form generator output pin of Multi-function timer 0. This pin operates as PPG00 when it is used in PPG0 output modes.	7	3	3	C2
	RTO01_1 (PPG00_1)		110	76	76	F10
	RTO02_0 (PPG02_0)	Wave form generator output pin of Multi-function timer 0. This pin operates as PPG02 when it is used in PPG0 output modes.	8	4	4	D3
	RTO02_1 (PPG02_1)		111	77	77	F11
	RTO03_0 (PPG02_0)	Wave form generator output pin of Multi-function timer 0. This pin operates as PPG02 when it is used in PPG0 output modes.	9	5	5	D2
	RTO03_1 (PPG02_1)		116	78	78	F12

Module	Pin Name	Function	Pin No.			
			LQFP176	LQFP120 Ex-LQFP120	LQFP120 (S6E2D55GJA)	FBGA161
GDC Panel	PNL_DCLK	GDC clock output pin	67	45	45	K8
	PNL_DEN	GDC data enable output pin (blanking signal)	68	46	46	L8
	PNL_PWE	GDC power enable control output pin	66	44	44	L7
	PNL_LE	GDC line end output pin	69	47	47	K9
	PNL_LH_SYNC	GDC horizontal synchronization output pin	70	48	48	L9
	PNL_FV_SYNC	GDC vertical synchronization output pin	71	49	49	L10
	PNL_PD0	GDC panel data output pin	165	113	113	C4
	PNL_PD1		164	112	112	B5
	PNL_PD2		163	111	111	C5
	PNL_PD3		162	110	110	A6
	PNL_PD4		161	109	109	B6
	PNL_PD5		160	108	108	C6
	PNL_PD6		158	106	106	B7
	PNL_PD7		157	105	105	C7
	PNL_PD8		156	104	104	A8
	PNL_PD9		155	103	103	B8
	PNL_PD10		154	102	102	C8
	PNL_PD11		153	101	101	A9
	PNL_PD12		152	100	100	B9
	PNL_PD13		151	99	99	C9
	PNL_PD14		150	98	98	D9
	PNL_PD15		149	97	97	C10
	PNL_PD16		131	89	89	C13
	PNL_PD17		130	88	88	C12
	PNL_PD18		125	87	87	D13
	PNL_PD19		124	86	86	D12
	PNL_PD20		123	85	85	D11
	PNL_PD21		122	84	84	D10
	PNL_PD22		121	83	83	E13
	PNL_PD23		120	82	82	E12
	PNL_TSIG0	GDC timing generator for panel control PNL_TSIG signals are customized synchronization signals for direct interfacing to the column and row drivers of most panel types. For more information, refer to Peripheral Manual (GDC Core part).	70	48	48	L9
	PNL_TSIG1		71	49	49	L10
	PNL_TSIG2		68	46	46	L8
	PNL_TSIG3		69	47	47	K9
	PNL_TSIG4		66	44	44	L7
	PNL_TSIG5		130	88	88	C12
	PNL_TSIG6		125	87	87	D13
	PNL_TSIG7		124	86	86	D12
	PNL_TSIG8		123	85	85	D11
	PNL_TSIG9		122	84	84	D10
	PNL_TSIG10		121	83	83	E13
	PNL_TSIG11		120	82	82	E12

Module	Pin Name	Function	Pin No.			
			LQFP176	LQFP120 Ex-LQFP120	LQFP120 (S6E2D55GJA)	FBGA161
GDC SDRAM-IF (176 pin only)	GE_SDDQ24	SDRAM-IF data input / output pin	18	-	-	-
	GE_SDDQ25		17	-	-	-
	GE_SDDQ26		16	-	-	-
	GE_SDDQ27		15	-	-	-
	GE_SDDQ28		14	-	-	-
	GE_SDDQ29		13	-	-	-
	GE_SDDQ30		5	-	-	-
	GE_SDDQ31		4	-	-	-
	GE_SDDQM0	SDRAM-IF input / output mask pin	148	-	-	-
	GE_SDDQM1		147	-	-	-
	GE_SDDQM2		146	-	-	-
	GE_SDDQM3		145	-	-	-
Reset	INITX	External Reset Input pin. A reset is valid when INITX = L.	78	50	50	M8
Mode	MD1	Mode 1 pin. During serial programming to Flash memory, MD1 = L must be input.	84	56	56	M12
	MD0	Mode 0 pin. During normal operation, MD0 = L must be input. During serial programming to Flash memory, MD0 = H must be input.	85	57	57	M11
Power	VCC	Power supply Pin	1	1	1	C1
			23	13	13	G1
			44	30	30	L1
			62	40	40	N4
			89	61	61	L13
			133	91	91	A12
			173	117	117	A4
GND	VSS	GND Pin	24	14	14	H1
			45	31	31	M1
			61	39	39	N3
			88	60	60	M13
			132	90	90	B13
			159	107	107	A7
			176	120	120	B1
Clock	X0	Main clock (oscillation) input pin	86	58	58	N11
	X0A	Sub clock (oscillation) input pin	79	51	51	N7
	X1	Main clock (oscillation) I/O pin	87	59	59	N12
	X1A	Sub clock (oscillation) I/O pin	80	52	52	N9
	CROUT_0	Built-in High-speed CR-osc clock output port	52	34	34	L4
	CROUT_1		64	42	42	N5
Analog Power	AVCC	A/D converter analog power supply pin	90	62	62	K13
	AVRL	A/D converter analog reference voltage input pin	92	64	64	J13
	AVRH	A/D converter analog reference voltage input pin	93	65	65	J12

Type	Circuit	Remarks
C		・Open drain output ・CMOS level hysteresis input
D		・CMOS level output ・CMOS level hysteresis input ・With pull-up resistor control ・With standby mode control ・Pull-up resistor : Approximately 80 kΩ ・I_{OH} = -4 mA, I_{OL} = 4 mA ・When this pin is used as an I^2C pin, the digital output P-ch transistor is always off.
E		・CMOS level output ・CMOS level hysteresis input ・With pull-up resistor control ・With standby mode control ・Pull-up resistor : Approximately 80 kΩ ・I_{OH} = -2 mA, I_{OL} = 2 mA ・When this pin is used as an I^2C pin, the digital output P-ch transistor is always off.

6.3 Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

1. Humidity

   Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.

2. Discharge of Static Electricity

   When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.

3. Corrosive Gases, Dust, or Oil

   Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.

4. Radiation, Including Cosmic Radiation

   Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.

5. Smoke, Flame

   CAUTION: Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of Cypress products in other special environmental conditions should consult with sales representatives.

Pin status Type	Function Group	Power-on Reset or Low-Voltage Detection State	INITX Input State	Device Internal Reset State	Run Mode or Sleep Mode State	Timer Mode RTC Mode or Stop Mode State		Deep Standby RTC Mode or Deep Standby Stop Mode State		Return from Deep Standby Mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
E	Mode input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / input enabled	GPIO selected	Hi-Z / input enabled	GPIO selected
F	NMIX selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	WKUP input enabled	Hi-Z / WKUP input enabled	Maintain previous state
	Resource other than above selected	Hi-Z	Hi-Z / input enabled	Hi-Z / input enabled			Hi-Z / Internal input fixed at 0			GPIO selected
	GPIO selected									
G	JTAG selected	Hi-Z	Pull-up / Input enabled	Pull-up / Input enabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state
	GPIO selected	Setting disabled	Setting disabled	Setting disabled			Hi-Z / Internal input fixed at 0	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
H	JTAG selected	Hi-Z	Pull-up / Input enabled	Pull-up / Input enabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state
	Resource other than above selected	Setting disabled	Setting disabled	Setting disabled			Hi-Z / Internal input fixed at 0	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	GPIO selected									
I	Resource selected	Hi-Z	Hi-Z / input enabled	Hi-Z / input enabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	GPIO selected									

Package thermal resistance and maximum permissible power for each package are shown below.
The operation is guaranteed maximum permissible power or less for semiconductor devices.

Table 12-1 Table for Package Thermal Resistance and Maximum Permissible Power

Package	Printed Circuit Board	Thermal Resistance θ_{JA} (°C/W)	Maximum Permissible Power (mW)	
			T_A= +85°C	T_A= +105°C
LQFP: LQM120 (0.5 mm pitch)	4 layers	38	1053	526
LQFP: LQM120 *1 (0.5 mm pitch)	4 layers	39	1026	513
LQFP: LQP176 (0.5 mm pitch)	4 layers	35	1143	571
FBGA: FDJ161 (0.5 mm pitch)	4 layers	35	1143	571
Ex-LQFP: LEM120 (0.5 mm pitch)	4 layers	18*2	2222	1111

*1: When S6E2D55GJA product.
*2: This is a case where the connection process was carried out back exposed die pad foundation. Please connect directly to GND back exposed die pad.

Notes:

1. *The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.*
2. *Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.*
3. *No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet.*
4. *Users considering application outside the listed conditions are advised to contact their representatives beforehand.*

Table 12-7 Typical and Maximum Current Consumption in Sleep Operation (PLL), when PCLK0 = PCLK1 = PCLK2 = HCLK

Parameter	Symbol	Pin Name	Conditions	Frequency*4 (MHz)	Value		Unit	Remarks
					Typ*1	Max*2		
Power supply current	I_{CCS}	VCC	Sleep *5,*6 operation (PLL)	72 MHz	84	160	mA	*3 When all peripheral clocks are ON GDC clock 160 MHz
				60 MHz	80	155	mA	
				48 MHz	75	150	mA	
				36 MHz	71	145	mA	
				24 MHz	67	141	mA	
				12 MHz	63	137	mA	
				8 MHz	61	134	mA	
				4 MHz	60	133	mA	
				72 MHz	15	82	mA	*3 When all peripheral clocks are OFF
				60 MHz	13	80	mA	
				48 MHz	12	79	mA	
				36 MHz	10	77	mA	
				24 MHz	8	75	mA	
				12 MHz	7	74	mA	
				8 MHz	6	73	mA	
				4 MHz	5	72	mA	

*1: T_A=+25°C, V_{CC}=3.3 V

*2: T_J=+125°C, V_{CC}=3.6 V

*3: When all ports are fixed.

*4: Frequency is a value of HCLK. PCLK0=PCLK1=PCLK2=HCLK

*5: When using the crystal oscillator of 4 MHz (including the current consumption of the oscillation circuit)

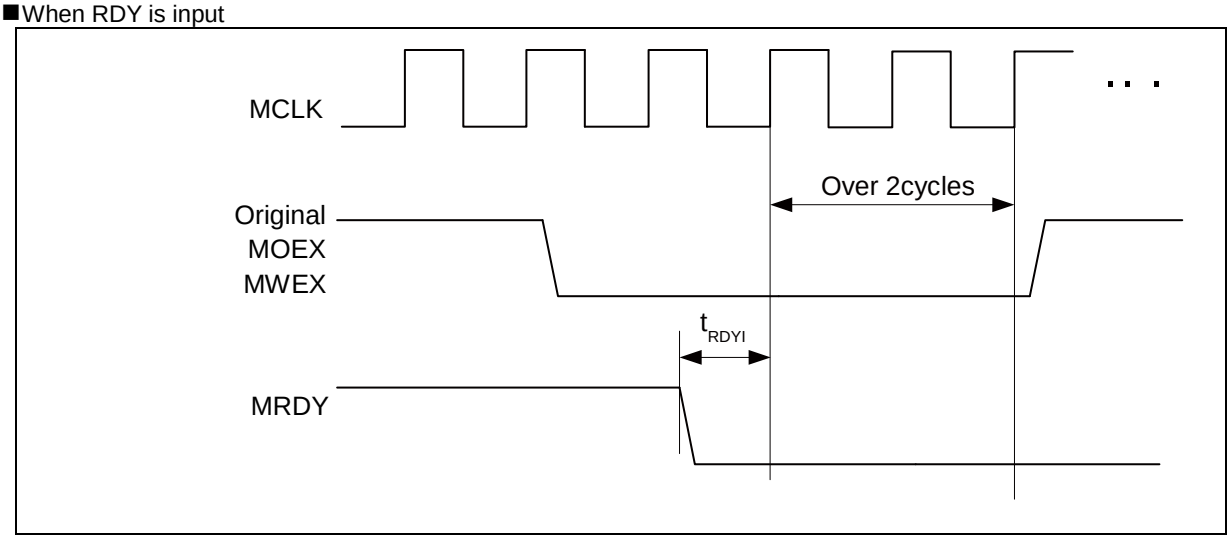
*6: Data access is nothing to VFLASH memory

External Ready Input Timing

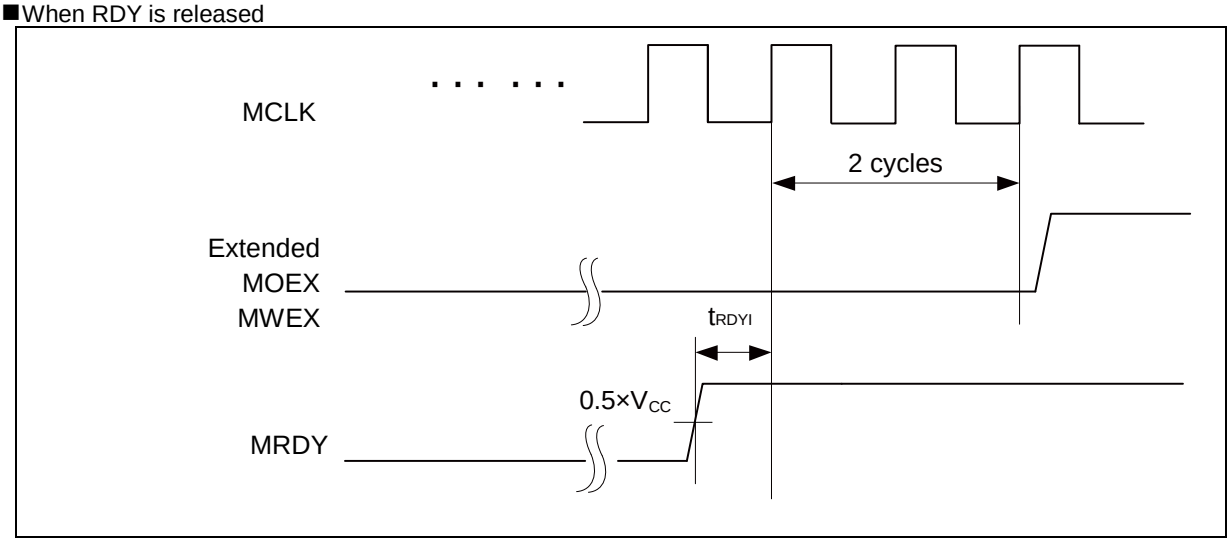
(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

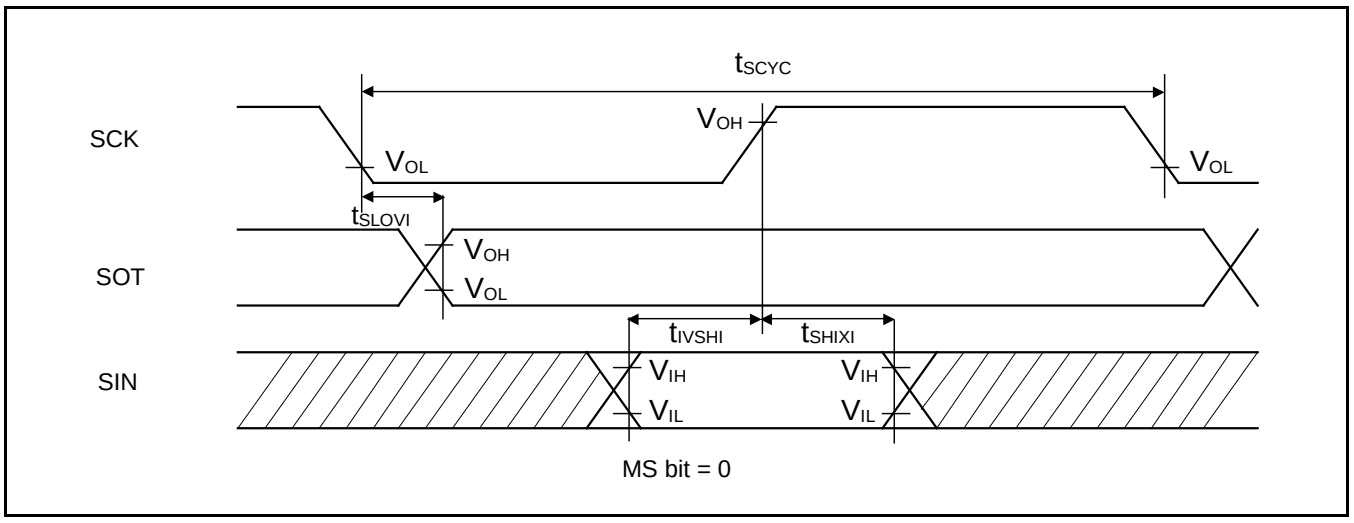
Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
MCLK↑ MRDY input setup time	t_{RDYI}	MCLK, MRDY	-	19	-	ns	

■When RDY is input

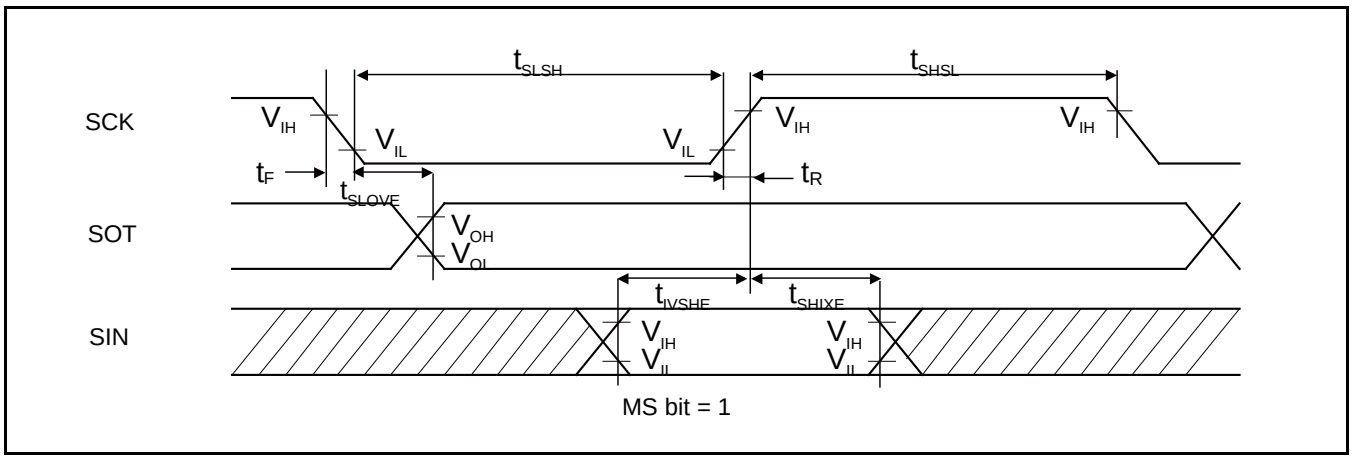


■When RDY is released

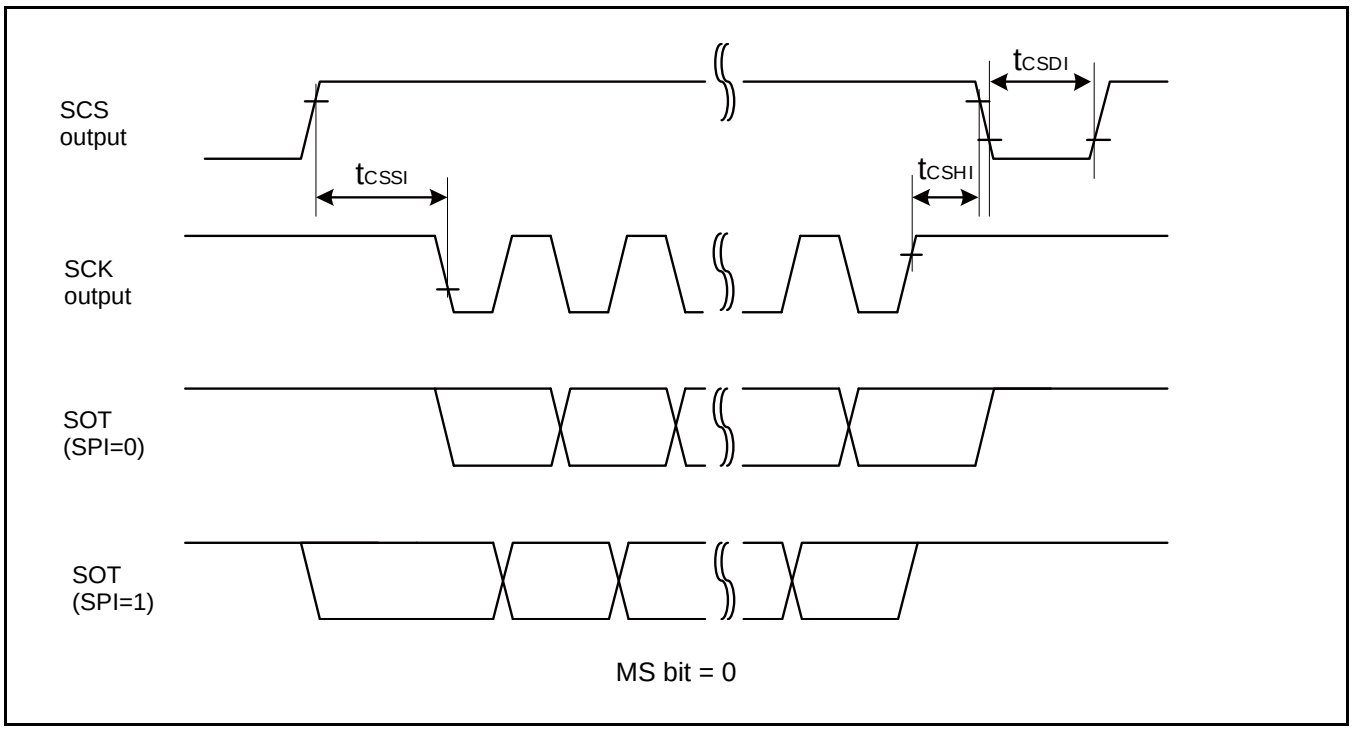




MS bit = 0



MS bit = 1



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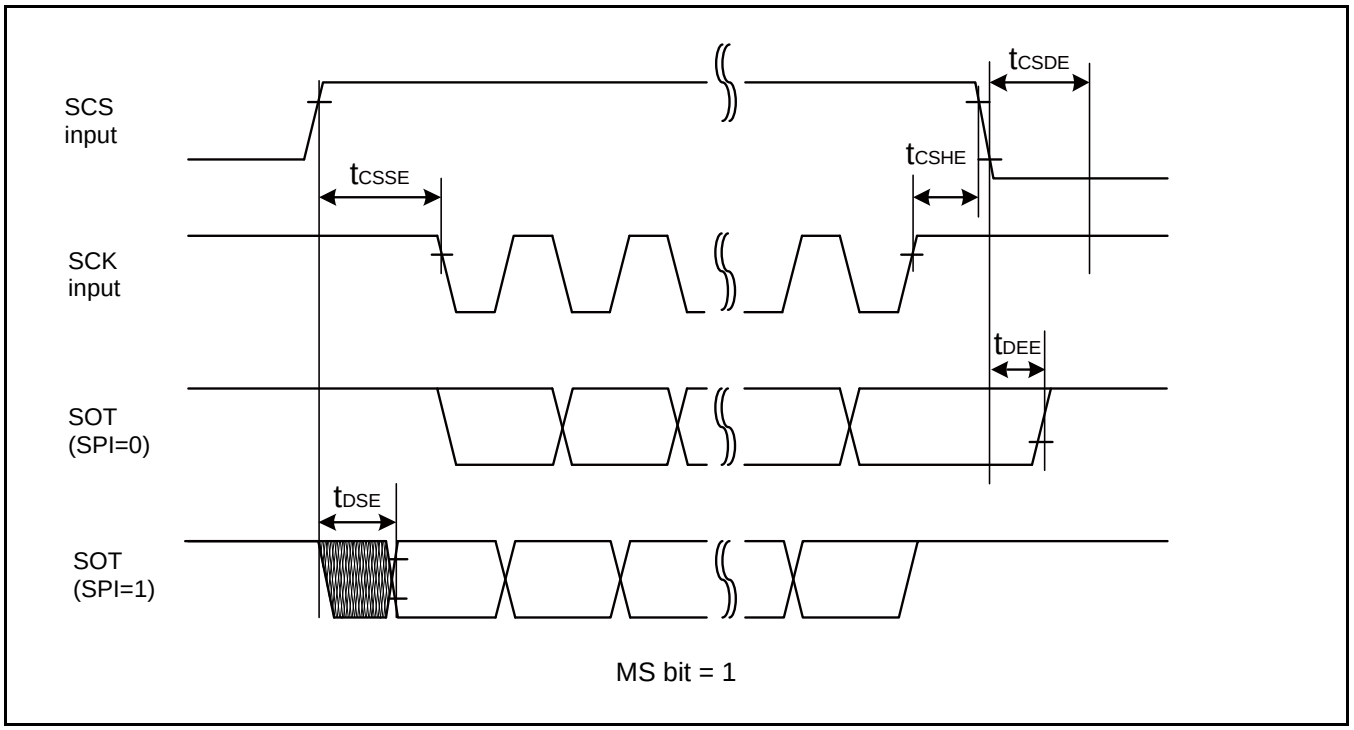
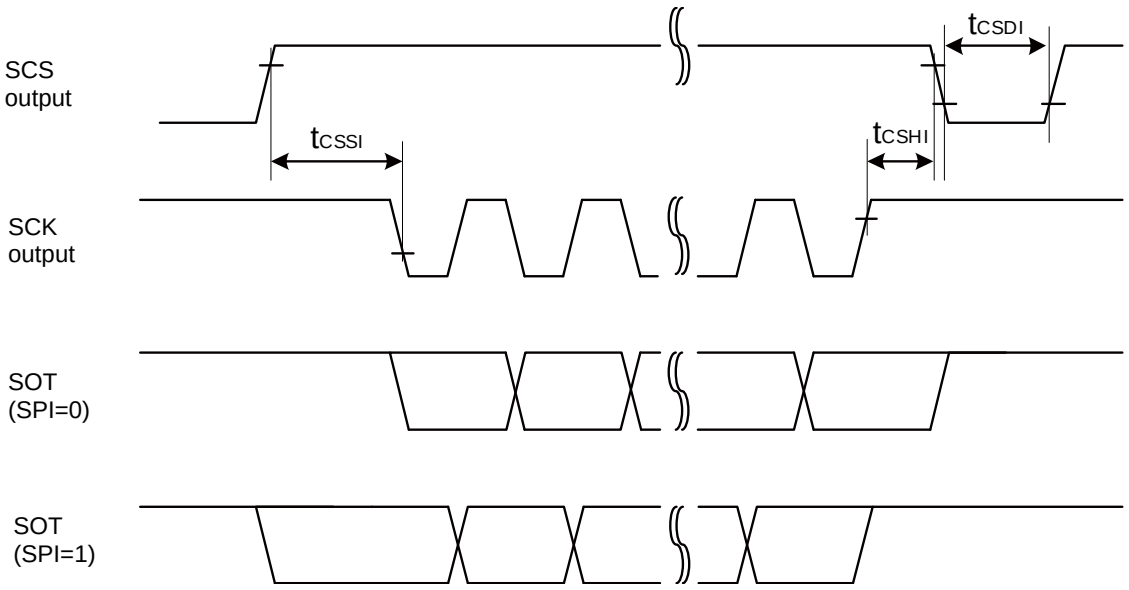
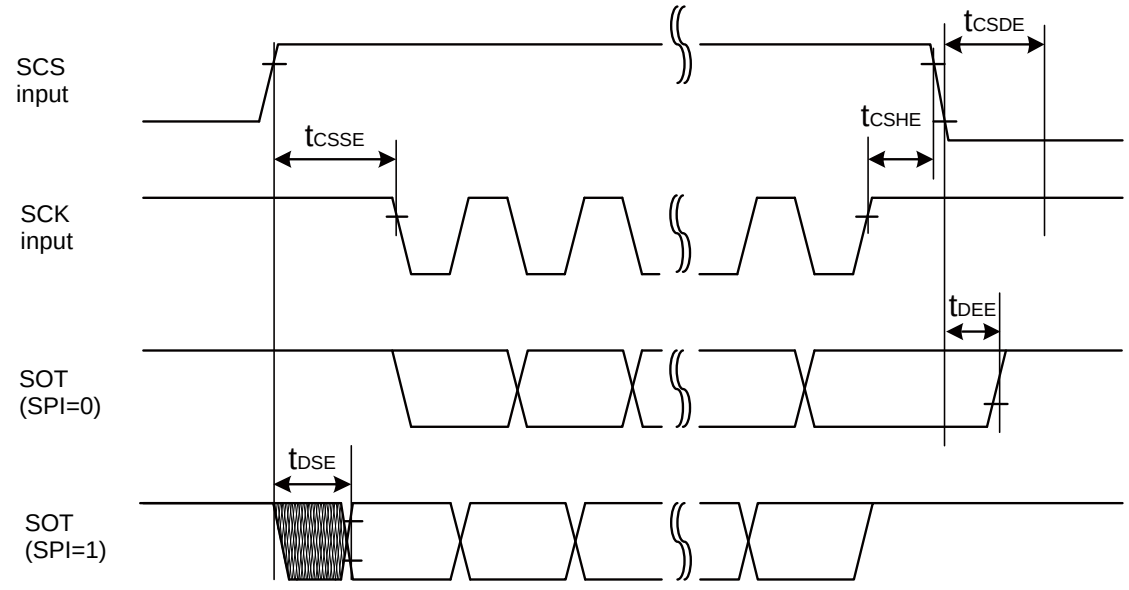


MS bit = 1



MS bit = 0



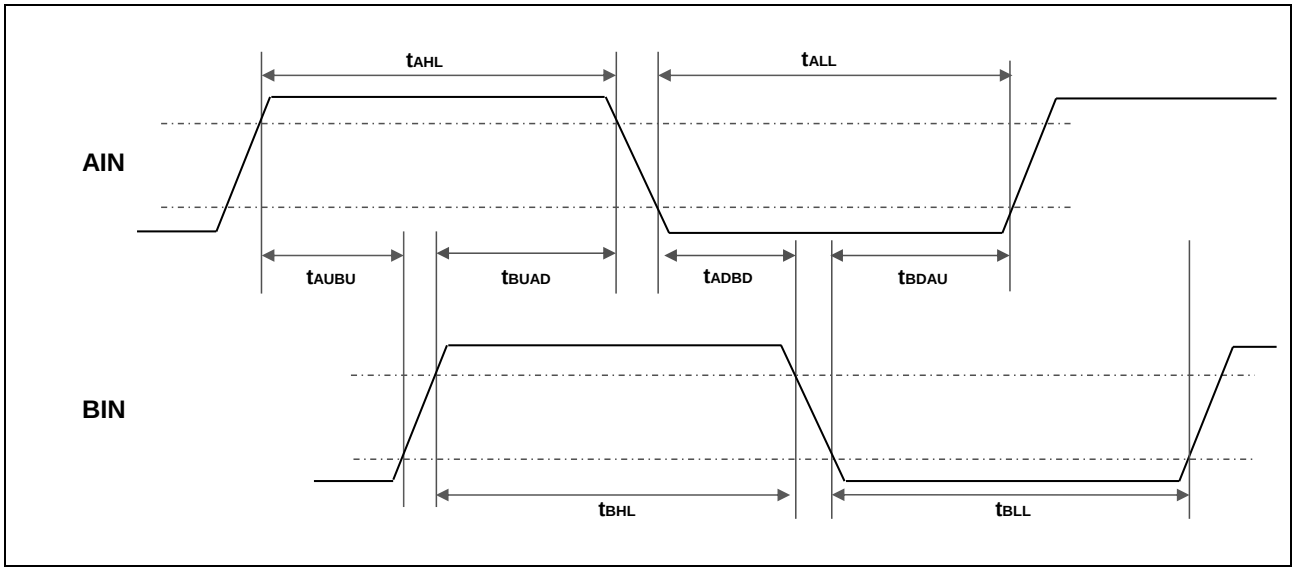
MS bit = 1

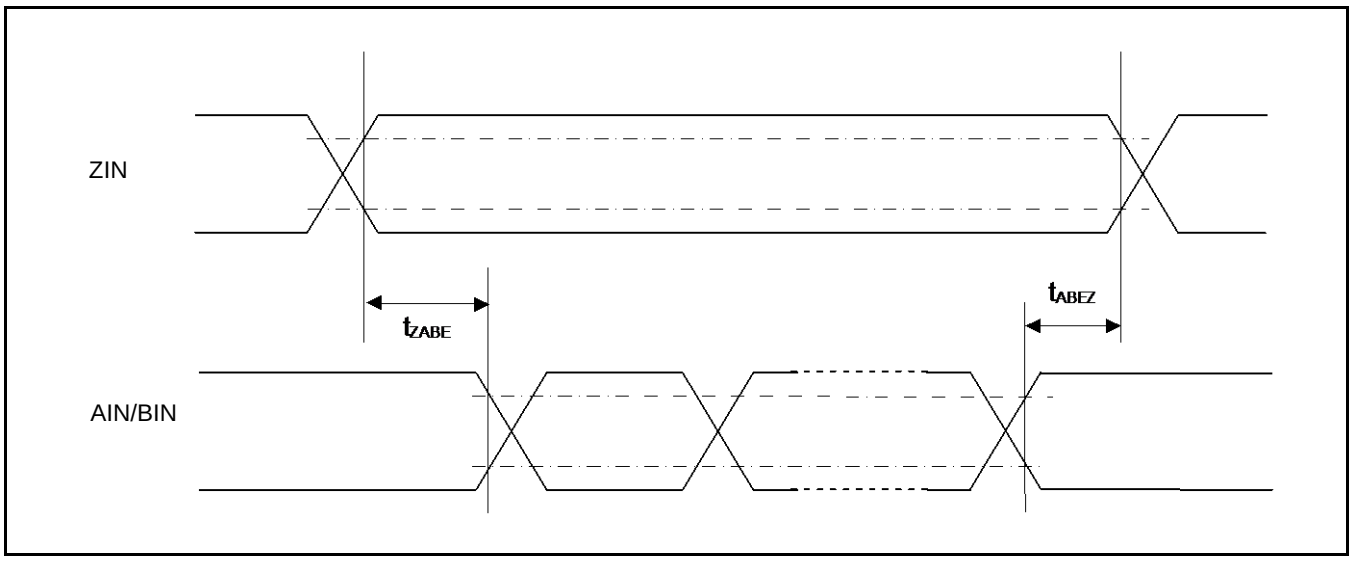
12.4.14 Quadrature Position/Revolution Counter Timing

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Conditions	Value		Unit
			Min	Max	
AIN pin H width	t_{AHL}	-	$2t_{CYCP}$*	-	ns
AIN pin L width	t_{ALL}	-			
BIN pin H width	t_{BHL}	-			
BIN pin L width	t_{BLL}	-			
BIN rising time from AIN pin H level	t_{AUBU}	PC_Mode2 or PC_Mode3			
AIN falling time from BIN pin H level	t_{BUAD}	PC_Mode2 or PC_Mode3			
BIN falling time from AIN pin L level	t_{ADBD}	PC_Mode2 or PC_Mode3			
AIN rising time from BIN pin L level	t_{BDAU}	PC_Mode2 or PC_Mode3			
AIN rising time from BIN pin H level	t_{BUAU}	PC_Mode2 or PC_Mode3			
BIN falling time from AIN pin H level	t_{AUBD}	PC_Mode2 or PC_Mode3			
AIN falling time from BIN pin L level	t_{BDAD}	PC_Mode2 or PC_Mode3			
BIN rising time from AIN pin L level	t_{ADBU}	PC_Mode2 or PC_Mode3			
ZIN pin H width	t_{ZHL}	QCR:CGSC=0			
ZIN pin L width	t_{ZLL}	QCR:CGSC=0			
AIN/BIN rising and falling time from determined ZIN level	t_{ZABE}	QCR:CGSC=1			
Determined ZIN level from AIN/BIN rising and falling time	t_{ABEZ}	QCR:CGSC=1			

*: t_{CYCP} indicates the APB bus clock cycle time except when in Stop mode, in timer mode.
About the APB bus number which Quadrature Position/Revolution Counter is connected to, see 8. Block Diagram in this data sheet.




ZIN
AIN/BIN
tZABE
tABEZ

Slave Mode Timing

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input frequency	t_{SCYC}	I2SCK	-	-	12.288	MHz	
Input clock pulse width	t_{SHW}	I2SCK	-	45	55	%	
	t_{SLW}			45	55	%	
I2SWS→I2SCK Setup time	t_{SFI}	I2SCK, I2SWS	-	8	-	ns	
I2SWS→I2SCK Hold time	t_{HFI}	I2SCK, I2SWS	-	0	-	ns	
I2SCK↑→I2SDO Delay time*1	t_{DDO}	I2SCK, I2SDO	-	0	32	ns	
I2SCK↑→I2SDO Delay Time*2	t_{DFB1}		-	0	32	ns	
I2SDI→I2SCK↓ Setup time	t_{SDI}	I2SCK, I2SDI	-	8	-	ns	
I2SDI→I2SCK↓ Hold time	t_{HDI}		-	0	-	ns	
Input signal rising time	t_{RI}	I2SCK, I2SWS,I2SDI	-	-	5	ns	
Input signal falling time	t_{FI}		-	-	5	ns	

*1: Except for the first bit of transmission frame

*2: When FSPH register 1.

Notes:

- *When the external load capacitance C_L = 20 pF*
- *When I2SWS=48 kHz, I2MCLK=256 × I2SWS*
  Frame synchronization signal (I2SWS) is settable to 48 kHz, 32 kHz, 16 kHz.
  See Chapter 7-2: I^2S(Inter-IC Sound bus)Interface in FM4 Family Peripheral Manual Communication part (002-04862) for the details.

12.5 12-bit A/D Converter

Electrical Characteristics for the A/D Converter

(V_{CC} = AV_{CC} = 2.7V to 3.6V, V_{SS} = AV_{SS} = AVRL = 0V)

Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	12	bit	
Integral Nonlinearity	-	-	-	-	± 4.5	LSB	AVRH=2.7 V to 3.6 V Offset calibration when used
Differential Nonlinearity	-	-	-	-	± 2.5	LSB	
Zero transition voltage	V_{ZT}	ANxx	-	± 2	± 7	LSB	
Full-scale transition voltage	V_{FST}	ANxx	-	AVRH ± 2	AVRH ± 7	LSB	
Total error	-	-	-	± 3	± 8	LSB	
Conversion time	-	-	1.0*1	-	-	µs	
Sampling time *2	t_S	-	0.3	-	10	µs	
Compare clock cycle*3	t_{CCK}	-	50	-	1000	ns	
State transition time to operation permission	t_{STT}	-	-	-	1.0	µs	
Power supply current (analog + digital)	-	AV_{CC}	-	0.30	0.45	mA	A/D 1unit operation
			-	0.1	9.5	µA	When A/D stop
Reference power supply current(AVRH)	-	AVRH	-	0.66	1.18	mA	A/D 1unit operation AVRH=3.3 V
			-	0.2	3.2	µA	When A/D stop
Analog input capacity	C_{AIN}	-	-	-	12.05	pF	
Analog input resistance	R_{AIN}	-	-	-	1.8	kΩ	
Interchannel disparity	-	-	-	-	4	LSB	
Analog port input leak current	-	ANxx	-	-	5	µA	
Analog input voltage	-	ANxx	AV_{SS}	-	AVRH	V	
			AV_{SS}	-	AV_{CC}	V	
Reference voltage	-	AVRH	2.7	-	AV_{CC}	V	t_{CCK} ≥ 50 ns
	-	AVRL	AV_{SS}	-	AV_{SS}	V	

*1: The conversion time is the value of sampling time (t_S) + compare time (t_C).

Ensure that it satisfies the value of sampling time (t_S) and compare clock cycle (t_{CCK}).

For setting of sampling time and compare clock cycle, see Chapter 1-1: A/D Converter in FM4 Family Peripheral Manual Analog Macro Part (002-04860). The register setting of the A/D converter is reflected by the APB bus clock timing.

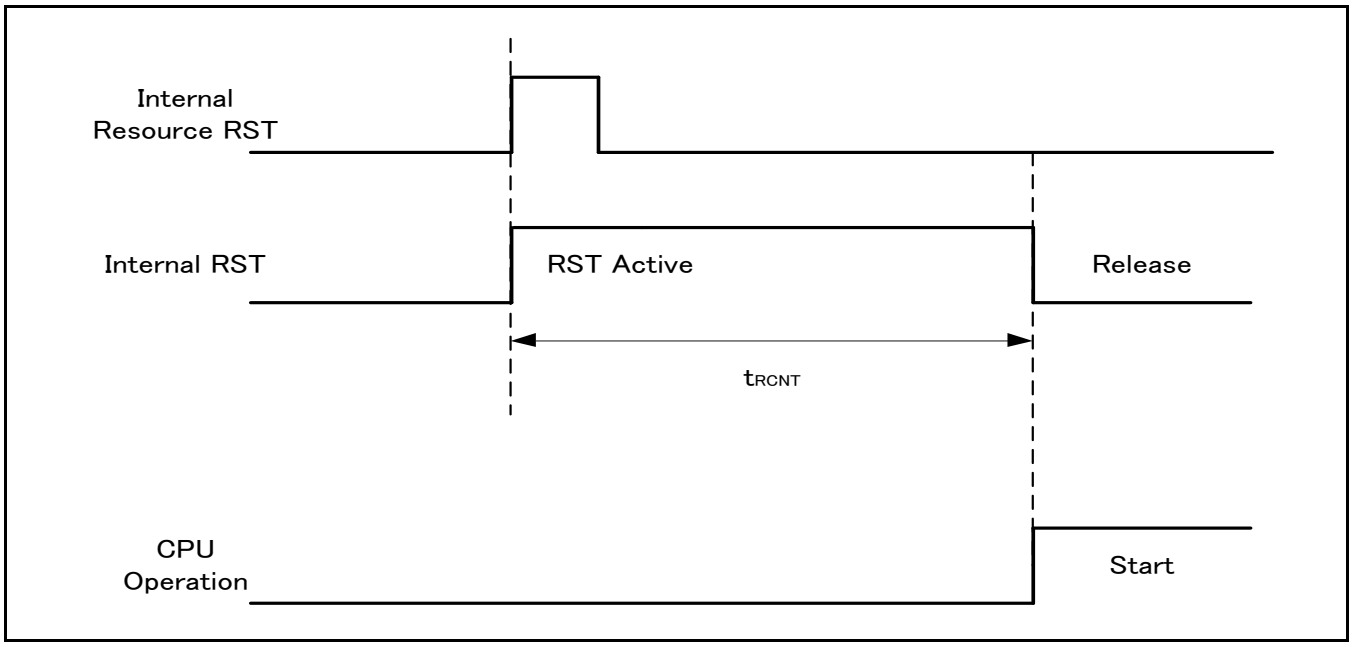
For more information about the APB bus signal to which the A/D converter is connected, see 10. Block Diagram in this data sheet.

The sampling clock and compare clock are set at base clock (HCLK).

*2: A necessary sampling time changes by external impedance. Ensure that it set the sampling time to satisfy (Equation 1).

*3: The compare time (t_C) is the value of (Equation 2).

Example of Standby Recovery Operation (when in Internal Resource Reset Recovery*)



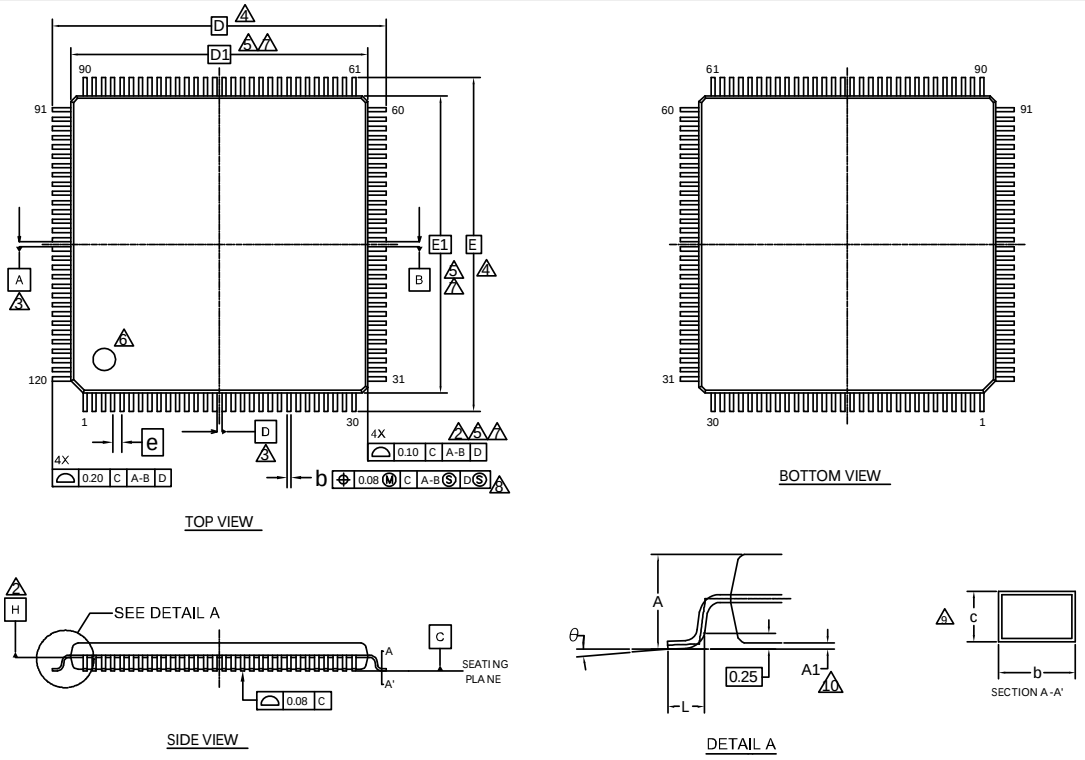
*: Depending on the Low-Power consumption mode, the reset issue from the internal resource is not included in the recovery cause.

Notes:

- *The return factor is different in each low power consumption mode.*
  See Chapter 6: The return factor from each low power consumption modes in "FM4 Family Peripheral Manual Main Part (002-04856).
- *The recovery process is unique for each operating mode. See Chapter 6: Low Power Consumption mode in FM4 Family Peripheral Manual Main Part (002-04856)*
- *When the power-on reset/low-voltage detection reset, they are not included in the return factor. See 12.4.8 Power-on Reset Timing.*
- *In recovering from reset, CPU changes to High-speed Run mode. In the case of using the main clock and PLL clock, they need further main clock oscillation stabilization wait time and oscillation stabilization wait time of Main PLL clock.*
- *Internal resource reset indicates Watchdog reset and CSV reset.*

14. Package Dimensions

Package Type	Package Code
LQFP 120	LQM 120



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.05	—	0.15
b	0.17	0.22	0.27
c	0.115	—	0.195
D	18.00 BSC		
D1	16.00 BSC		
e	0.50 BSC		
E	18.00 BSC		
E1	16.00 BSC		
L	0.45	0.60	0.75
θ	0°	—	8°

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
11. JEDEC SPECIFICATION NO. REF: N/A.

002-16172 **

PACKAGE OUTLINE, 120 LEAD LQFP
18.0X18.0X1.7 MM LQM120 REV**