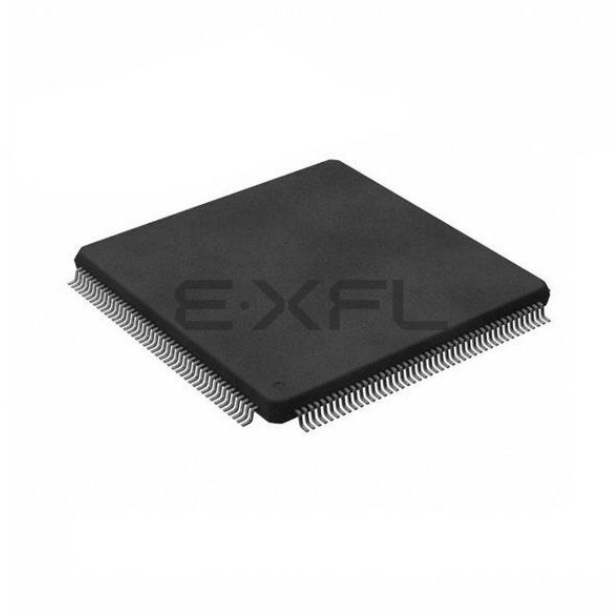


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	160MHz
Connectivity	CSIO, EBI/EMI, I²C, LINbus, SD, SPI, UART/USART, USB
Peripherals	DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	154
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	36K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 24x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e2df5j0agv2000a

CAN-FD Interface (One channel)

- Compatible with CAN Specification 2.0A/B
- Maximum transfer rate: 5 Mbps
- Message buffer for receiver: Up to 192 messages
- Message buffer for transmitter: Up to 32 messages
- CAN with flexible data rate (non-ISO CAN FD)
- Notes:
  - CAN FD cannot communicate between non-ISO CAN FD and ISO CAN FD, because non-ISO CAN FD and ISO CAN FD are different frame format.
  - About the problem of "non-ISO CAN FD", see the White Paper from CiA(CAN in Automation).
  - http://www.can-newsletter.org/engineering/standardization/141222_can-fd-and-crc-issued_white-paper_bosch

Multi-function Serial Interface (Max eight channels)

- 64 bytes with FIFO (the FIFO step numbers vary depending on the settings of the communication mode or bit length.)
- Operation mode is selectable from the following for each channel.
  - UART
  - CSIO
  - LIN
  - I^2C
- UART
  - Full-duplex double buffer
  - Selection with or without parity supported
  - Built-in dedicated baud rate generator
  - External clock available as a serial clock
  - Various error detect functions available (parity errors, framing errors, and overrun errors)
- CSIO
  - Full-duplex double buffer
  - Built-in dedicated baud rate generator
  - Overrun error detect function available
  - Serial chip select function (ch.6 and ch.7 only)
  - Supports High-speed SPI (ch.6 only)
  - Data length 5 to 16-bit
- LIN
  - LIN protocol Rev.2.1 supported
  - Full-duplex double buffer
  - Master/Slave mode supported
  - LIN break field generation (can change to 13 to 16-bit length)
  - LIN break delimiter generation (can change to 1 to 4-bit length)
  - Various error detect functions available (parity errors, framing errors, and overrun errors)
- I^2C
  - Standard mode (Max 100 kbps) / Fast mode (Max 400 kbps) supported
  - Fast mode Plus (Fm+) (Max 1000 kbps, only for ch.4=ch.A) supported

DMA Controller (Eight channels)

The DMA controller has an independent bus for the CPU, so the CPU and the DMA controller can process simultaneously.

- 8 independently configured and operated channels
- Transfer can be started by software or requested from the built-in peripherals
- Transfer address area: 32-bit (4 Gbytes)
- Transfer mode: Block transfer/Burst transfer/Demand transfer
- Transfer data type: bytes/half-word/word
- Transfer block count: 1 to 16
- Number of transfers: 1 to 65536

DSTC (Descriptor System Data Transfer Controller) (128 channels)

The DSTC can transfer data at high-speed without going via the CPU. The DSTC adopts the descriptor system and, following the specified contents of the descriptor that has already been constructed on the memory, can directly access the memory/peripheral device and performs the data transfer operation.

It supports the software activation, the hardware activation, and the chain activation functions.

A/D Converter (Max 24 channels)

- 12-bit A/D Converter
  - Successive Approximation type
  - Built-in 2 units
  - Conversion time: 1.0 µs @ 3.3 V
  - Priority conversion available (priority at two levels)
  - Scanning conversion mode
  - Built-in FIFO for conversion data storage (for SCAN conversion: 16 steps, for priority conversion: four steps)

Base Timer (Max eight channels)

Operation mode is selectable from the followings for each channel.

- 16-bit PWM timer
- 16-bit PPG timer
- 16-/32-bit reload timer
- 16-/32-bit PWC timer

General-Purpose I/O Port

This series can use its pins as general-purpose I/O ports when they are not used for external bus or peripherals. Moreover, the port relocate function is built in. It can set to which I/O port the peripheral function can be allocated.

- Capable of pull-up control per pin
- Capable of reading pin level directly
- Built-in port relocate function
- Up to 98 general-purpose I/O ports @ 120-pin package
- Some I/O pins are 5V tolerant.
  See "4. Pin Descriptions" and "5. I/O Circuit Type" for the corresponding pins.

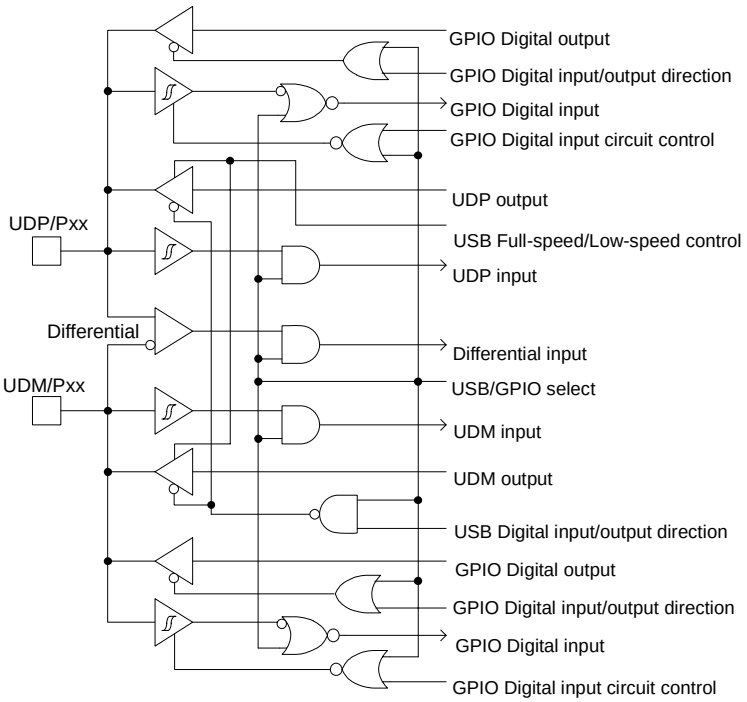
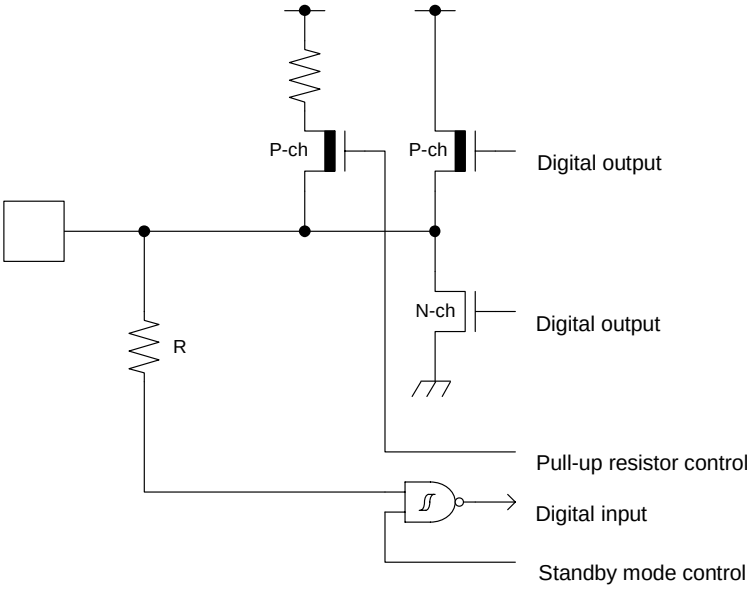
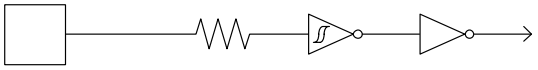
Pin No.				Pin name	I/O circuit type	Pin state type
LQFP176	LQFP120 Ex-LQFP120	LQFP120 (S6E2D55GJA)	FBGA161			
9	5	5	D2	P3E SOT7_0 (SDA7_0) TIOA3_1 INT07_1 I2SDI0_0 RTO03_0 (PPG02_0) MAD07_0	G	K
10	6	6	D1	P3F SCK7_0 (SCL7_0) TIOA4_1 I2SCK0_0 RTO04_0 (PPG04_0) MAD06_0	G	I
11	7	7	D4	P7C TIOA5_1 RTO05_0 (PPG04_0) MWEX_0	G	I
12	8	–	E4	P7B ADTG_2 GE_HBCSX1 MOEX_0	K	I
–	–	8	–	P7B ADTG_2 MOEX_0	K	I
13	–	–	–	PA8 GE_SDDQ29	L	I
14	–	–	–	PA9 GE_SDDQ28	L	I
15	–	–	–	PAA GE_SDDQ27	L	I
16	–	–	–	PAB GE_SDDQ26	L	I
17	–	–	–	PAC GE_SDDQ25	L	I
18	–	–	–	PAD GE_SDDQ24	L	I

Module	Pin Name	Function	Pin No.			
			LQFP176	LQFP120 Ex-LQFP120	LQFP120 (S6E2D55GJA)	FBGA161
I^2S 0	I2SMCLK0_0	I^2S ch.0 external clock pin	6	2	2	C3
	I2SDO0_0	I^2S ch.0 serial transition data output pin	7	3	3	C2
	I2SWS0_0	I^2S ch.0 frame synchronization signal pin	8	4	4	D3
	I2SDI0_0	I^2S ch.0 serial received data input pin	9	5	5	D2
	I2SCK0_0	I^2S ch.0 bit clock pin	10	6	6	D1
I^2S 1	I2SMCLK1_0	I^2S ch.1 external clock pin	51	33	33	M3
	I2SDO1_0	I^2S ch.1 serial transition data output pin	52	34	34	L4
	I2SWS1_0	I^2S ch.1 frame synchronization signal pin	53	35	35	M4
	I2SDI1_0	I^2S ch.1 serial received data input pin	54	36	36	K5
	I2SCK1_0	I^2S ch.1 bit clock pin	55	37	37	L5
GDC High-Speed Quad SPI	GE_SPCK	SPI clock output pin	34	20	-	J1
	GE_SPDQ0	SPI data input / output pin	35	21	-	K1
	GE_SPDQ1		38	24	-	J2
	GE_SPDQ2		39	25	-	J3
	GE_SPDQ3		36	22	-	H2
	GE_SPCSX0	SPI chip select output pin	37	23	-	H3
GDC HyperBus I/F	GE_HBCK	HBI clock output pin	34	20	-	J1
	GE_HBDQ0	HBI data input / output pin	36	22	-	H2
	GE_HBDQ1		37	23	-	H3
	GE_HBDQ2		38	24	-	J2
	GE_HBDQ3		39	25	-	J3
	GE_HBDQ4		40	26	-	K2
	GE_HBDQ5		41	27	-	K3
	GE_HBDQ6		42	28	-	L2
	GE_HBDQ7		43	29	-	L3
	GE_HBCSX0	HBI chip select output pin	35	21	-	K1
	GE_HBCSX1		12	8	-	E4
	GE_HBRWDS	HBI RWDS input / output pin	33	19	-	G2
	GE_HBRESETX	HBI hardware reset output pin	25	15	-	F3
	GE_HBINTX	HBI interrupt input pin	26	16	-	F2
	GE_HBRSTOX	HBI reset input pin	27	17	-	F1
	GE_HBWPX	HBI write protect output pin	28	18	-	G3

Module	Pin Name	Function	Pin No.			
			LQFP176	LQFP120 Ex-LQFP120	LQFP120 (S6E2D55GJA)	FBGA161
VBAT Power	VBAT	VBAT power supply pin. Backup power supply (battery etc.) and system power supply.	81	53	53	M9
Analog GND	AVSS	A/D converter GND pin	91	63	63	K12
C Pin	C	Power supply stabilization capacity pin	60	38	38	N2

Note:

- *While this device contains a Test Access Port (TAP) based on the IEEE 1149.1-2001 JTAG standard, it is not fully compliant to all requirements of that standard. This device may contain a 32-bit device ID that is the same as the 32-bit device ID in other devices with different functionality. The TAP pins may also be configurable for purposes other than access to the TAP controller.*

Type	Circuit	Remarks
H		It is possible to select the USB I/O / GPIO function. When the USB I/O is selected. ・Full-speed, Low-speed control When the GPIO is selected. ・CMOS level output ・CMOS level hysteresis input ・With standby mode control ・I_{OH} = -20.5 mA, I_{OL} = 18.5 mA
I		・CMOS level output ・CMOS level hysteresis input ・5 V tolerant ・With pull-up resistor control ・With standby mode control ・Pull-up resistor : Approximately 80 kΩ ・I_{OH} = -2 mA, I_{OL} = 2 mA ・Available to control of PZR registers.
J		・CMOS level hysteresis input

12.3 DC Characteristics

12.3.1 Current Rating

Table 12-2 Typical and Maximum Current Consumption in Normal Operation (PLL), Code Running from Flash Memory (Flash Accelerator Mode and Trace Buffer Function Enabled)

Parameter	Symbol	Pin Name	Conditions		Frequency*4 (MHz)	Value		Unit	Remarks
						Typ*1	Max*2		
Power supply current	I_{CC}	VCC	Normal operation *6,*7 (PLL)	*5	160 MHz	182	279	mA	*3 When all peripheral clocks are ON GDC clock 160 MHz
					144 MHz	176	270	mA	
					120 MHz	167	256	mA	
					100 MHz	159	244	mA	
					80 MHz	151	233	mA	
					60 MHz	143	221	mA	
					40 MHz	136	210	mA	
					20 MHz	128	199	mA	
					8 MHz	123	191	mA	
					4 MHz	122	190	mA	
			Normal operation , *6,*7 (PLL)	*5	160 MHz	43	117	mA	*3 When all peripheral clocks are OFF
					144 MHz	39	112	mA	
					120 MHz	34	106	mA	
					100 MHz	29	100	mA	
					80 MHz	24	95	mA	
					60 MHz	20	90	mA	
					40 MHz	15	84	mA	
					20 MHz	10	78	mA	
					8 MHz	7	74	mA	
					4 MHz	6	73	mA	

*1: T_A=+25°C, V_{CC}=3.3 V

*2: T_J=+125°C, V_{CC}=3.6 V

*3: When all ports are fixed.

*4: Frequency is a value of HCLK. PCLK0=PCLK1=PCLK2=HCLK/2

*5: When operating flash accelerator mode and trace buffer function (FRWTR.RWT = 10, FBFCR.BE = 1)

*6: Data access is nothing to main flash memory and VFLASH memory

*7: When using the crystal oscillator of 4 MHz (including the current consumption of the oscillation circuit)

Table 12-5 Typical and Maximum Current Consumption in Normal Operation (other than PLL), Code with Data Accessing Running from Flash Memory (Flash 0 Wait-cycle Mode and Read Access 0 Wait)

Parameter	Symbol	Pin Name	Conditions		Frequency*4 (MHz)	Value		Unit	Remarks
						Typ*1	Max*2		
Power supply current	I_{CC}	VCC	Normal operation, *6,*8 (built-in High-speed CR)	*5	4 MHz	110	181	mA	*3 When all peripheral clocks are ON GDC clock 160 MHz
						4.1	74	mA	*3 When all peripheral clocks are OFF
			Normal operation , *6,*7,*8 (Sub oscillation)	*5	32 kHz	0.7	76.65	mA	*3 When all peripheral clocks are ON
						0.69	71.65	mA	*3 When all peripheral clocks are OFF
			Normal operation , *6,*8 (built-in Low-speed CR)	*5	100 kHz	0.74	88.65	mA	*3 When all peripheral clocks are ON
						0.73	74.65	mA	*3 When all peripheral clocks are OFF

*1: T_A=+25°C, V_{CC}=3.3 V

*2: T_J=+125°C, V_{CC}=3.6 V

*3: When all ports are fixed.

*4: Frequency is a value of HCLK. PCLK0=PCLK1=PCLK2=HCLK/2

*5: When operating flash 0 wait-cycle mode and read access 0 wait (FRWTR.RWT = 00, FSYNDN.SD = 000)

*6: With data access to a main flash memory.

*7: When using the crystal oscillator of 32 kHz (including the current consumption of the oscillation circuit)

*8: Data access is nothing to VFLASH memory

12.4.4 Operating Conditions of Main PLL (In the Case of Using Main Clock for Input Clock of PLL)

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time*1 (LOCK UP time)	t_{LOCK}	100	-	-	µs	
PLL input clock frequency	f_{PLLI}	4	-	16	MHz	
PLL multiplication rate	-	13	-	100	multiplier	
PLL macro oscillation clock frequency	f_{PLLO}	200	-	400	MHz	
Main PLL clock frequency*2	f_{CLKPLL}	-	-	200	MHz	

*1: Time from when the PLL starts operating until the oscillation stabilizes.

*2: For more information about Main PLL clock (CLKPLL), see Chapter 2-1: Clock in FM4 Family Peripheral Manual Main part (002-04856).

12.4.5 Operating Conditions of USB/I²S/GDC PLL (In the Case of Using Main Clock for Input Clock of PLL)

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time*1 (LOCK UP time)	t_{LOCK}	100	-	-	µs	
PLL input clock frequency	f_{PLLI}	4	-	16	MHz	
PLL multiplication rate	-	13	-	100	multiplier	
PLL macro oscillation clock frequency	f_{PLLO}	200	-	400	MHz	USB/GDC
				384	MHz	I²S
USB clock frequency *2	f_{CLKPLL}	-	-	50	MHz	After the M frequency division
I²S clock frequency *3	f_{CLKPLL}	-	-	12.288	MHz	After the M frequency division
GDC clock frequency *4	f_{CLKPLL}	-	-	160	MHz	After divided by GDC part

*1: Time from when the PLL starts operating until the oscillation stabilizes.

*2: For more information about USB clock, see Chapter 2-2: USB Clock Generation in FM4 Family Peripheral Manual Communication Macro part (002-04862).

*3: For more information about I²S clock, see Chapter 7-1: I²S Clock Generation in FM4 Family Peripheral Manual Communication Macro part (002-04862).

*4: For more information about GDC clock, see FM4 Family Peripheral Manual GDC part (002-04917).

When Using Synchronous Serial Chip Select (SCINV = 1, CSLVL=1)

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Conditions	Value		Unit
			Min	Max	
SCS↓→SCK↑ setup time	t_{CSSI}	Internal shift clock operation	(*1)-50	(*1)+0	ns
SCK↓→SCS↑ hold time	t_{CSHI}		(*2)+0	(*2)+50	ns
SCS deselect time	t_{CSDI}		(*3)-50+5t_{CYCP}	(*3)+50+5t_{CYCP}	ns
SCS↓→SCK↑ setup time	t_{CSSE}	External shift clock operation	3t_{CYCP}+30	-	ns
SCK↓→SCS↑ hold time	t_{CSHE}		0	-	ns
SCS deselect time	t_{CSDE}		3t_{CYCP}+30	-	ns
SCS↓→SOT delay time	t_{DSE}		-	40	ns
SCS↑→SOT delay time	t_{DEE}		0	-	ns

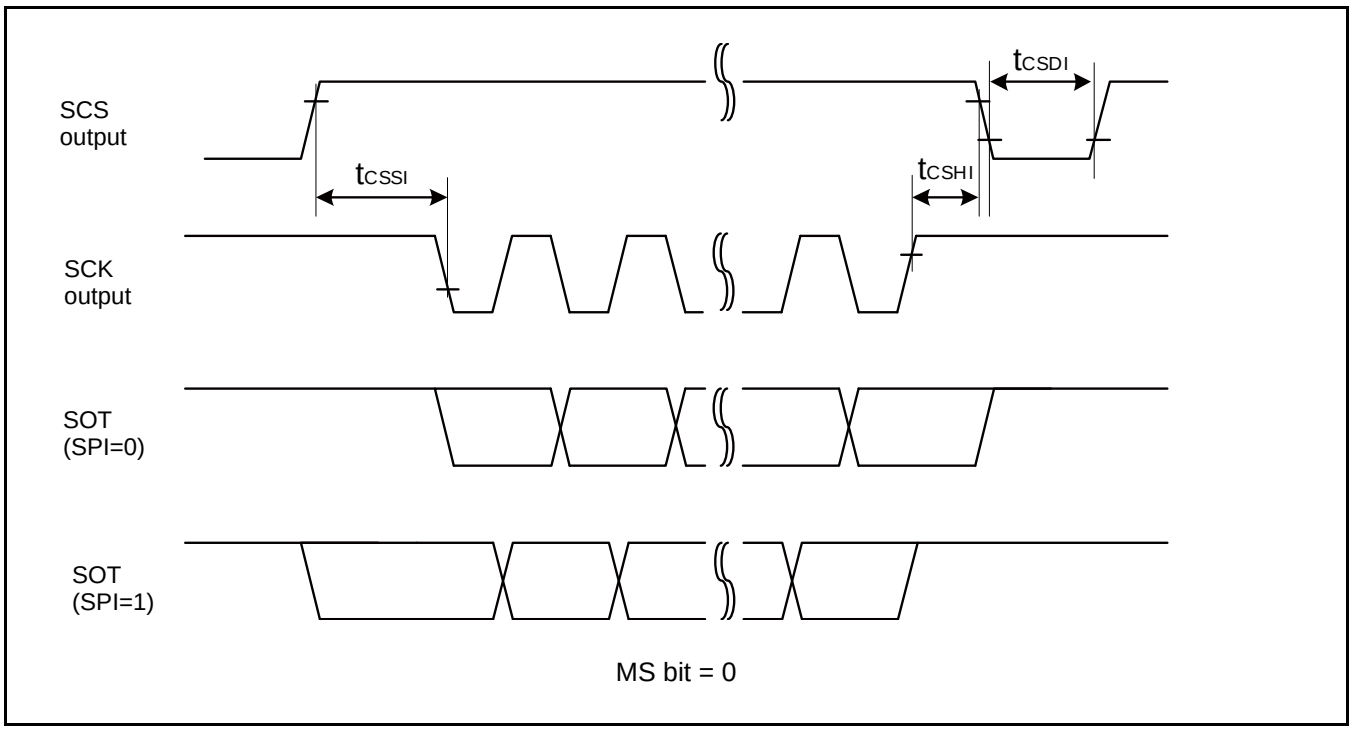
(*1): CSSU bit value×serial chip select timing operating clock cycle [ns]

(*2): CSHD bit value×serial chip select timing operating clock cycle [ns]

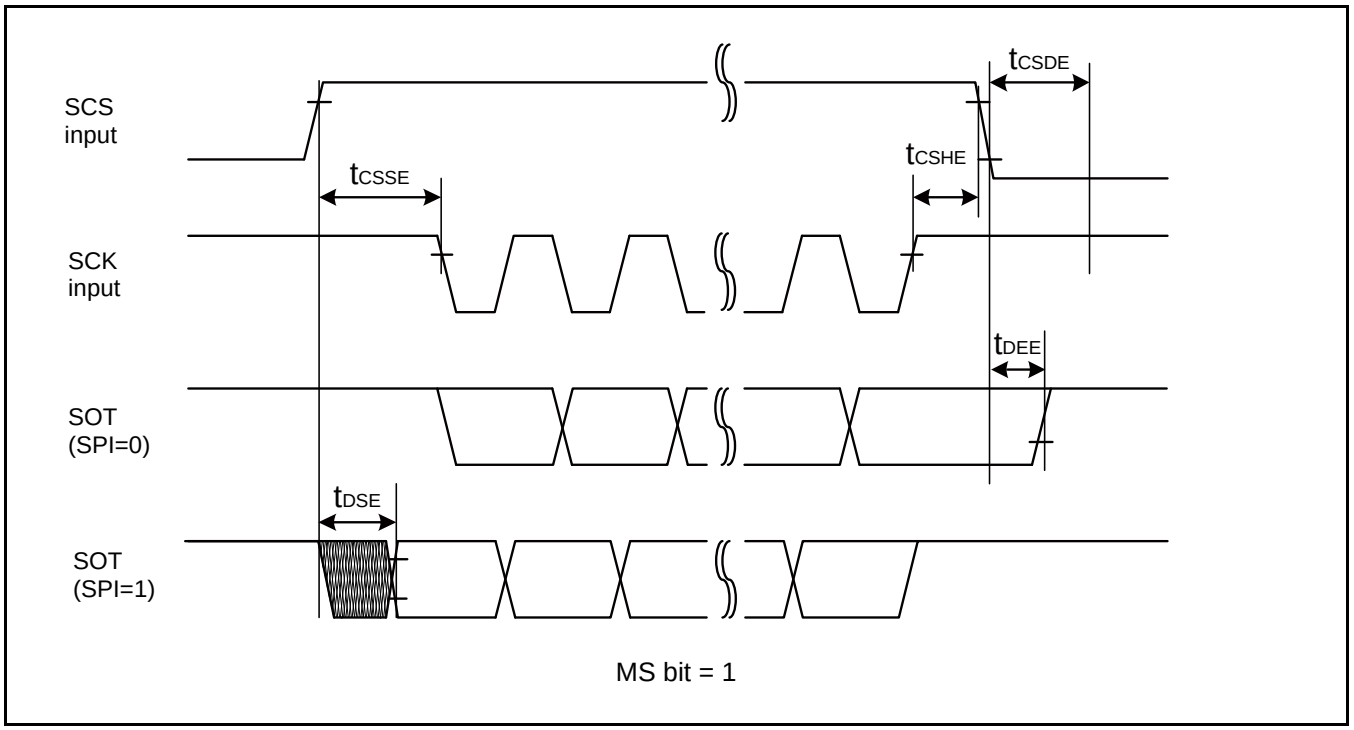
(*3): CSDS bit value×serial chip select timing operating clock cycle [ns]

Notes:

- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which multi-function serial is connected to, see 8. Block Diagram in this data sheet.
- *About CSSU, CSHD, CSDS, serial chip select timing operating clock, see FM4 Family Peripheral Manual Main part (002-04856).*
- *When the external load capacitance C_L = 30 pF.*



MS bit = 0



MS bit = 1

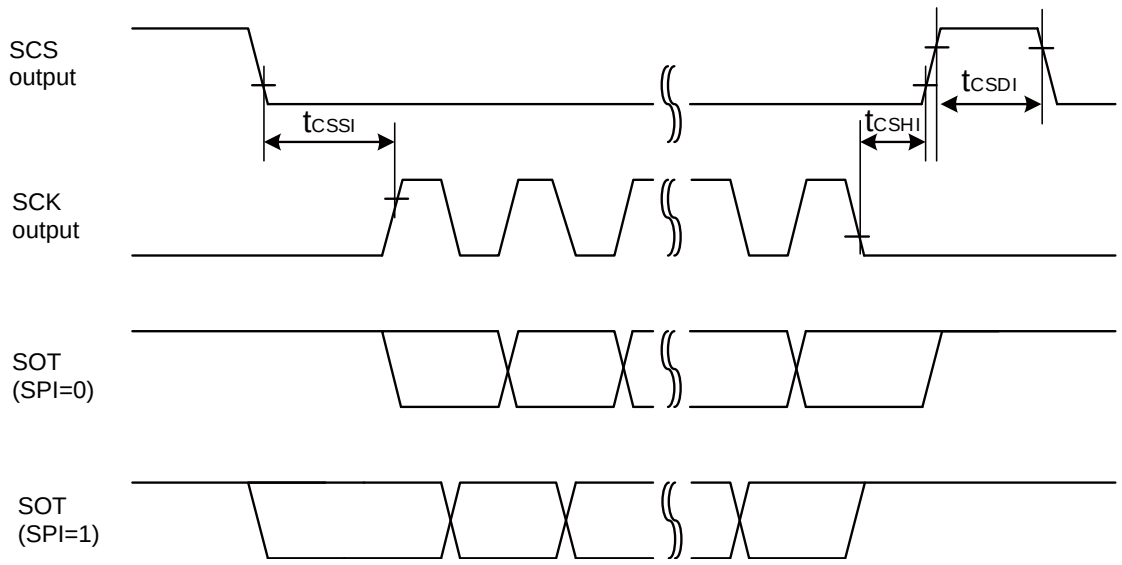
High-Speed Synchronous Serial (SPI = 0, SCINV = 1)

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

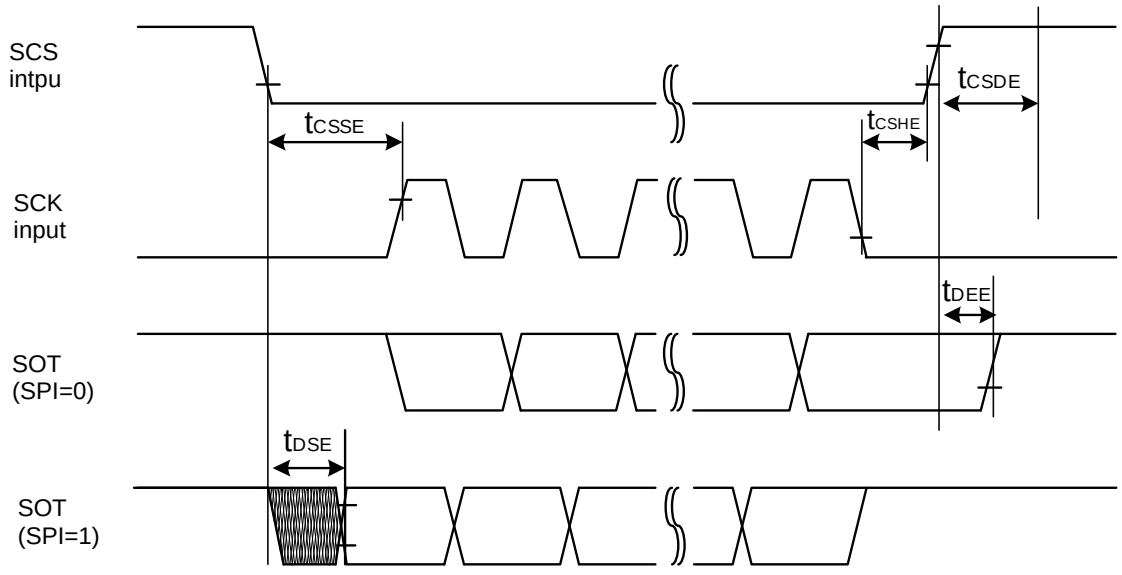
Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	ns
SCK↑→SOT delay time	t_{SHOVI}	SCKx, SOTx		- 10	+ 10	ns
SIN→SCK↓ setup time	t_{IVSLI}	SCKx, SINx		14 12.5*	-	ns
SCK↓→SIN hold time	t_{SLIXI}	SCKx, SINx		5	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ - 5	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	ns
SCK↑→SOT delay time	t_{SHOVE}	SCKx, SOTx		-	15	ns
SIN→SCK↓ setup time	t_{IVSLE}	SCKx, SINx		5	-	ns
SCK↓→SIN hold time	t_{SLIXE}	SCKx, SINx		5	-	ns
SCK falling time	t_F	SCKx		-	5	ns
SCK rising time	t_R	SCKx		-	5	ns

Notes:

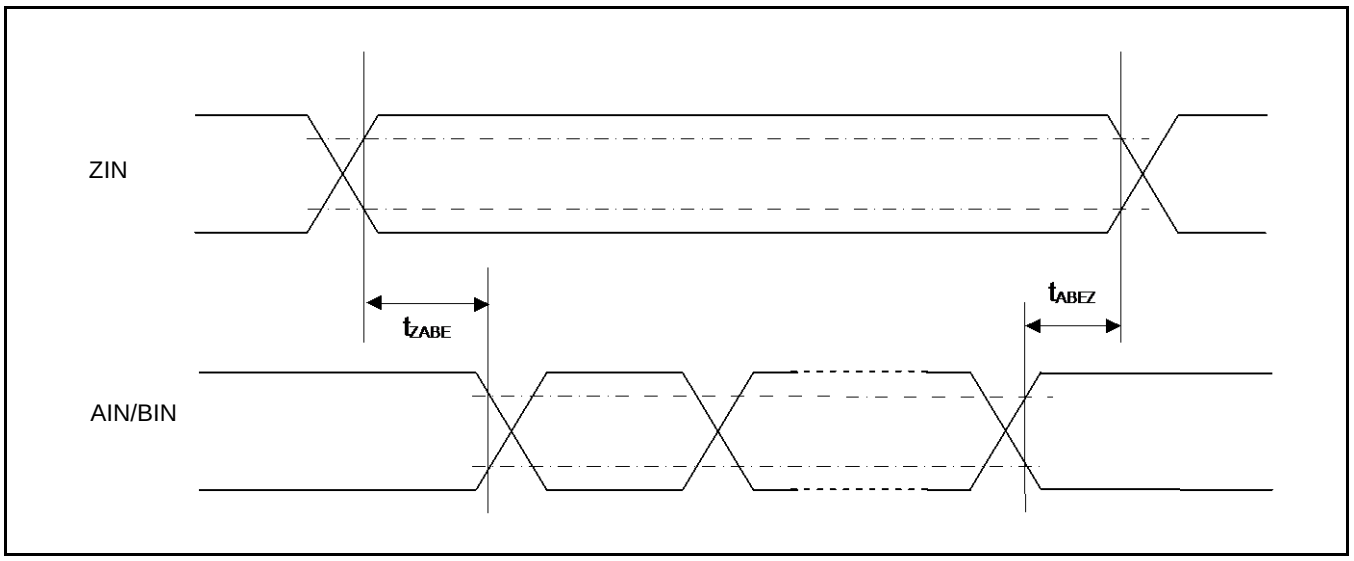
- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which multi-function serial is connected to, see 8. Block Diagram in this data sheet.
- *These characteristics only guarantee the following pins.*
  SIN6_0, SOT6_0, SCK6_0, SCS60_0
- *When the external load capacitance C_L = 30 pF. (For *, when C_L = 10 pF)*



MS bit = 0



MS bit = 1


ZIN
AIN/BIN
tZABE
tABEZ

Fast Mode Plus (Fm+)

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Conditions	Fast Mode Plus (Fm+)*6		Unit	Remarks
			Min	Max		
SCL clock frequency	f_{SCL}	C_L = 30 pF, R = (V_p/I_{OL})*1	0	1000	kHz	
(Repeated) Start condition hold time SDA ↓ → SCL ↓	t_{HDSTA}		0.26	-	µs	
SCL clock L width	t_{LOW}		0.5	-	µs	
SCL clock H width	t_{HIGH}		0.26	-	µs	
(Repeated) Start condition setup time SCL ↑ → SDA ↓	t_{SUSTA}		0.26	-	µs	
Data hold time SCL ↓ → SDA ↓ ↑	t_{HDDAT}		0	0.45*2, *3	µs	
Data setup time SDA ↓ ↑ → SCL ↑	t_{SUDAT}		50	-	ns	
Stop condition setup time SCL ↑ → SDA ↑	t_{SUSTO}		0.26	-	µs	
Bus free time between Stop condition and Start condition	t_{BUF}		0.5	-	µs	
Noise filter	t_{SP}	60 MHz ≤ t_{CYCP} < 80 MHz	6 t_{CYCP}*4	-	ns	*5
		80 MHz ≤ t_{CYCP} ≤100 MHz	8 t_{CYCP}*4	-	ns	

*1: R and C_L represent the pull-up resistance and load capacitance of the SCL and SDA lines, respectively. Vp indicates the power supply voltage of the pull-up resistance and I_{OL} indicates V_{OL} guaranteed current.

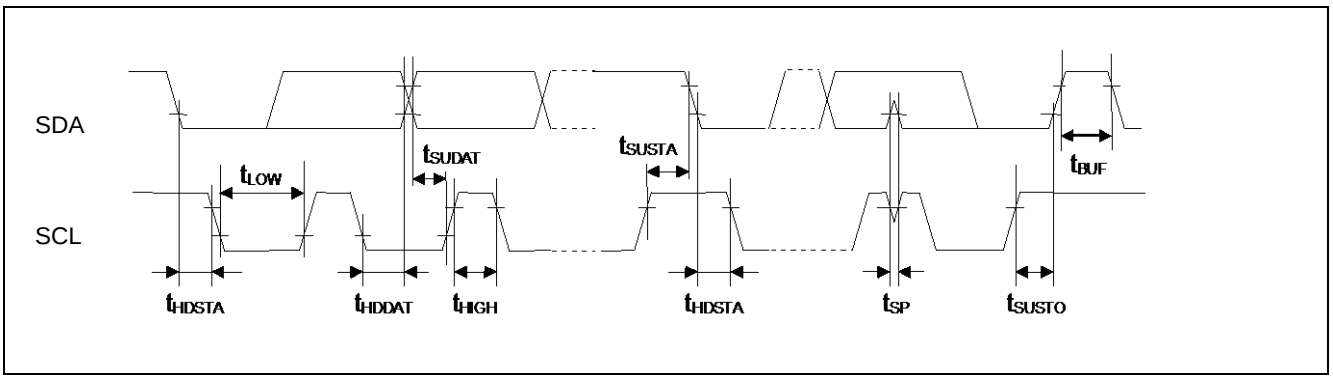
*2: The maximum t_{HDDAT} must satisfy that it does not extend at least L period (t_{LOW}) of device's SCL signal.

*3: A Fast mode I^2C bus device can be used on a Standard mode I^2C bus system as long as the device satisfies the requirement of "t_{SUDAT} ≥ 250 ns".

*4: t_{CYCP} is the APB bus clock cycle time.
About the APB bus number that I^2C is connected to, see 8. Block Diagram in this data sheet.
To use fast mode plus (Fm+), set the peripheral bus clock at 64 MHz or more.

*5: The noise filter time can be changed by register settings.
Change the number of the noise filter steps according to APB bus clock frequency.

*6: When using fast mode plus (Fm+), set the I/O pin to the mode corresponding to I^2C Fm+ in the EPFR register. See Chapter 12 : I/O Port in "FM4 Family Peripheral Manual Main part (002-04856)" for the details.



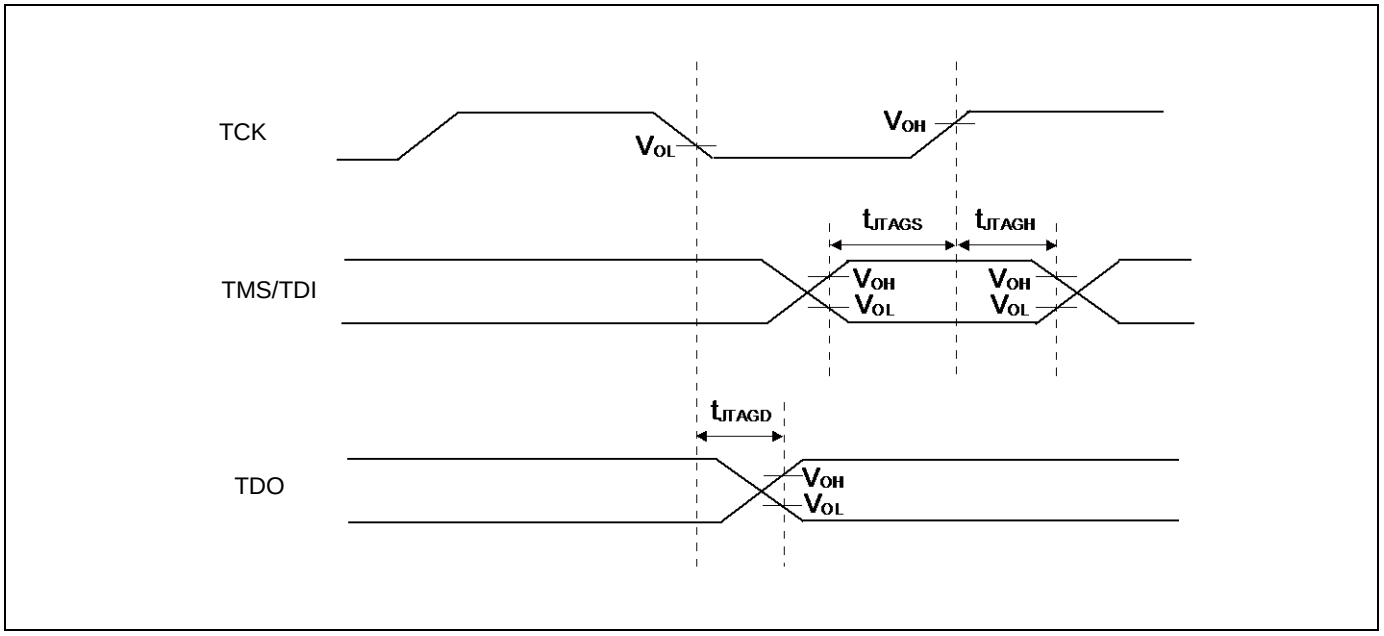
12.4.17 JTAG Timing

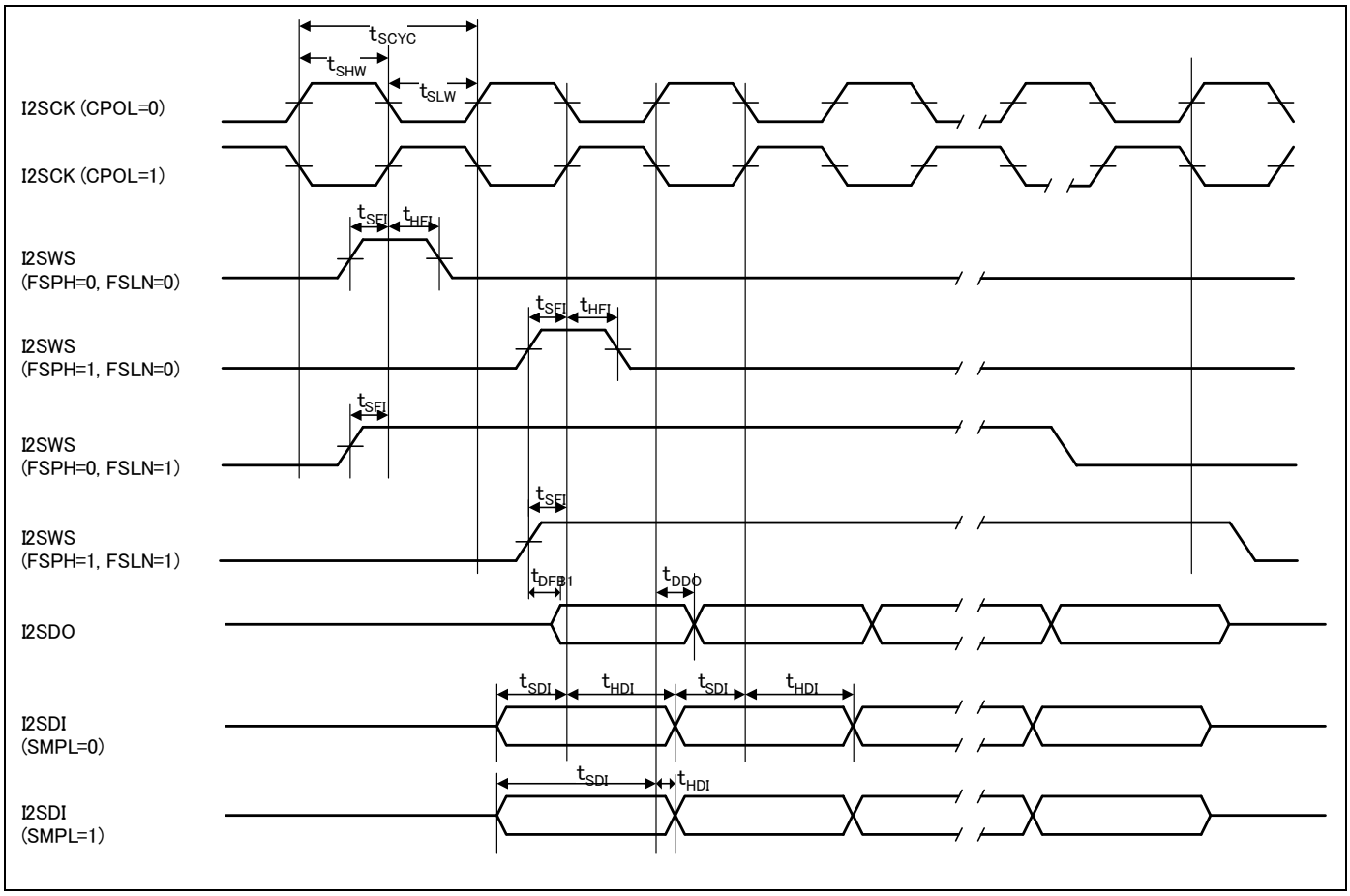
(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
TMS, TDI setup time	t_{JTAGS}	TCK, TMS, TDI	-	15	-	ns	
TMS, TDI hold time	t_{JTAGH}	TCK, TMS, TDI	-	15	-	ns	
TDO delay time	t_{JTAGD}	TCK, TDO	-	-	45	ns	

Note:

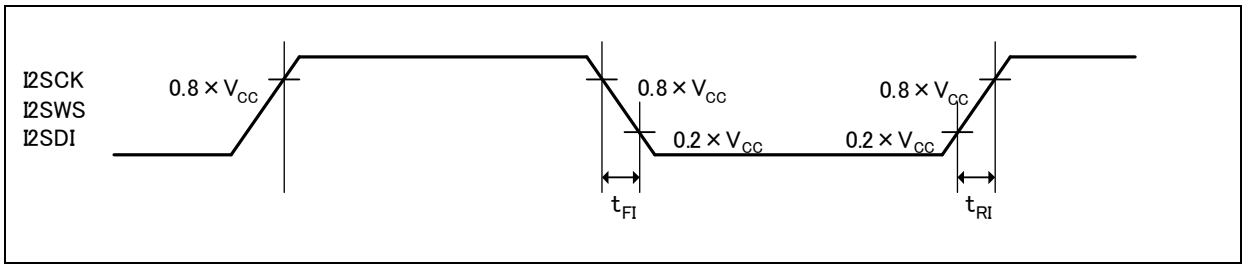
- *When the external load capacitance C_L= 30 pF.*





Notes:

- *See Chapter 7-2: I²S(Inter-IC Sound bus)Interface in FM4 Family Peripheral Manual Communication part (002-04862) for the details of FSPH, FSLN, SMPL*
- *I2SCK input is selectable polarity by CPOL bit of CNTREG register*



12.4.21 GDC: High-Speed Quad SPI Timing

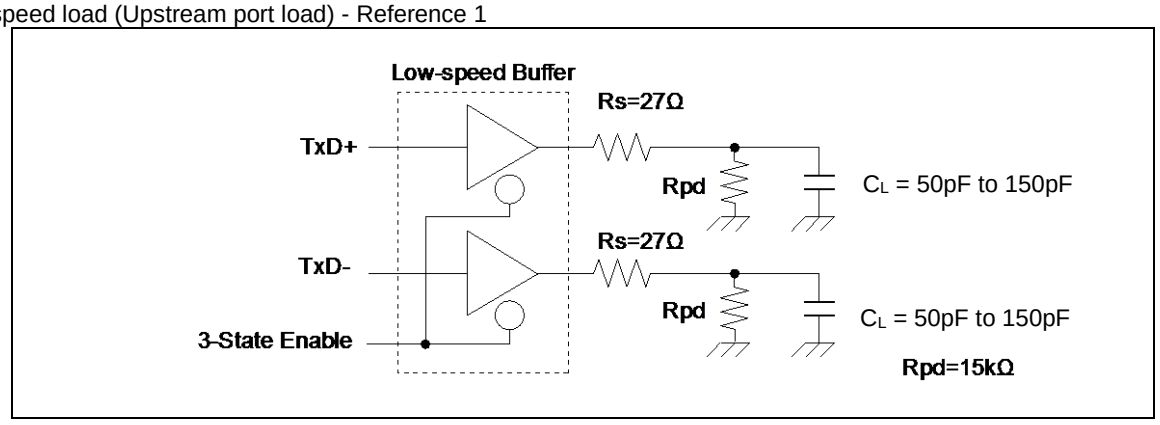
(V_{CC} = 3.0V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Serial clock frequency	t_{SCYCM}	GE_SPCK	C_L=20 pF	-	80	MHz
Enabled CS→ CLK Starting Time (mode0/mode2)	$t_{OSLSK02}$	GE_SPCK, GE_SPCSX0		$1.5 \times t_{SCYCM} - 4.25$	-	ns
Enabled CS→ CLK Starting Time (mode1/mode3)	$t_{OSLSK13}$			$t_{SCYCM} - 4.25$	-	ns
CLK Last→ Disabled CS Time (mode0/mode2)	$t_{OSKSL02}$			t_{SCYCM}	-	ns
CLK Last→ Disabled CS Time (mode1/mode3)	$t_{OSKSL13}$			$1.5 \times t_{SCYCM}$	-	ns
SIO Data output time	t_{OSDAT}	GE_SPCK, GE_SPDQ0, GE_SPDQ1, GE_SPDQ2, GE_SPDQ3		-1.25	4.25	ns
SIO Setup	t_{DSSET}			4	-	ns
SIO Hold	t_{SDHOLD}			$0.5 \times t_{SCYCM}$	-	ns

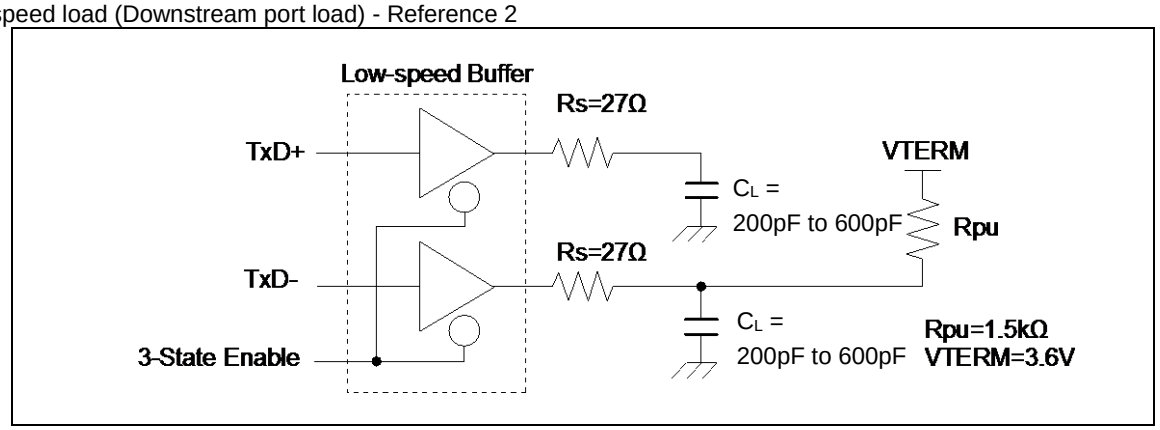
Note:

- *See Chapter 8-3: High-Speed Quad SPI controller in FM4 Family Peripheral Manual Communication part (002-04862) for the detail of RTM mode.*

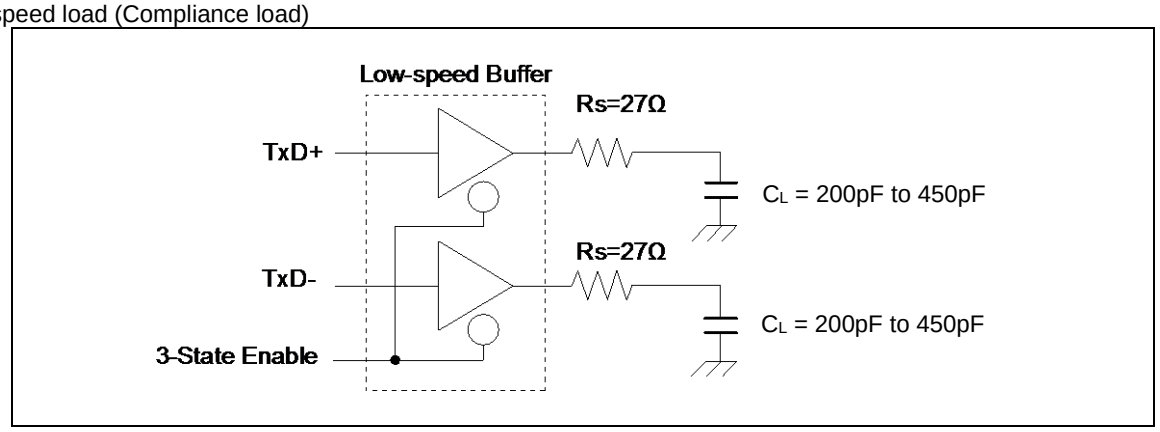
■Low-speed load (Upstream port load) - Reference 1



■Low-speed load (Downstream port load) - Reference 2



■Low-speed load (Compliance load)



12.10.2 Recovery Cause: Reset

The time from reset release to the program operation start is shown.

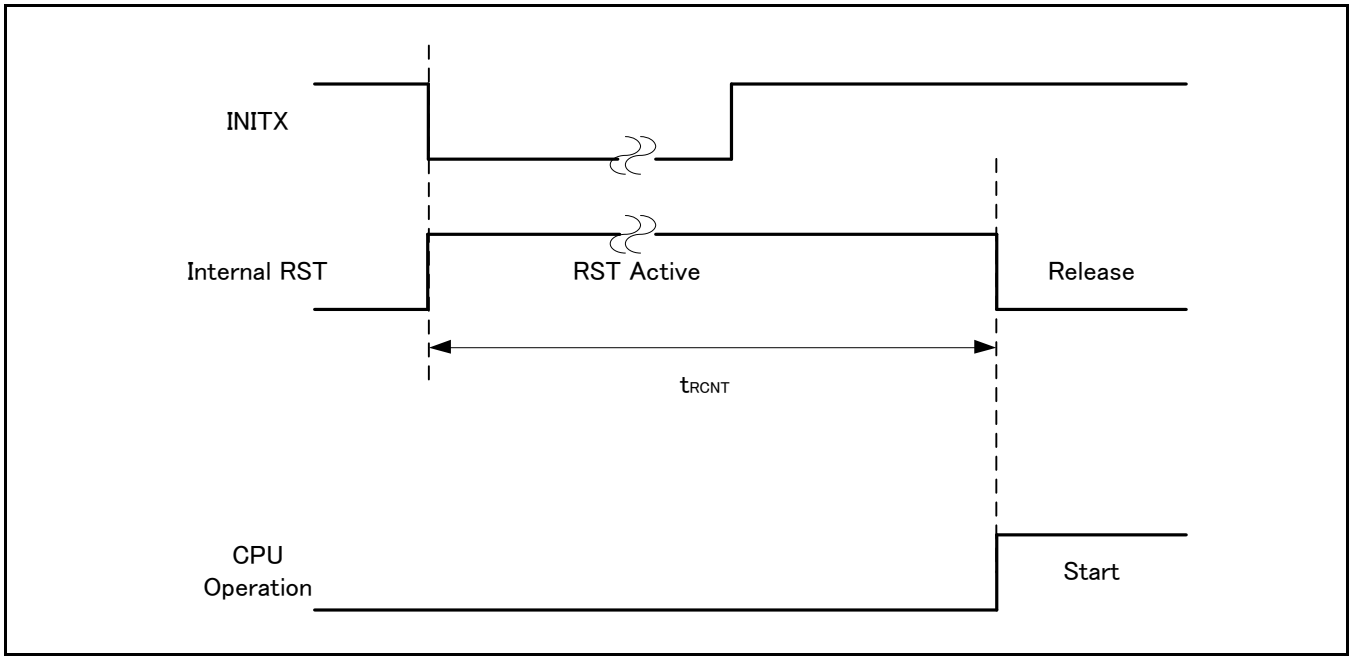
Recovery Count Time

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

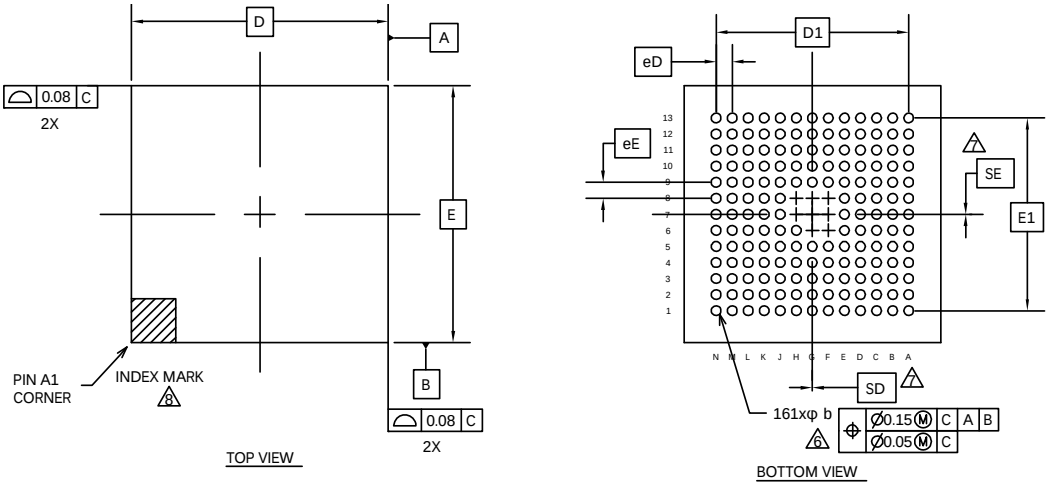
Parameter	Symbol	Value		Unit	Remarks
		Typ	Max*		
Sleep mode	t_{RCNT}	155	266	µs	
High-speed CR Timer mode Main Timer mode PLL Timer mode		155	266	µs	
Low-speed CR timer mode		315	567	µs	
Sub timer mode		315	567	µs	
RTC mode Stop mode		315	567	µs	
Deep standby RTC mode		336	667	µs	without RAM retention
Deep standby Stop mode		336	667	µs	with RAM retention

*: The maximum value depends on the built-in CR accuracy.

Example of Standby Recovery Operation (when in INITX Recovery)



Package Type	Package Code
FBGA 161	FDJ 161



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.20
A1	0.20	0.25	0.30
D		8.00 BSC	
E		8.00 BSC	
D1		6.00 BSC	
E 1		6.00 BSC	
MD		13	
ME		13	
n		161	
Φb	0.25	0.30	0.35
eD		0.50 BSC	
eE		0.50 BSC	
SD / SE		0.00	

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONS AND TOLERANCES METHODS PER ASME Y14.5-2009. THIS OUTLINE CONFORMS TO JEP95, SECTION 4.5.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-010.
4. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION. SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION. n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW. WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" OR "SE" =0. WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
8. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK. METALLIZED MARK INDENTATION OR OTHER MEANS.
9. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
10. JEDEC SPECIFICATION NO. REF: N/A.

002-16413 **

PACKAGE OUTLINE, 161 BALL FBGA
8.00X8.00X1.20 MM FDJ161 REV**