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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	56800E
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	23
Program Memory Size	12KB (6K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 16
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 15x12b SAR
Oscillator Type	External, Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc56f8002vwl

- Parallel instruction set with unique DSP addressing modes
- Hardware DO and REP loops
- Three internal address buses
- Four internal data buses
- Instruction set supports DSP and controller functions
- Controller-style addressing modes and instructions for compact code
- Efficient C compiler and local variable support
- Software subroutine and interrupt stack with depth limited only by memory
- JTAG/enhanced on-chip emulation (EOnCE) for unobtrusive, processor speed–independent, real-time debugging

3.1.2 Operation Range

- 1.8 V to 3.6 V operation (power supplies and I/O)
- From power-on-reset: approximately 1.9 V to 3.6 V
- Ambient temperature operating range:
  - –40 °C to 125 °C

3.1.3 Memory

- Dual Harvard architecture permits as many as three simultaneous accesses to program and data memory
- Flash security and protection that prevent unauthorized users from gaining access to the internal flash
- On-chip memory
  - 16 KB of program flash for 56F8006 and 12 KB of program flash for 56F8002
  - 2 KB of unified data/program RAM
- EEPROM emulation capability using flash

3.1.4 Interrupt Controller

- Five interrupt priority levels
  - Three user programmable priority levels for each interrupt source: Level 0, 1, 2
  - Unmaskable level 3 interrupts include: illegal instruction, hardware stack overflow, misaligned data access, SWI3 instruction. Maskable level 3 interrupts include: EOnCE step counter, EOnCE breakpoint unit, EOnCE trace buffer
  - Lowest-priority software interrupt: level LP
- Allow nested interrupt that higher priority level interrupt request can interrupt lower priority interrupt subroutine
- The masking of interrupt priority level is managed by the 56800E core
- One programmable fast interrupt that can be assigned to any interrupt source
- Notification to system integration module (SIM) to restart clock out of wait and stop states
- Ability to relocate interrupt vector table

3.1.5 Peripheral Highlights

- One multi-function, six-output pulse width modulator (PWM) module
  - Up to 96 MHz PWM operating clock
  - 15 bits of resolution
  - Center-aligned and edge-aligned PWM signal mode
  - Phase shifting PWM pulse generation

  - 1/16 bit-time noise detection
- One serial peripheral interface (SPI)
  - Full-duplex operation
  - Master and slave modes
  - Programmable length transactions (2 to 16 bits)
  - Programmable transmit and receive shift order (MSB as first or last bit transmitted)
  - Maximum slave module frequency = module clock frequency/2
- One inter-integrated Circuit (I^2C) port
  - Operates up to 400 kbps
  - Supports master and slave operation
  - Supports 10-bit address mode and broadcasting mode
  - Supports SMBus, Version 2
- One 16-bit programmable interval timer (PIT)
  - 16 bit counter with programmable counter modulo
  - Interrupt capability
- One 16-bit programmable delay block (PDB)
  - 16 bit counter with programmable counter modulo and delay time
  - Counter is initiated by positive transition of internal or external trigger pulse
  - Supports two independently controlled delay pulses used to synchronize PGA and ADC conversions with input trigger event
  - Two PDB outputs can be ORed together to schedule two conversions from one input trigger event
  - PDB outputs can be can be used to schedule precise edge placement for a pulsed output that generates the control signal for the CMP windowing comparison
  - Supports continuous or single shot mode
  - Bypass mode supported
- Computer operating properly (COP)/watchdog timer capable of selecting different clock sources
  - Programmable prescaler and timeout period
  - Programmable wait, stop, and partial powerdown mode operation
  - Causes loss of reference reset 128 cycles after loss of reference clock to the PLL is detected
  - Choice of clock sources from four sources in support of EN60730 and IEC61508:
    - On-chip relaxation oscillator
    - External crystal oscillator/external clock source
    - System clock (IPBus up to 32 MHz)
    - On-chip low power 1 kHz oscillator
- Real-timer counter (RTC)
  - 8-bit up-counter
  - Three software selectable clock sources
    - External crystal oscillator/external clock source
    - On-chip low-power 1 kHz oscillator
    - System bus (IPBus up to 32 MHz)
  - Can signal the device to exit power down mode
- Phase lock loop (PLL) provides a high-speed clock to the core and peripherals
  - Provides 3x system clock to PWM and dual timer and SCI
  - Loss of lock interrupt
  - Loss of reference clock interrupt

- Clock sources
  - On-chip relaxation oscillator with two user selectable frequencies: 400 kHz for low speed mode, 8 MHz for normal operation
  - On-chip low-power 1 kHz oscillator can be selected as clock source to the RTC and/or COP
  - External clock: crystal oscillator, ceramic resonator, and external clock source
- Power management controller (PMC)
  - On-chip regulator for digital and analog circuitry to lower cost and reduce noise
  - Integrated power-on reset (POR)
  - Low-voltage interrupt with a user selectable trip voltage of 1.81 V or 2.31 V
  - User selectable brown-out reset
  - Run, wait, and stop modes
  - Low-power run, wait, and stop modes
  - Partial power down mode
- Up to 40 general-purpose I/O (GPIO) pins
  - Individual control for each pin to be in peripheral or GPIO mode
  - Individual input/output direction control for each pin in GPIO mode
  - Hysteresis and configurable pullup device on all input pins
  - Configurable slew rate and drive strength and optional input low pass filters on all output pins
  - 20 mA sink/source current
- JTAG/EOnCE debug programming interface for real-time debugging
  - IEEE 1149.1 Joint Test Action Group (JTAG) interface
  - EOnCE interface for real-time debugging

3.1.6 Power Saving Features

- Three low power modes
  - Low-speed run, wait, and stop modes: 200 kHz IP bus clock provided by ROSC
  - Low-power run, wait, and stop modes: clock provided by external 32–38.4 kHz crystal
  - Partial power down mode
- Low power external oscillator can be used in any low-power mode to provide accurate clock to active peripherals
- Low power real time counter for use in run, wait, and stop modes with internal and external clock sources
- 32 µs typical wakeup time from partial power down modes
- Each peripheral can be individually disabled to save power

3.2 Award-Winning Development Environment

Processor Expert™ (PE) provides a Rapid Application Design (RAD) tool that combines easy-to-use component-based software application creation with an expert knowledge system.

The CodeWarrior Integrated Development Environment is a sophisticated tool for code navigation, compiling, and debugging. A complete set of evaluation modules (EVMs), demonstration board kit, and development system cards support concurrent engineering. Together, PE, CodeWarrior, and EVMs create a complete, scalable tools solution for easy, fast, and efficient development.

A full set of programmable peripherals — PWM, PGAs, ADCs, SCI, SPI, I^2C, PIT, timers, and analog comparators — supports various applications. Each peripheral can be independently shut down to save power. Any pin in these peripherals can also be used as general-purpose input/outputs (GPIOs).

3.3 Architecture Block Diagram

The 56F8006/56F8002's architecture is shown in Figure 2 and Figure 3. Figure 2 illustrates how the 56800E system buses communicate with internal memories and the IPBus interface and the internal connections among each unit of the 56800E core. Figure 3 shows the peripherals and control blocks connected to the IPBus bridge. Please see the system integration module (SIM) section in the *MC56F8006 Reference Manual* for information about which signals are multiplexed with those of other peripherals.

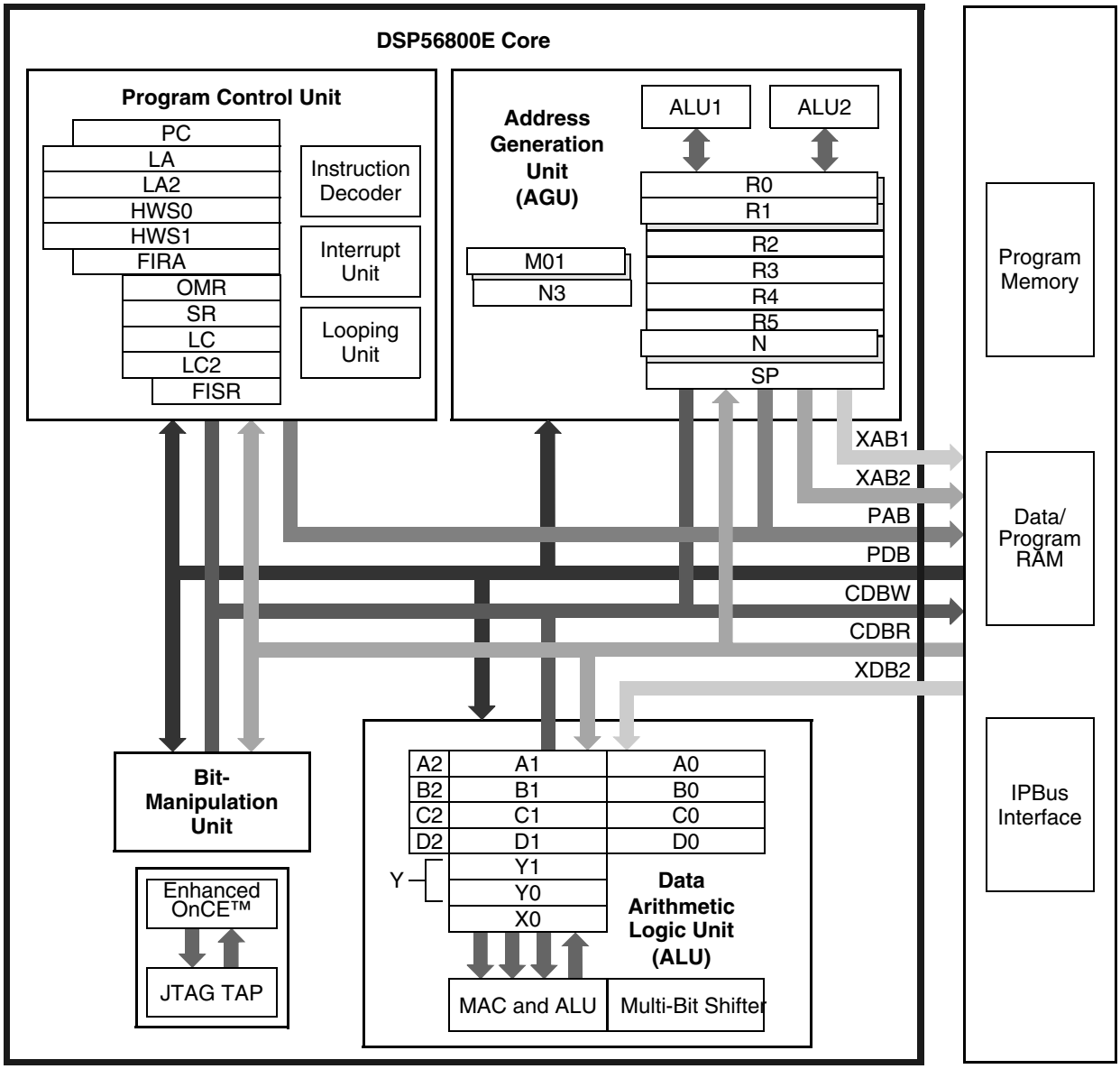

Figure 2. 56800E Core Block Diagram

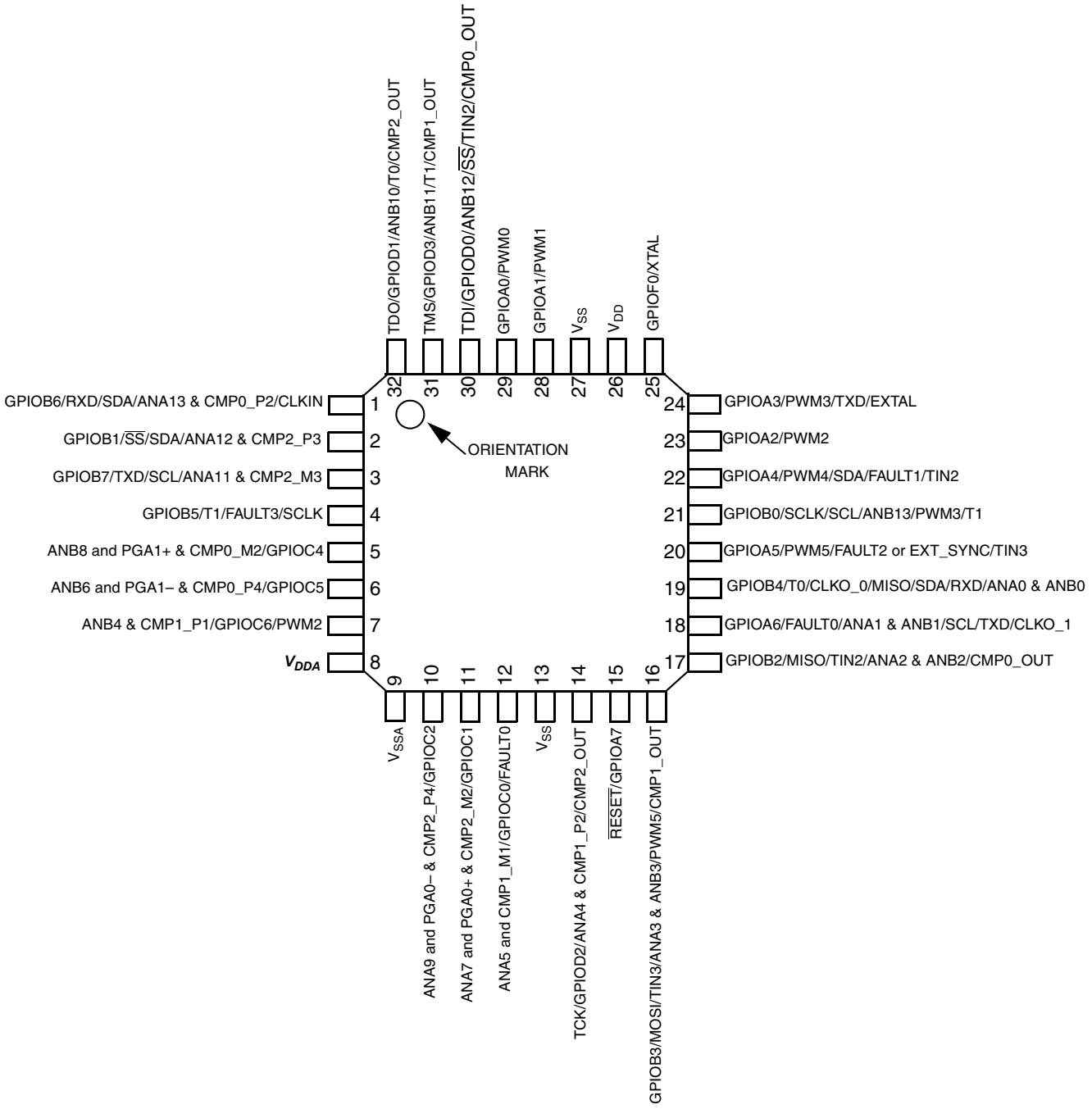

Figure 5. Top View, MC56F8006 32-Pin LQFP Package

Each ADC contains a temperature sensor. Outputs of temperature sensors, PGAs, on-chip regulators and VDDA are internally routed to ADC inputs.

- Internal PGA0 output available on ANA15
- Internal PGA0 positive input calibration voltage available on ANA16
- Internal PGA0 negative input calibration voltage available on ANA17
- Internal PGA1 output available on ANB15
- Internal PGA1 positive input calibration voltage available on ANB16
- Internal PGA1 negative input calibration voltage available on ANB17
- ADCA temperature sensor available on ANA26
- ADCB temperature sensor available on ANB26
- Output of on-chip digital voltage regulator is routed to ANA24
- Output of on-chip analog voltage regulator is routed to ANA25
- Output of on-chip small voltage regulator for ROSC is routed to ANB24
- Output of on-chip small voltage regulator for PLL is routed to ANB25
- VDDA is routed to ANA27 and ANB27

6.8 Joint Test Action Group (JTAG)/Enhanced On-Chip Emulator (EOnCE)

The DSP56800E Family includes extensive integrated support for application software development and real-time debugging. Two modules, the Enhanced On-Chip Emulation module (EOnCE) and the core test access port (TAP, commonly called the JTAG port), work together to provide these capabilities. Both are accessed through a common 4-pin JTAG/EOnCE interface. These modules allow you to insert the 56F8006/56F8002 into a target system while retaining debug control. This capability is especially important for devices without an external bus, because it eliminates the need for a costly cable to bring out the footprint of the chip, as is required by a traditional emulator system.

The DSP56800E EOnCE module is a Freescale-designed module used to develop and debug application software used with the chip. This module allows non-intrusive interaction with the CPU and is accessible through the pins of the JTAG interface or by software program control of the DSP56800E core. Among the many features of the EOnCE module is the support for data communication between the controller and the host software development and debug systems in real-time program execution. Other features allow for hardware breakpoints, the monitoring and tracking of program execution, and the ability to examine and modify the contents of registers, memory, and on-chip peripherals, all in a special debug environment. No user-accessible resources need to be sacrificed to perform debugging operations.

The DSP56800E JTAG port is used to provide an interface for the EOnCE module to the DSP JTAG pins. Joint Test Action Group (JTAG) boundary scan is an IEEE 1149.1 standard methodology enabling access to test features using a test access port (TAP). A JTAG boundary scan consists of a TAP controller and boundary scan registers. Please contact your Freescale sales representative or authorized distributor for device-specific BSDL information.

NOTE

In normal operation, an external pullup on the TMS pin is highly recommend to place the JTAG state machine in reset state if this pin is not configured as GPIO.

7 Security Features

The 56F8006/56F8002 offers security features intended to prevent unauthorized users from reading the contents of the flash memory (FM) array. The 56F8006/56F8002's flash security consists of several hardware interlocks that prevent unauthorized users from gaining access to the flash array.

After flash security is set, an authorized user can be enabled to access on-chip memory if a user-defined software subroutine, which reads and transfers the contents of internal memory via peripherals, is included in the application software. This

Table 21. DC Characteristics (continued)

Characteristic	Symbol	Condition	Min	Typ[1]	Max	Unit	Ambient temperature operating range
Low-voltage detection threshold — high range[7]	V_{LVDH}[8]	V_{DD} falling	2.31	2.34	2.36	V	–40 °C ~ 105 °C
			2.16	2.3	2.48		—40 °C ~ +125 °C
		V_{DD} rising	2.38	2.44	2.47		–40 °C ~ 105 °C
			2.23	2.39	2.49		—40 °C ~ +125 °C
Low-voltage detection threshold — low range[7]	V_{LVDL}	V_{DD} falling	1.8	1.84	1.87	V	–40 °C ~ 105 °C
			N/A	N/A	N/A		—40 °C ~ +125 °C
		V_{DD} rising	1.88	1.93	1.96		–40 °C ~ 105 °C
Low-voltage warning threshold	V_{LVW}[9]	V_{DD} falling	2.58	2.62	2.71	V	–40 °C ~ 105 °C
			2.5	2.61	2.74		—40 °C ~ +125 °C
		V_{DD} rising	2.59	2.67	2.74		–40 °C ~ 105 °C
			2.51	2.66	2.79		—40 °C ~ +125 °C
Low-voltage inhibit reset/recover hysteresis[7]	V_{hys}		—	50	—	mV	—40 °C ~ +105 °C
Bandgap Voltage Reference[10]	V_{BG}		1.15	1.17	1.18	V	–40 °C ~ 105 °C
			1.14				—40 °C ~ +125 °C

1 Typical values are measured at 25 °C. Characterized, not tested

2 As the supply voltage rises, the LVD circuit holds the MCU in reset until the supply has risen above V_{LVDL}. If the system clock frequency < 16 MHz, V_{DD} can be 1.7 V to 3.6 V.

3 All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.

4 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

5 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load shunts current greater than maximum injection current. This is the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present or if clock rate is low (which would reduce overall power consumption).

6 Maximum is highest voltage that POR is guaranteed.

7 Low voltage detection and warning limits measured at 32 MHz bus frequency. This characteristic is not applicable to devices with a temperature range from –40 °C to 125 °C. Please see the PMC chapter in the reference manual for details.

Table 22. Supply Current Consumption (continued)

Mode	Conditions	Typical @ 3.3 V, 25 °C		Maximum @ 3.6 V, 105 °C		Maximum @ 3.6 V, 125 °C	
		I_{DD} [1]	I_{DDA}	I_{DD} [1]	I_{DDA}	I_{DD} [1]	I_{DDA}
LPwait [3]	32.768 kHz device clock; Clocked by a 32.768 kHz external crystal oscillator in power down; PLL disabled; All peripheral modules disabled and clock gated off; processor core in wait state	157.55 µA	1.57 mA	380 µA	3.4 mA	398 µA	3.6 mA
Stop	32 MHz device clock relaxation oscillator (ROSC) in high speed mode; PLL engaged; all peripheral module and core clocks are off; ADC/DAC/comparator powered off; processor core in stop state	8.21 mA	65.51 µA	9.8 mA	130 µA	10.3 mA	132 µA
LSstop [2]	200 kHz device clock; relaxation oscillator (ROSC) in standby mode; PLL disabled; all peripheral modules disabled and clock gated off; processor core in stop state.	194.69 µA	65.51 µA	340 µA	120 µA	357 µA	123 µA
LPstop [2]	32.768 kHz device clock; Clocked by a 32.768 kHz external crystal relaxation oscillator (ROSC) in power down; PLL disabled; all peripheral modules disabled and clock gated off; processor core in stop state.	2.77 µA	13.99 nA	45 µA	3.0 µA	58 µA	3.6 µA
PPD [4] with XOSC	32.768 kHz clock fed on XTAL RTC or COP monitoring XOSC (but no wakeup) processor core in stop state	879.72 nA	11.56 nA	18 µA	2.4 µA	22 µA	3.0 µA
PPD with LP oscillator (1 kHz) enabled	RTC or COP monitoring LP oscillator (but no wakeup); processor core in stop state.	499.15 nA	13.9 nA	14 µA	2.4 µA	17 µA	2.8 mA
PPD with no clock monitoring	RTC and LP oscillator are disabled; processor core in stop state.	494.04 nA	12.88 nA	14 µA	2.4 µA	17 µA	2.8 µA

1 No output switching; all ports configured as inputs; all inputs low; no DC loads.

2 Low speed mode: LPR (lower voltage regulator control bit) = 0 and voltage regulator is in full regulation. Characterization only.

3 Low power mode: LPR (lower voltage regulator control bit) = 1; the voltage regulator is put into standby.

4 Partial power down mode: PPDE (partial power down enable bit) = 1; power management controller (PMC) enters partial power down mode the next time that the STOP command is executed.

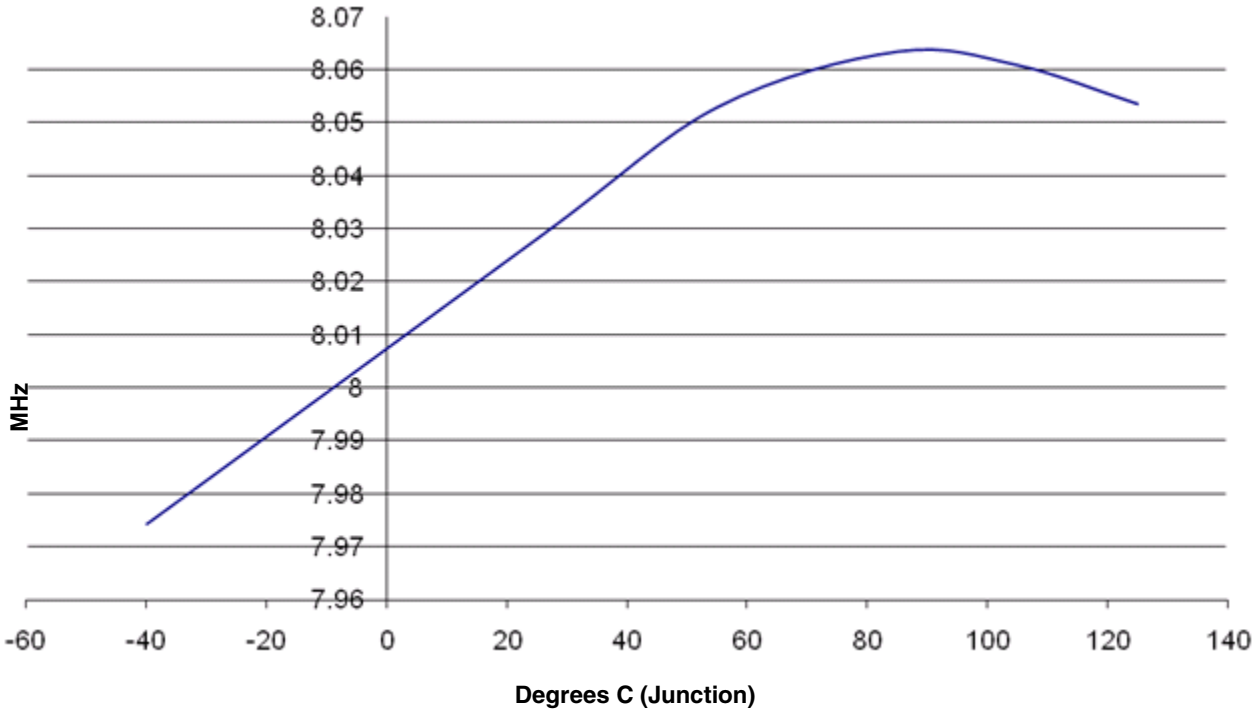

Figure 22. Relaxation Oscillator Temperature Variation (Typical) After Trim for devices with temperature operating range from –40 °C to 105 °C

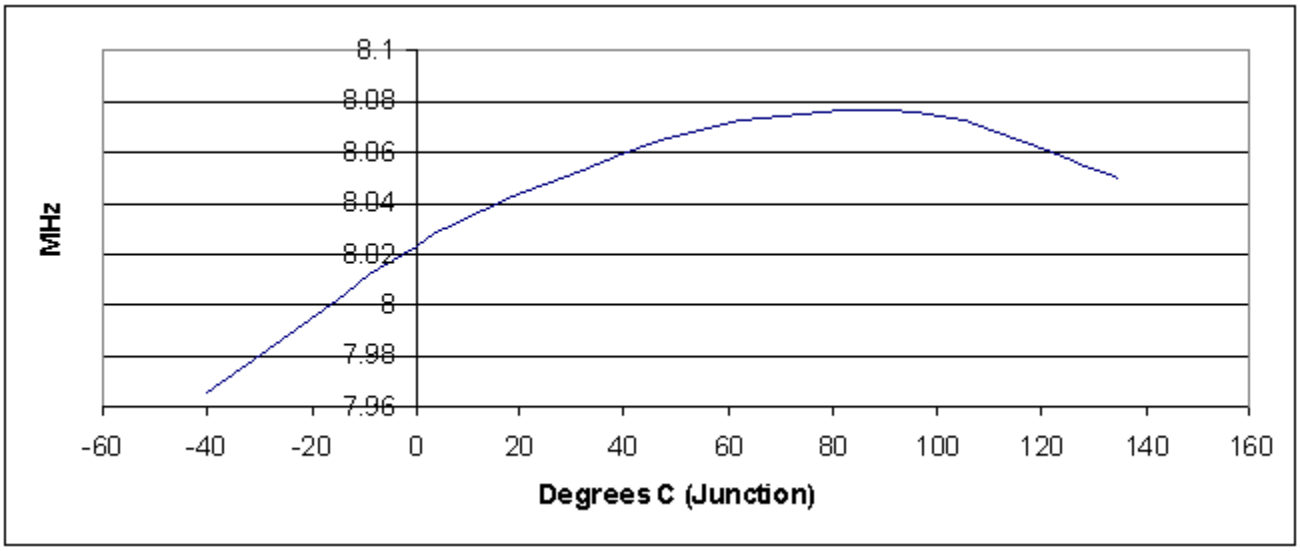

Figure 23. Relaxation Oscillator Temperature Variation (Typical) After Trim for devices with temperature operating range from –40 °C to 125 °C

- Tri-stated, when a bus or signal is placed in a high impedance state
- Data Valid state, when a signal level has reached V_{OL} or V_{OH}
- Data Invalid state, when a signal level is in transition between V_{OL} and V_{OH}

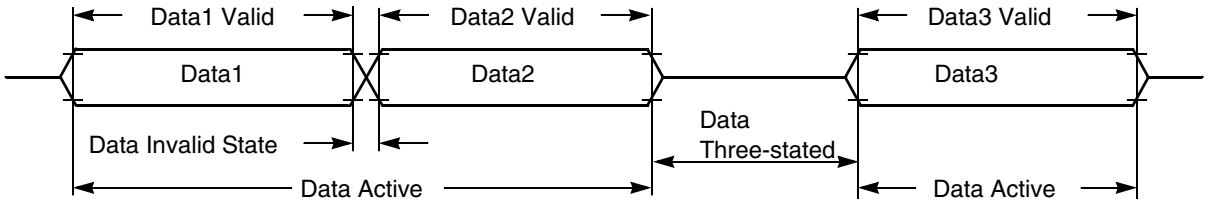

Figure 26. Signal States

8.13.1 Serial Peripheral Interface (SPI) Timing

Table 29. SPI Timing[1]

Characteristic	Symbol	Min	Max	Unit	See Figure
Cycle time Master Slave	t_C	 125 62.5	 — —	 ns ns	Figure 27, Figure 28, Figure 29, Figure 30
Enable lead time Master Slave	t_{ELD}	 — 31	 — —	 ns ns	Figure 30
Enable lag time Master Slave	t_{ELG}	 — 125	 — —	 ns ns	Figure 30
Clock (SCK) high time Master Slave	t_{CH}	 50 31	 — —	 ns ns	Figure 27, Figure 28, Figure 29, Figure 30
Clock (SCK) low time Master Slave	t_{CL}	 50 31	 — —	 ns ns	Figure 30
Data set-up time required for inputs Master Slave	t_{DS}	 20 0	 — —	 ns ns	Figure 27, Figure 28, Figure 29, Figure 30
Data hold time required for inputs Master Slave	t_{DH}	 0 2	 — —	 ns ns	Figure 27, Figure 28, Figure 29, Figure 30
Access time (time to data active from high-impedance state) Slave	t_A	4.8	15	ns	Figure 30
Disable time (hold time to high-impedance state) Slave	t_D	3.7	15.2	ns	Figure 30

Table 29. SPI Timing[1] (continued)

Characteristic	Symbol	Min	Max	Unit	See Figure
Data valid for outputs Master Slave (after enable edge)	t_{DV}	 — —	 4.5 20.4	 ns ns	Figure 27, Figure 28, Figure 29, Figure 30
Data invalid Master Slave	t_{DI}	 0 0	 — —	 ns ns	Figure 27, Figure 28, Figure 29, Figure 30
Rise time Master Slave	t_R	 — —	 11.5 10.0	 ns ns	Figure 27, Figure 28, Figure 29, Figure 30
Fall time Master Slave	t_F	 — —	 9.7 9.0	 ns ns	Figure 27, Figure 28, Figure 29, Figure 30

1 Parameters listed are guaranteed by design.

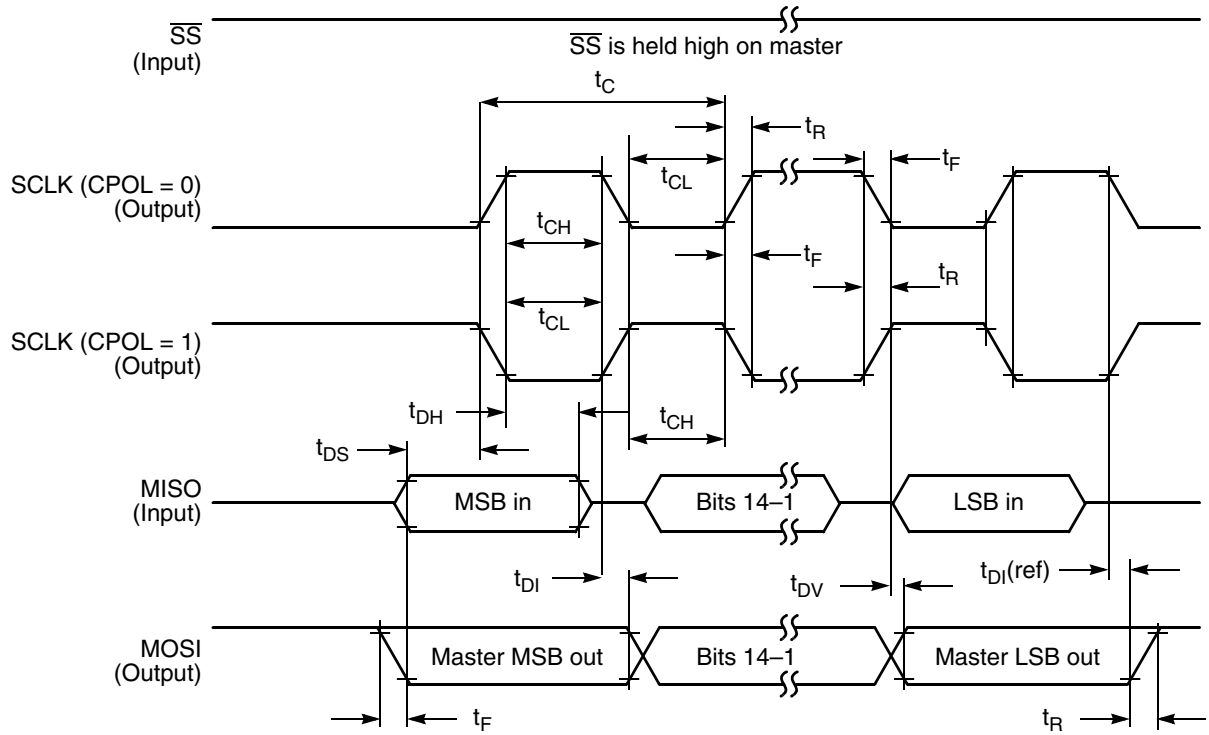

Figure 27. SPI Master Timing (CPHA = 0)

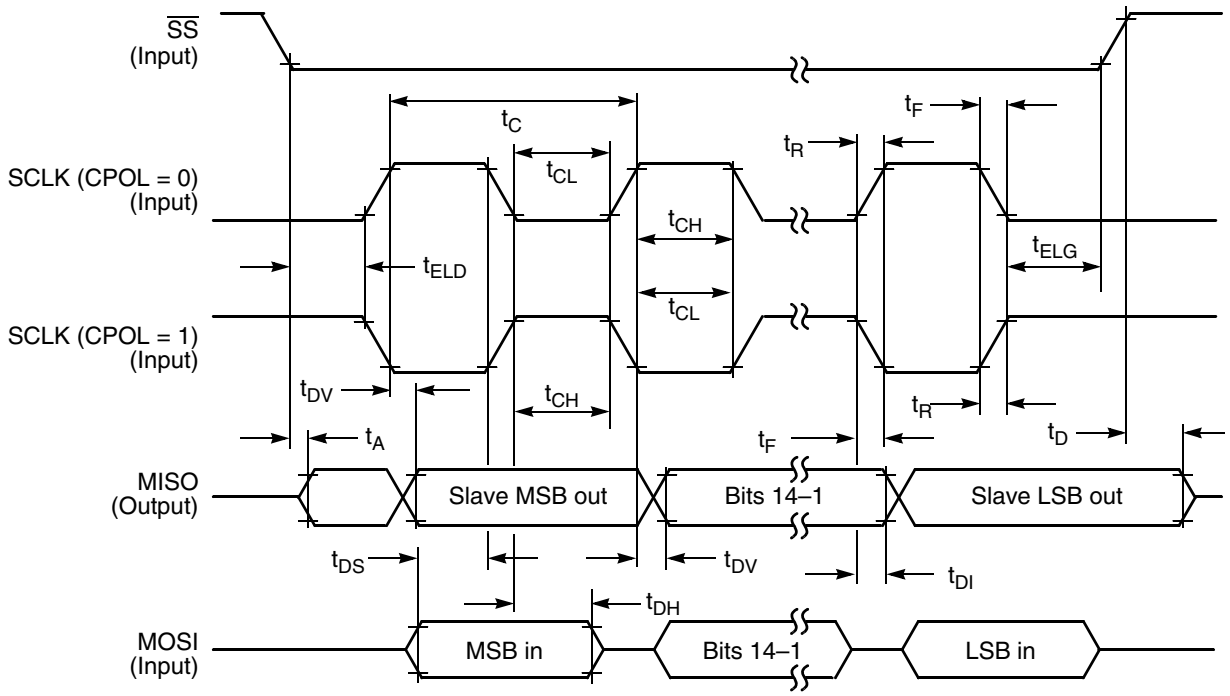

Figure 30. SPI Slave Timing (CPHA = 1)

8.13.2 Serial Communication Interface (SCI) Timing

Table 30. SCI Timing[1]

Characteristic	Symbol	Min	Max	Unit	See Figure
Baud rate[2]	BR	—	(f_{MAX}/16)	Mbps	—
RXD pulse width	RXD_{PW}	0.965/BR	1.04/BR	ns	Figure 31
TXD pulse width	TXD_{PW}	0.965/BR	1.04/BR	ns	Figure 32
LIN Slave Mode					
Deviation of slave node clock from nominal clock rate before synchronization	$F_{TOL\_UNSYNCH}$	–14	14	%	—
Deviation of slave node clock relative to the master node clock after synchronization	F_{TOL_SYNCH}	–2	2	%	—
Minimum break character length	T_{BREAK}	13	—	Master node bit periods	—
		11	—	Slave node bit periods	—

1 Parameters listed are guaranteed by design.

2 f_{MAX} is the frequency of operation of the SCI in MHz, which can be selected system clock (max. 32 MHz) or 3x system clock (max. 96 MHz) for the 56F8006/56F8002 device.

Power consumption is given by the following equation:

Eqn. 1

$$\begin{aligned}\text{Total power} = \quad & \text{A: internal [static component]} \\ & +\text{B: internal [state-dependent component]} \\ & +\text{C: internal [dynamic component]} \\ & +\text{D: external [dynamic component]} \\ & +\text{E: external [static component]}\end{aligned}$$

A, the internal [static] component, is comprised of the DC bias currents for the oscillator, leakage currents, PLL, and voltage references. These sources operate independently of processor state or operating frequency.

B, the internal [state-dependent] component, reflects the supply current required by certain on-chip resources only when those resources are in use. These include RAM, flash memory, and the ADCs.

C, the internal [dynamic] component, is classic $C*V^2*F$ CMOS power dissipation corresponding to the 56800E core and standard cell logic.

D, the external [dynamic] component, reflects power dissipated on-chip as a result of capacitive loading on the external pins of the chip. This is also commonly described as $C*V^2*F$, although simulations on two of the I/O cell types used on the 56800E reveal that the power-versus-load curve does have a non-zero Y-intercept.

Table 39. I/O Loading Coefficients at 10 MHz

	Intercept	Slope
8 mA drive	1.3	0.11 mW/pF
4 mA drive	1.15 mW	0.11 mW/pF

Power due to capacitive loading on output pins is (first order) a function of the capacitive load and frequency at which the outputs change. Table 39 provides coefficients for calculating power dissipated in the I/O cells as a function of capacitive load. In these cases:

$$\textit{TotalPower} = \Sigma((\text{Intercept} + \text{Slope}*\text{Cload})*\text{frequency}/10\ \text{MHz}) \qquad \textit{Eqn. 2}$$

where:

- Summation is performed over all output pins with capacitive loads
- Total power is expressed in mW
- C_{load} is expressed in pF

Because of the low duty cycle on most device pins, power dissipation due to capacitive loads was found to be fairly low when averaged over a period of time.

E, the external [static component], reflects the effects of placing resistive loads on the outputs of the device. Sum the total of all V^2/R or IV to arrive at the resistive load contribution to power. Assume V = 0.5 for the purposes of these rough calculations. For instance, if there is a total of eight PWM outputs driving 10 mA into LEDs, then P = 8*0.5*0.01 = 40 mW.

In previous discussions, power consumption due to parasitics associated with pure input pins is ignored, as it is assumed to be negligible.

freescale semiconductor	MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ASH70029A
		PAGE: 873A
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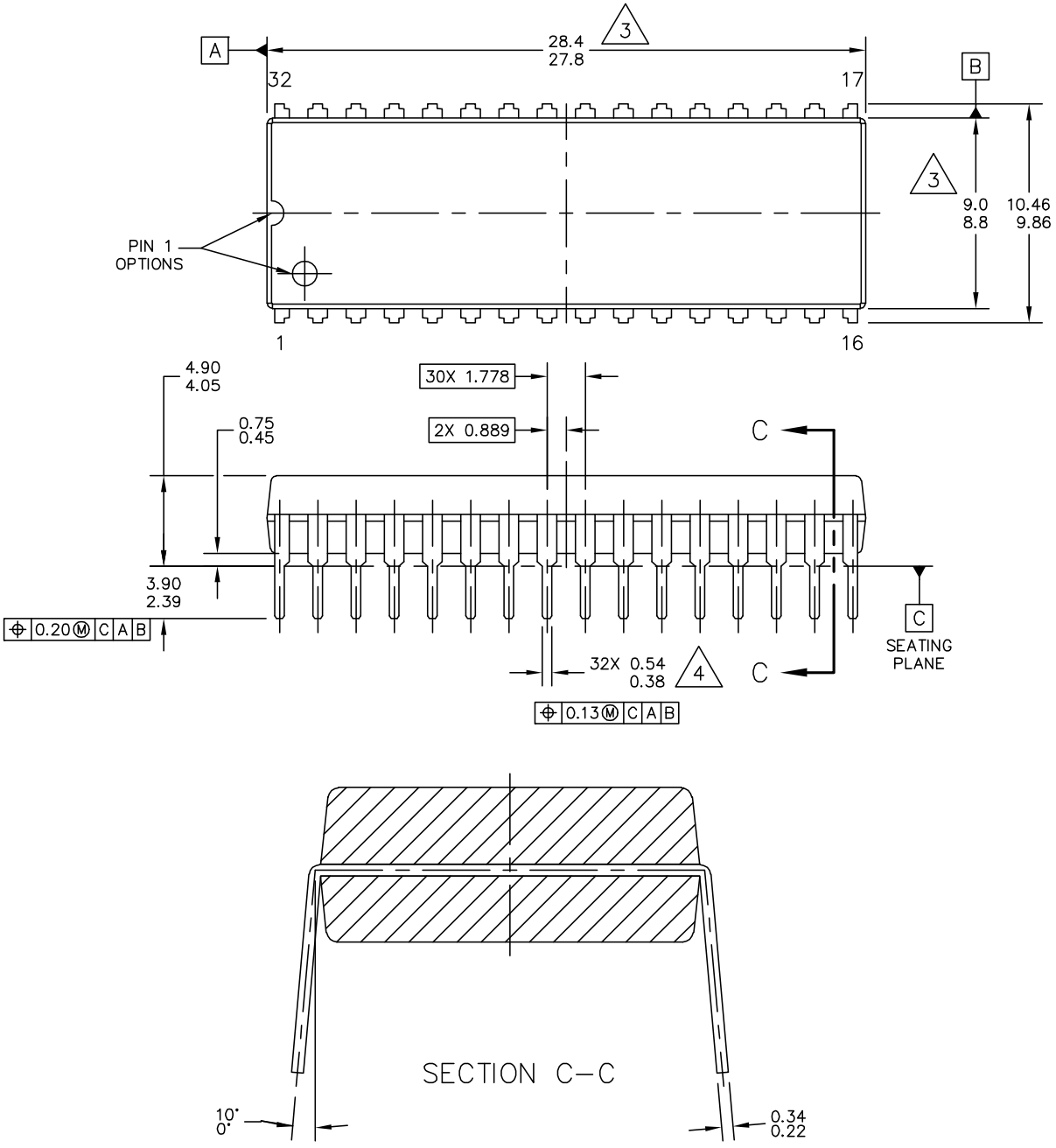
NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5–1994.
3. DATUMS A, B, AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE DATUM C.
5. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM DIMENSION BY MORE THAN 0.08 MM. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION: 0.07 MM.
6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 MM PER SIDE. DIMENSIONS ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 MM AND 0.25 MM FROM THE LEAD TIP.

TITLE: LOW PROFILE QUAD FLAT PACK (LQFP) 32 LEAD, 0.8 PITCH (7 X 7 X 1.4)	CASE NUMBER: 873A-03	
	STANDARD: JEDEC MS-026 BBA	
	PACKAGE CODE: 6300	SHEET: 3 OF 4

Figure 39. 56F8006/56F8002 32-Pin LQFP Mechanical Information

10.4 32-Pin PSDIP



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TITLE: 32 LEAD PDIP	DOCUMENT NO: 98ASA99330D	REV: A
	CASE NUMBER: 1376–02	25 APR 2005
	STANDARD: NON–JEDEC	

Table 43. Interrupt Vector Table Contents[1] (continued)

Peripheral	Vector Number	User Encoding	Priority Level	Vector Base Address +	Interrupt Function
Reserved	34- 39	0x22-0x27	0	P:0x44 - P:0x4E	Reserved
core	40	N/A	0	P:0x50	SW Interrupt 0
core	41	N/A	1	P:0x52	SW Interrupt 1
core	42	N/A	2	P:0x54	SW Interrupt 2
core	43	N/A	3	P:0x56	SW Interrupt 3
SWILP	44	N/A	-1	P:0x58	SW Interrupt Low Priority
USER1	45	N/A	1	P:0x5A	User Programmable Priority Level 1 Interrupt
USER2	46	N/A	1	P:0x5C	User Programmable Priority Level 1 Interrupt
USER3	47	N/A	1	P:0x5E	User Programmable Priority Level 1 Interrupt
USER4	48	N/A	2	P:0x60	User Programmable Priority Level 2 Interrupt
USER5	49	N/A	2	P:0x62	User Programmable Priority Level 2 Interrupt
USER6[3]	50	N/A	2	P:0x64	User Programmable Priority Level 2 Interrupt

1 Two words are allocated for each entry in the vector table. This does not allow the full address range to be referenced from the vector table, providing only 19 bits of address.

2 If the VBA is set to the reset value, the first two locations of the vector table overlay the chip reset addresses because the reset address would match the base of this vector table.

3 USER6 vector can be defined as a fast interrupt if the instruction located in this vector location is not a JSR or BSR instruction. Please see section 9.3.3.3 of *DSP56800E 16-Bit Core Reference Manual* for detail.

Appendix B
Peripheral Register Memory Map and Reset Value

NOTE

In Table 44, ADC0 stands for ADCA, ADC1 stands for ADCB, and GPIOn is the same as GPIO_n (for example, GPIOA_PUR is the same as GPIO_A_PUR).

Table 44. Detailed Peripheral Memory Map

Offset Addr. (Hex)	Reset Value (Hex)	Periph.	Register	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Bit 0
00	0000	TMR0	TMR0_ COMP1	COMPARISON_1															
01	0000	TMR0	TMR0_ COMP2	COMPARISON_2															
02	0000	TMR0	TMR0_ CAPT	CAPTURE															
03	0000	TMR0	TMR0_ LOAD	LOAD															
04	0000	TMR0	TMR0_ HOLD	HOLD															
05	0000	TMR0	TMR0_ CNTR	COUNTER															
06	0000	TMR0	TMR0_ CTRL	CM			PCS				SCS		ONCE	LENGTH	DIR	Co_INIT	OM		
07	0000	TMR0	TMR0_ SCTRL	TCF	TCFIE	TOF	TOFIE	IEF	IEFIE	IPS	INPUT	CAPTURE_ MODE		MSTR	EEOF	VAL	FORCE	OPS	OEN
08	0000	TMR0	TMR0_ CMPLD1	COMPARATOR_LOAD_1															
09	0000	TMR0	TMR0_ CMPLD2	COMPARATOR_LOAD_2															

Table 44. Detailed Peripheral Memory Map (continued)

Offset Addr. (Hex)	Reset Value (Hex)	Periph.	Register	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Bit 0
1A	0000	TMR1	TMR1_ CSCTRL	DBG_EN		FAULT	ALT_LOAD	0	0	0	0	TCF2EN	TCF1EN	TCF2	TCF1	CL2		CL1	
1B	0000	TMR1	TMR1_ FILT	0	0	0	0	0	FILT_CNT			FILT_PER							
1C–1F	—	TMR1	Reserved	RESERVED															
20	0000	PWM	PWM_ CTRL	LDFQ				HALF	IPOL2	IPOL1	IPOL0	PRSC		PWMRIE	PWMF	ISENS		LDOK	PWMEN
21	0000	PWM	PWM_ FCTRL	0	0	0	0	FPOL3	FPOL2	FPOL1	FPOL0	FIE3	FMODE3	FIE2	FMODE2	FIE1	FMODE1	FIE0	FMODE0
22	0000	PWM	PWM_ FLTACK	FPIN3	FFLAG3	FPIN2	FFLAG2	FPIN1	FFLAG1	FPIN0	FFLAG0		FTACK3		FTACK2		FTACK1		FTACK0
23	0000	PWM	PWM_ OUT	PAD_EN	0	OUTCTL5	OUTCTL4	OUTCTL3	OUTCTL2	OUTCTL1	OUTCTL0	0	0	OUT5	OUT4	OUT3	OUT2	OUT1	OUT0
24	0000	PWM	PWM_ CNTR	0	CR														
25	0000	PWM	PWM_ CMOD	0	PWMCM														
26	0000	PWM	PWM_ VAL0	PMVAL															
27	0000	PWM	PWM_ VAL1	PMVAL															
28	0000	PWM	PWM_ VAL2	PMVAL															

Table 44. Detailed Peripheral Memory Map (continued)

Offset Addr. (Hex)	Reset Value (Hex)	Periph.	Register	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Bit 0
22	0000	I2C	I2C_CR1	0	0	0	0	0	0	0	0	IICEN	IICIE	MST	TX	TXAK	RSTA	0	0
23	0080	I2C	I2C_SR	0	0	0	0	0	0	0	0	TCF	IAAS	BUSY	ARBL	0	SRW	IICIF	RXAK
24	0000	I2C	I2C_DATA	0	0	0	0	0	0	0	0	DATA							
25	0000	I2C	I2C_CR2	0	0	0	0	0	0	0	0	GCAEN	ADEXT	0	0	0	AD10	AD9	AD8
26	0000	I2C	I2C_SMB_CSR	0	0	0	0	0	0	0	0	RESERVED	RESERVED	SIICAEN	TCKSEL	SLTF	SHTF	0	0
27	0000	I2C	I2C_ADDR2	0	0	0	0	0	0	0	0	SAD7	SAD6	SAD5	SAD4	SAD3	SAD2	SAD1	0
28	0000	I2C	I2C_SLT1	0	0	0	0	0	0	0	0	SSLT15	SSLT14	SSLT13	SSLT12	SSLT11	SSLT10	SSLT9	SSLT8
29	0000	I2C	I2C_SLT2	0	0	0	0	0	0	0	0	SSLT7	SSLT6	SSLT5	SSLT4	SSLT3	SSLT2	SSLT1	SSLT0
30–3F	—	I2C	Reserved	RESERVED															
40	0302	COP	COP_CTRL	0	0	0	0	0	0	PSS		0	CLKSEL		CLOREN	CSEN	CWEN	CEN	CWP
41	FFFF	COP	COP_TOUT	TIMEOUT															
42	FFFF	COP	COP_CNTR	COUNT_SERVICE															
43–5F	—	COP	Reserved	RESERVED															

Table 44. Detailed Peripheral Memory Map (continued)

Offset Addr. (Hex)	Reset Value (Hex)	Periph.	Register	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Bit 0
0D	0000	GPIOE	GPIOE_ SLEW	0	0	0	0	0	0	0	0	SLEW							
0E–1F	—	GPIOE	Reserved	RESERVED															
20	00FF	GPIOF	GPIOF_ PUR	0	0	0	0	0	0	0	0	0	0	0	0	PUR			
21	0000	GPIOF	GPIOF_DR	0	0	0	0	0	0	0	0	0	0	0	0	DR			
22	0000	GPIOF	GPIOF_ DDR	0	0	0	0	0	0	0	0	0	0	0	0	DDR			
23	0080	GPIOF	GPIOF_ PER	0	0	0	0	0	0	0	0	0	0	0	0	PER			
24	—	GPIOF	Reserved	RESERVED															
25	0000	GPIOF	GPIOF_ IENR	0	0	0	0	0	0	0	0	0	0	0	0	IENR			
26	0000	GPIOF	GPIOF_ IPOLR	0	0	0	0	0	0	0	0	0	0	0	0	IPOLR			
27	0000	GPIOF	GPIOF_ IPR	0	0	0	0	0	0	0	0	0	0	0	0	IPR			
28	0000	GPIOF	GPIOF_ IESR	0	0	0	0	0	0	0	0	0	0	0	0	IESR			
29	—	GPIOF	Reserved	RESERVED															
2A	0000	GPIOF	GPIOF_ RAWDATA	0	0	0	0	0	0	0	0	0	0	0	0	RAWDATA			
2B	0000	GPIOF	GPIOF_ DRIVE	0	0	0	0	0	0	0	0	0	0	0	0	DRIVE			
2C	00FF	GPIOF	GPIOF_IFE	0	0	0	0	0	0	0	0	0	0	0	0	IFE			
2D	0000	GPIOF	GPIOF_ SLEW	0	0	0	0	0	0	0	0	0	0	0	0	SLEW			
2E–3F	—	GPIOF	Reserved	RESERVED															