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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	56800E
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	23
Program Memory Size	12KB (6K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 16
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 15x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc56f8002vwlr

Table of Contents

2 Block Diagram

Figure 1 shows a top-level block diagram of the MC56F8006/MC56F8002 digital signal controller. Package options for this family are described later in this document. Italics indicate a 56F8002 device parameter.

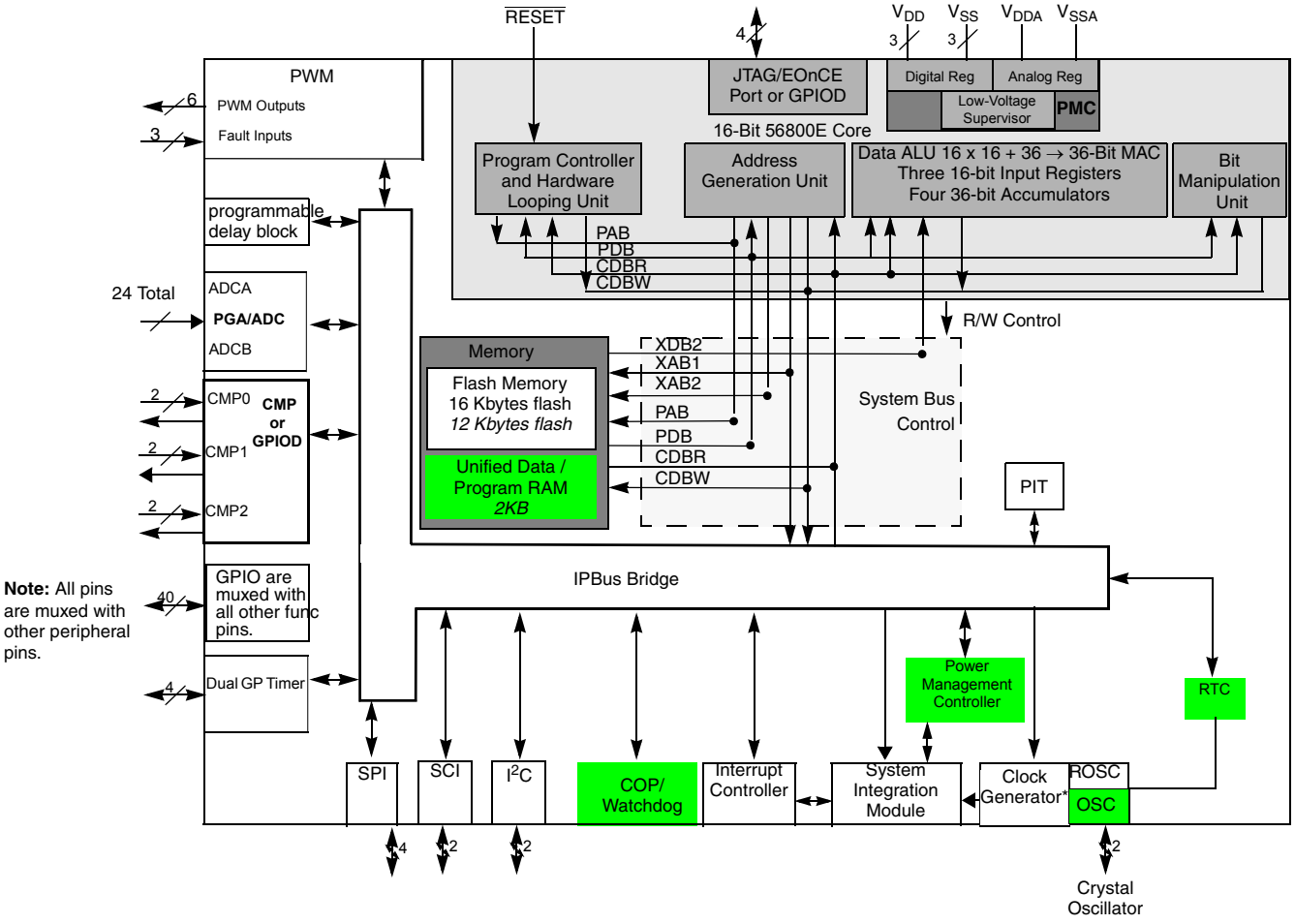

Figure 1. MC56F8006/MC56F8002 Block Diagram

3 Overview

3.1 56F8006/56F8002 Features

3.1.1 Core

- Efficient 16-bit 56800E family digital signal controller (DSC) engine with dual Harvard architecture
- As many as 32 million instructions per second (MIPS) at 32 MHz core frequency
- 155 basic instructions in conjunction with up to 20 address modes
- Single-cycle 16 × 16-bit parallel multiplier-accumulator (MAC)
- Four 36-bit accumulators, including extension bits
- 32-bit arithmetic and logic multi-bit shifter

  - Four programmable fault inputs with programmable digital filter
  - Double-buffered PWM registers
  - Separate deadtime insertions for rising and falling edges
  - Separate top and bottom pulse-width correction by means of software
  - Asymmetric PWM output within both Center Aligned and Edge Aligned operation
  - Separate top and bottom polarity control
  - Each complementary PWM signal pair allows selection of a PWM supply source from:
    - PWM generator
    - Internal timers
    - Analog comparator outputs
- Two independent 12-bit analog-to-digital converters (ADCs)
  - 2 x 14 channel external inputs plus seven internal inputs
  - Support simultaneous and software triggering conversions
  - ADC conversions can be synchronized by PWM and PDB modules
  - Sampling rate up to 400 KSPS for 10- or 12-bit conversion result; 470 KSPS for 8-bit conversion result
  - Two 16-word result registers
- Two programmable gain amplifier (PGAs)
  - Each PGA is designed to amplify and convert differential signals to a single-ended value fed to one of the ADC inputs
  - 1X, 2X, 4X, 8X, 16X, or 32X gain
  - Software and hardware triggers are available
  - Integrated sample/hold circuit
  - Includes additional calibration features:
    - Offset calibration eliminates any errors in the internal reference used to generate the VDDA/2 output center point
    - Gain calibration can be used to verify the gain of the overall datapath
    - Both features require software correction of the ADC result
- Three analog comparators (CMPs)
  - Selectable input source includes external pins, internal DACs
  - Programmable output polarity
  - Output can drive timer input, PWM fault input, PWM source, external pin output, and trigger ADCs
  - Output falling and rising edge detection able to generate interrupts
- One dual channel 16-bit multi-purpose timer module (TMR)
  - Two independent 16-bit counter/timers with cascading capability
  - Up to 96 MHz operating clock
  - Each timer has capture and compare and quadrature decoder capability
  - Up to 12 operating modes
  - Four external inputs and two external outputs
- One serial communication interface (SCI) with LIN slave functionality
  - Up to 96 MHz operating clock
  - Full-duplex or single-wire operation
  - Programmable 8- or 9- bit data format
  - Two receiver wakeup methods:
    - Idle line
    - Address mark

3.3 Architecture Block Diagram

The 56F8006/56F8002's architecture is shown in Figure 2 and Figure 3. Figure 2 illustrates how the 56800E system buses communicate with internal memories and the IPBus interface and the internal connections among each unit of the 56800E core. Figure 3 shows the peripherals and control blocks connected to the IPBus bridge. Please see the system integration module (SIM) section in the *MC56F8006 Reference Manual* for information about which signals are multiplexed with those of other peripherals.

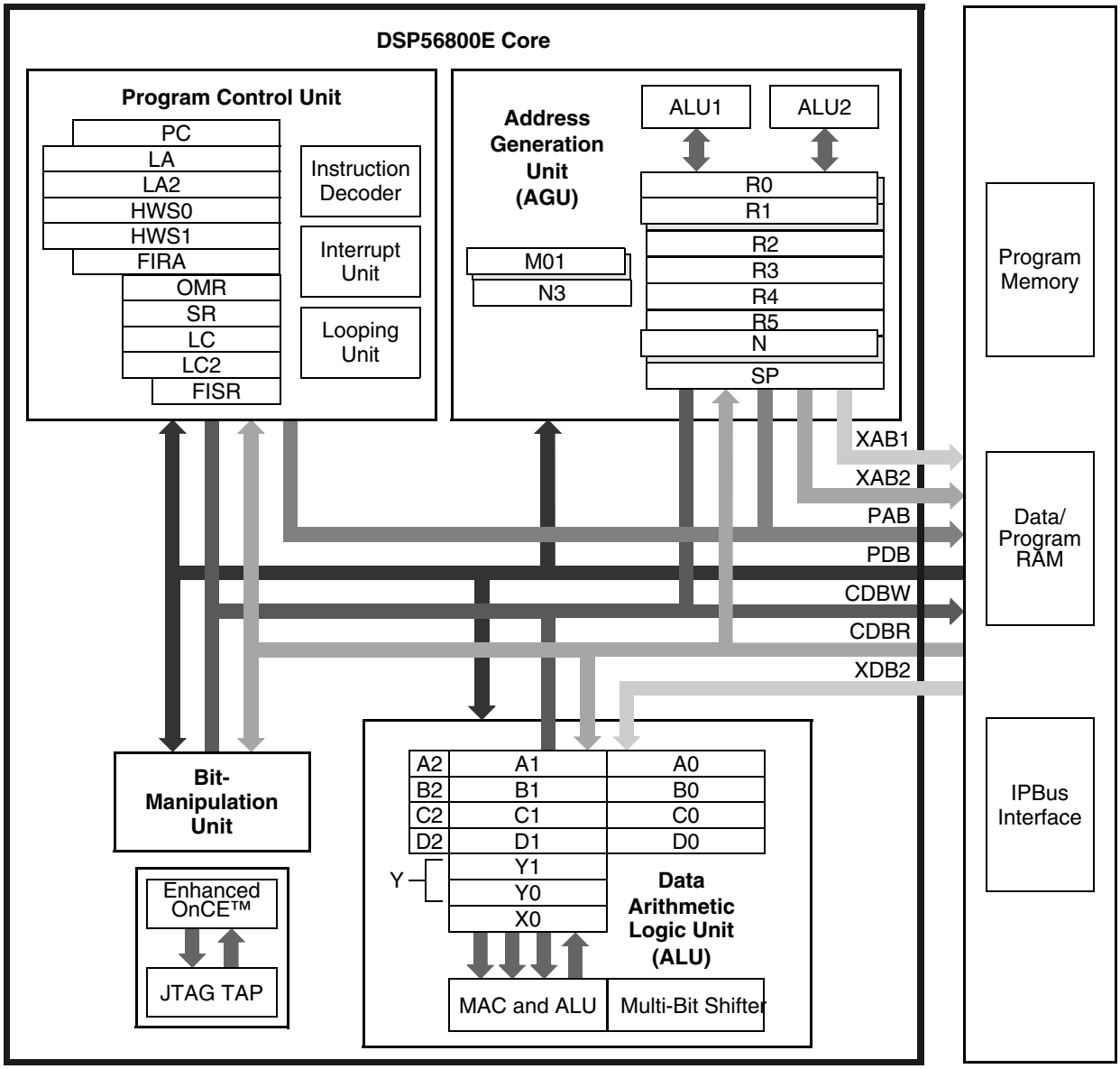

Figure 2. 56800E Core Block Diagram

Table 5. 56F8006/56F8002 Signal and Package Information (continued)

Signal Name	28 SOIC	32 LQFP	32 PSDIP	48 LQFP	Type	State During Reset	Signal Description
GPIOA3	17	24	20	36	Input/ Output	Input, internal pullup enabled	Port A GPIO — This GPIO pin can be individually programmed as an input or output pin.
(PWM3)					Output		PWM3 — The PWM channel 3.
(TXD)					Output		TXD — The SCI transmit data output or transmit/receive in single wire operation.
(EXTAL)					Analog Input		EXTAL — External Crystal Oscillator Input. This input can be connected to a 32.768 kHz or 1–16 MHz external crystal or ceramic resonator. When used to supply a source to the internal PLL, the crystal/resonator must be in the 4 MHz to 8 MHz range. Tie this pin low or configure as GPIO if XTAL is being driven by an external clock source. If using a 32.768 kHz crystal, place the crystal as close as possible to device pins to speed startup. After reset, the default state is GPIOA3.
GPIOA4	16	22	18	33	Input/ Output	Input, internal pullup enabled	Port A GPIO — This GPIO pin can be individually programmed as an input or output pin.
(PWM4)					Output		PWM4 — The PWM channel 4.
(SDA)					Input/Open-drain Output		SDA — The I^2C serial data line.
(FAULT1)					Input		FAULT1 — PWM fault input 1used for disabling selected PWM outputs in cases where fault conditions originate off-chip.
(TIN2)					Input		TIN2 — Dual timer module channel 2 input After reset, the default state is GPIOA4.
GPIOA5	14	20	16	29	Input/ Output	Input, internal pullup enabled	Port A GPIO — This GPIO pin can be individually programmed as an input or output pin.
(PWM5)					Output		PWM5 — The PWM channel 5.
(FAULT2/ EXT_SYNC)					Input/ Output		FAULT2 — PWM fault input 2 used for disabling selected PWM outputs in cases where fault conditions originate off-chip. EXT_SYNC — When not being used as a fault input, this pin can be used to receive a pulse to reset the PWM counter or to generate a positive pulse at the start of every PWM cycle.
(TIN3)					Input		TIN3 — Dual timer module channel 3 input After reset, the default state is GPIOA5.

5.6 EOnCE Memory Map

Control registers of the EOnCE are located at the top of data memory space. These locations are fixed by the 56F800E core. These registers can also be accessed through JTAG port if flash security is not set. Table 11 lists all EOnCE registers necessary to access or control the EOnCE.

Table 11. EOnCE Memory Map

Address	Register Acronym	Register Name
X:0xFF FFFF	OTX1/ORX1	Transmit Register Upper Word Receive Register Upper Word
X:0xFF FFFE	OTX/ORX (32 bits)	Transmit Register Receive Register
X:0xFF FFFD	OTXRXSR	Transmit and Receive Status and Control Register
X:0xFF FFFC	OCLSR	Core Lock/Unlock Status Register
X:0xFF FFFB– X:0xFF FFA1		Reserved
X:0xFF FFA0	OCR	Control Register
X:0xFF FF9F– X:0xFF FF9E	OSCNTR (24 bits)	Instruction Step Counter
X:0xFF FF9D	OSR	Status Register
X:0xFF FF9C	OBASE	Peripheral Base Address Register
X:0xFF FF9B	OTBCR	Trace Buffer Control Register
X:0xFF FF9A	OTBPR	Trace Buffer Pointer Register
X:0xFF FF99– X:0xFF FF98	OTB (21–24 bits/stage)	Trace Buffer Register Stages
X:0xFF FF97– X:0xFF FF96	OBCR (24 bits)	Breakpoint Unit Control Register
X:0xFF FF95– X:0xFF FF94	OBAR1 (24 bits)	Breakpoint Unit Address Register 1
X:0xFF FF93– X:0xFF FF92	OBAR2 (32 bits)	Breakpoint Unit Address Register 2
X:0xFF FF91– X:0xFF FF90	OBMSK (32 bits)	Breakpoint Unit Mask Register 2
X:0xFF FF8F		Reserved
X:0xFF FF8E	OBCNTR	EOnCE Breakpoint Unit Counter
X:0xFF FF8D		Reserved
X:0xFF FF8C		Reserved
X:0xFF FF8B		Reserved
X:0xFF FF8A	OESCR	External Signal Control Register
X:0xFF FF89 – X:0xFF FF00		Reserved

application software could communicate over a serial port, for example, to validate the authenticity of the requested access, then grant it until the next device reset. The inclusion of such a back door technique is at the discretion of the system designer.

7.1 Operation with Security Enabled

After you have programmed flash with the application code, or as part of the programming of the flash with the application code, the 56F8006/56F8002 can be secured by programming the security word, 0x0002, into program memory location 0x00 1FF7. This can also be effected by use of the CodeWarrior IDE menu flash lock command. This nonvolatile word keeps the device secured after reset, caused, for example, by a power-down of the device. Refer to the flash memory chapter in the *MC56F8006 Peripheral Reference Manual* for detail. When flash security mode is enabled, the 56F8006/56F8002 disables the core EOnCE debug capabilities. Normal program execution is otherwise unaffected.

7.2 Flash Access Lock and Unlock Mechanisms

There are several methods that effectively lock or unlock the on-chip flash.

7.2.1 Disabling EOnCE Access

On-chip flash can be read by issuing commands across the EOnCE port, which is the debug interface for the 56800E CPU. The TCK, TMS, TDO, and TDI pins comprise a JTAG interface onto which the EOnCE port functionality is mapped. When the device boots, the chip-level JTAG TAP (test access port) is active and provides the chip's boundary scan capability and access to the ID register, but proper implementation of flash security blocks any attempt to access the internal flash memory via the EOnCE port when security is enabled. This protection is effective when the device comes out of reset, even prior to the execution of any code at startup.

7.2.2 Flash Lockout Recovery Using JTAG

If the device is secured, one lockout recovery mechanism is the complete erasure of the internal flash contents, including the configuration field, thus disabling security (the protection register is cleared). This does not compromise security, as the entire contents of your secured code stored in flash are erased before security is disabled on the device on the next reset or power-up sequence.

To start the lockout recovery sequence via JTAG, the JTAG public instruction (LOCKOUT_RECOVERY) must first be shifted into the chip-level TAP controller's instruction register. After the LOCKOUT_RECOVERY instruction has been shifted into the instruction register, the clock divider value must be shifted into the corresponding 7-bit data register. After the data register has been updated, you must transition the TAP controller into the RUN-TEST/IDLE state for the lockout sequence to commence. The controller must remain in this state until the erase sequence is complete. Refer to the *MC56F8006 Peripheral Reference Manual* for detail, or contact Freescale.

NOTE

After the lockout recovery sequence has completed, you must reset the JTAG-TAP controller and device to return to normal unsecured operation. Power-on reset resets both too.

7.2.3 Flash Lockout Recovery Using CodeWarrior

CodeWarrior can unlock a device by selecting the *Debug* menu, then selecting *DSP56800E*, followed by *Unlock Flash*. Another mechanism is also built into CodeWarrior using the device's memory configuration file. The command "*Unlock_Flash_on_Connect 1*" in the *.cfg* file accomplishes the same task as using the *Debug* menu.

This lockout recovery mechanism is the complete erasure of the internal flash contents, including the configuration field, thus disabling security (the protection register is cleared).

8.9 Phase Locked Loop Timing

Table 25. Phase Locked Loop Timing

Characteristic	Symbol	Min	Typ	Max	Unit
PLL input reference frequency[1]	f_{ref}	4	8	—	MHz
PLL output frequency[2]	f_{op}	120	192	—	MHz
PLL lock time[3] [4]	t_{plls}	—	40	100	µs
Accumulated jitter using an 8 MHz external crystal as the PLL source[5]	J_A	—	—	0.37	%
Cycle-to-cycle jitter	$t_{jitterpll}$	—	350	—	ps

1 An externally supplied reference clock should be as free as possible from any phase jitter for the PLL to work correctly. The PLL is optimized for 8 MHz input.

2 The core system clock operates at 1/6 of the PLL output frequency.

3 This is the time required after the PLL is enabled to ensure reliable operation.

4 From powerdown to powerup state at 32 MHz system clock state.

5 This is measured on the CLKO signal (programmed as system clock) over 264 system clocks at 32 MHz system clock frequency and using an 8 MHz oscillator frequency.

8.10 Relaxation Oscillator Timing

Table 26. Relaxation Oscillator Timing

Characteristic	Symbol	Minimum	Typical	Maximum	Unit
Relaxation oscillator output frequency[1] Normal Mode Standby Mode	f_{op}	—	 8.05 400	—	 MHz kHz
Relaxation oscillator stabilization time[2]	t_{roscs}	—	1	3	ms
Cycle-to-cycle jitter. This is measured on the CLKO signal (programmed prescaler_clock) over 264 clocks[3]	$t_{jitterrosc}$	—	400	—	ps
Variation over temperature –40 °C to 105 °C[4]		—	—	–3.0 to +2.0	%
Variation over temperature 0 °C to 105 °C[5]		—	—	–2.0 to +2.0	%
Variation over temperature –40 °C to 125 °C[4]		—	—	–3.5 to +3.0	%

1 Output frequency after factory trim.

2 This is the time required from standby to normal mode transition.

3 J_A is required to meet QSCI requirements.

4 See Figure 22. The power supply VDD must be greater than or equal to 2.6 V. Below 2.6 V, the maximum variation over the whole temperature and whole voltage range from 1.8 V to 2.6 V will be +/-16%.

5 This data is only applied to devices with temperature range from –40 °C to 105 °C.

8.16 ADC Specifications

Table 36. ADC Operating Conditions

Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
Input voltage		V_{ADIN}	V_{REFL}[2]	—	V_{REFH}[3]	V	
Input capacitance		C_{ADIN}	—	4.5	5.5	pF	
Input resistance		R_{ADIN}	—	5	7	kΩ	
Analog source resistance	12-bit mode f_{ADCK} > 4 MHz f_{ADCK} < 4 MHz	R_{AS}	 — —	 — —	 2 5	kΩ	External to MCU
	10-bit mode f_{ADCK} > 4 MHz f_{ADCK} < 4 MHz		 — —	 — —	 5 10		
	8-bit mode (all valid f_{ADCK})		—	—	10		
ADC conversion clock freq.	High speed (ADLPC=0)	f_{ADCK}	0.4	—	8.0	MHz	
	Low power (ADLPC=1)		0.4	—	4.0		

1 Typical values assume V_{DDAD} = 3.0 V, Temp = 25°C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 $V_{REFL} = V_{SSA}$

3 $V_{REFH} = V_{DDA}$

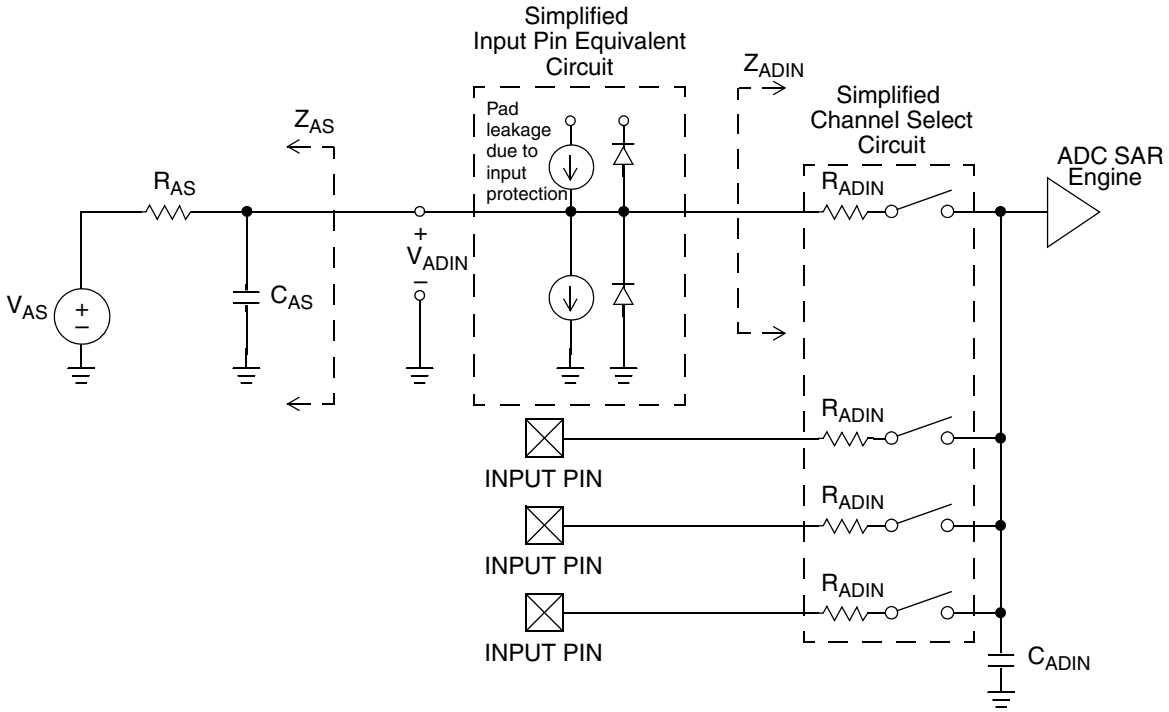

Figure 37. ADC Input Impedance Equivalency Diagram

junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

When heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimizing the size of the clearance is important to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back-calculate the case temperature using a separate measurement of the thermal resistance of the interface. From this case temperature, the junction temperature is determined from the junction-to-case thermal resistance.

9.2 Electrical Design Considerations

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, take normal precautions to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.

Use the following list of considerations to assure correct operation of the 56F8006/56F8002:

- Provide a low-impedance path from the board power supply to each V_{DD} pin on the 56F8006/56F8002 and from the board ground to each V_{SS} (GND) pin.
- The minimum bypass requirement is to place 0.01–0.1µF capacitors positioned as near as possible to the package supply pins. The recommended bypass configuration is to place one bypass capacitor on each of the V_{DD}/V_{SS} pairs, including V_{DDA}/V_{SSA}. Ceramic and tantalum capacitors tend to provide better tolerances.
- Ensure that capacitor leads and associated printed circuit traces that connect to the chip V_{DD} and V_{SS} (GND) pins are as short as possible.
- Bypass the V_{DD} and V_{SS} with approximately 100 µF, plus the number of 0.1 µF ceramic capacitors.
- PCB trace lengths should be minimal for high-frequency signals.
- Consider all device loads as well as parasitic capacitance due to PCB traces when calculating capacitance. This is especially critical in systems with higher capacitive loads that could create higher transient currents in the V_{DD} and V_{SS} circuits.
- Take special care to minimize noise levels on the V_{REF}, V_{DDA}, and V_{SSA} pins.
- Using separate power planes for V_{DD} and V_{DDA} and separate ground planes for V_{SS} and V_{SSA} are recommended. Connect the separate analog and digital power and ground planes as near as possible to power supply outputs. If an analog circuit and digital circuit are powered by the same power supply, you should connect a small inductor or ferrite bead in serial with V_{DDA} and V_{SSA} traces.
- Physically separate analog components from noisy digital components by ground planes. Do not place an analog trace in parallel with digital traces. Place an analog ground trace around an analog signal trace to isolate it from digital traces.
- Because the flash memory is programmed through the JTAG/EOnCE port, SPI, SCI, or I^2C, the designer should provide an interface to this port if in-circuit flash programming is desired.
- If desired, connect an external RC circuit to the $\overline{\text{RESET}}$ pin. The resistor value should be in the range of 4.7 kΩ–10 kΩ; the capacitor value should be in the range of 0.22 µF–4.7 µF.
- Configuring the $\overline{\text{RESET}}$ pin to GPIO output in normal operation in a high-noise environment may help to improve the performance of noise transient immunity.
- Add a 2.2 kΩ external pullup on the TMS pin of the JTAG port to keep EOnCE in a restate during normal operation if JTAG converter is not present.
- During reset and after reset but before I/O initialization, all I/O pins are at input state with internal pullup enabled. The typical value of internal pullup is around 33 kΩ. These internal pullups can be disabled by software.
- To eliminate PCB trace impedance effect, each ADC input should have a no less than 33 pF 10 Ω RC filter.
- External clamp diodes on analog input pins are recommended.

9.3 Ordering Information

Table 40 lists the pertinent information needed to place an order. Consult a Freescale Semiconductor sales office or authorized distributor to determine availability and to order devices.

Table 40. 56F8006/56F8002 Ordering Information

Device	Supply Voltage	Package Type	Pin Count	Frequency (MHz)	Ambient Temperature Range	Order Number
MC56F8002	1.8–3.6 V	Small Outline IC (SOIC)	28	32	–40° to + 105° C –40° to + 125° C	MC56F8002VWL MC56F8002MWL[1]
MC56F8006	1.8–3.6 V	Small Outline IC (SOIC)	28	32	–40° to + 105° C –40° to + 125° C	MC56F8006VWL MC56F8006MWL[1]
MC56F8006	1.8–3.6 V	Low-Profile Quad Flat Pack (LQFP)	32	32	–40° to + 105° C –40° to + 125° C	MC56F8006VLC MC56F8006MLC[1]
MC56F8006	1.8–3.6 V	Low-Profile Quad Flat Pack (LQFP)	48	32	–40° to + 105° C –40° to + 125° C	MC56F8006VLF MC56F8006MLF[1]
MC56F8006	1.8–3.6 V	Plastic Shrink Dual In-line Package (PSDIP)	32	32	–40° to + 105° C	MC56F8006VBM

[1] This package is RoHS compliant.

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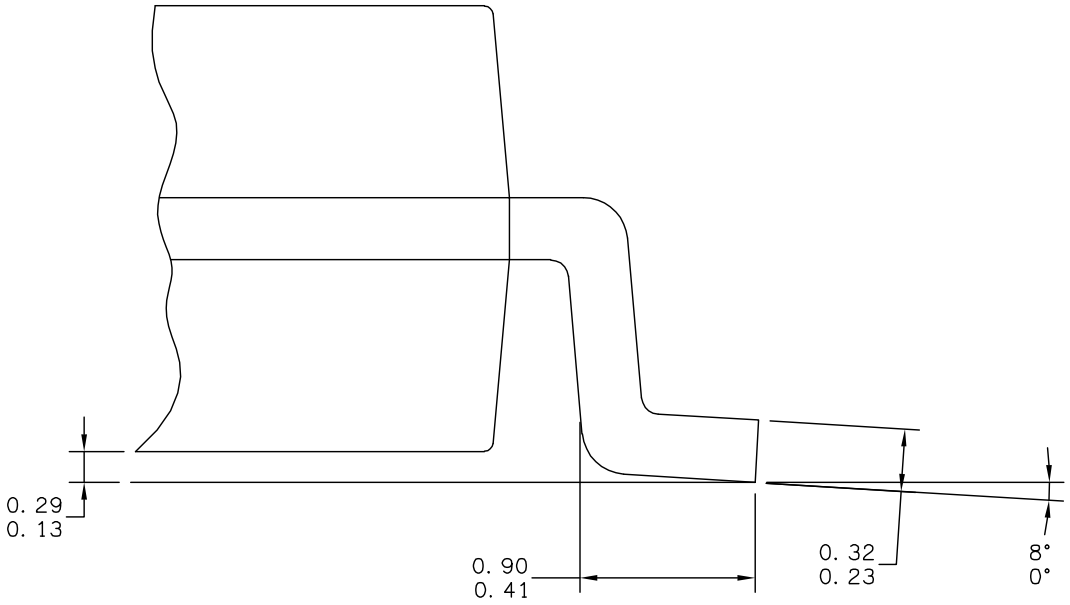
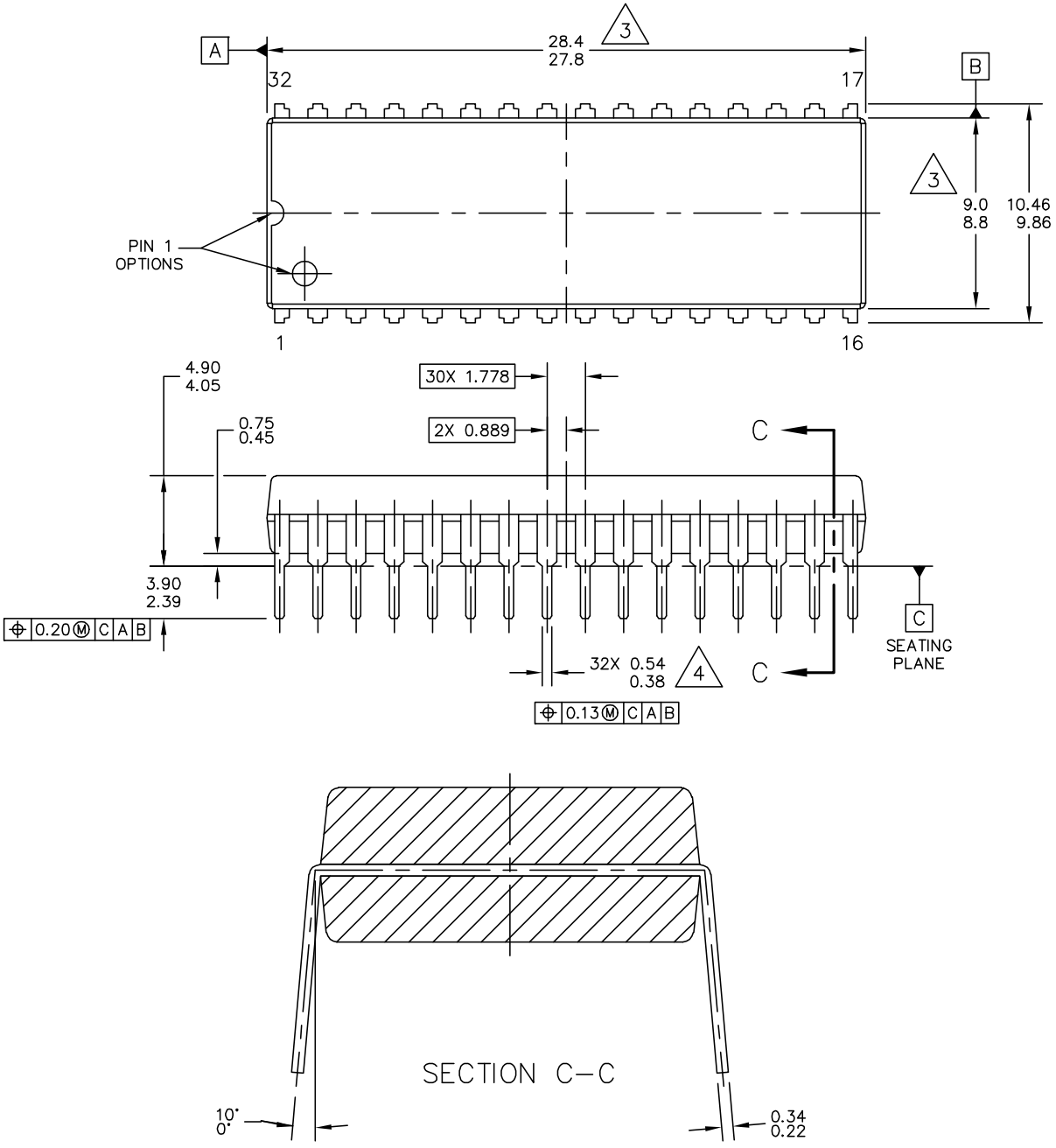


TITLE: SOIC, WIDE BODY, 28 LEAD CASEOUTLINE	CASE NUMBER: 751F-05	
	STANDARD: MS-013AE	
	PACKAGE CODE: 2009	SHEET: 2 OF 4

10.4 32-Pin PSDIP



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	CASE NUMBER: 1376–02	25 APR 2005
	STANDARD: NON–JEDEC	

NOTES:

1. ALL DIMENSION ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5-1994.
3. DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
4. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.

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	CASE NUMBER: 1376-02	25 APR 2005
	STANDARD: NON-JEDEC	

Figure 41. 56F8006/56F8002 32-Pin PSDIP Mechanical Information

Table 44. Detailed Peripheral Memory Map (continued)

Offset Addr. (Hex)	Reset Value (Hex)	Periph.	Register	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Bit 0
1A	0000	TMR1	TMR1_ CSCTRL	DBG_EN		FAULT	ALT_LOAD	0	0	0	0	TCF2EN	TCF1EN	TCF2	TCF1	CL2		CL1	
1B	0000	TMR1	TMR1_ FILT	0	0	0	0	0	FILT_CNT			FILT_PER							
1C–1F	—	TMR1	Reserved	RESERVED															
20	0000	PWM	PWM_ CTRL	LDFQ				HALF	IPOL2	IPOL1	IPOL0	PRSC		PWMRIE	PWMF	ISENS		LDOK	PWMEN
21	0000	PWM	PWM_ FCTRL	0	0	0	0	FPOL3	FPOL2	FPOL1	FPOL0	FIE3	FMODE3	FIE2	FMODE2	FIE1	FMODE1	FIE0	FMODE0
22	0000	PWM	PWM_ FLTACK	FPIN3	FFLAG3	FPIN2	FFLAG2	FPIN1	FFLAG1	FPIN0	FFLAG0		FTACK3		FTACK2		FTACK1		FTACK0
23	0000	PWM	PWM_ OUT	PAD_EN	0	OUTCTL5	OUTCTL4	OUTCTL3	OUTCTL2	OUTCTL1	OUTCTL0	0	0	OUT5	OUT4	OUT3	OUT2	OUT1	OUT0
24	0000	PWM	PWM_ CNTR	0	CR														
25	0000	PWM	PWM_ CMOD	0	PWMCM														
26	0000	PWM	PWM_ VAL0	PMVAL															
27	0000	PWM	PWM_ VAL1	PMVAL															
28	0000	PWM	PWM_ VAL2	PMVAL															

Table 44. Detailed Peripheral Memory Map (continued)

Offset Addr. (Hex)	Reset Value (Hex)	Periph.	Register	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Bit 0
C3	0000	PGA1	PGA1_STS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	RUNNING	STCOMP
C4–DF	—	PGA1	Reserved	RESERVED															
E0	0200	SCI	SCI_RATE	SBR													FRAC_SBR		
E1	0000	SCI	SCI_CTRL1	LOOP	SWAI	RSRC	M	WAKE	POL	PE	PT	TEIE	TIIE	RFIE	REIE	TE	RE	RWU	SBK
E2	0000	SCI	SCI_CTRL2	0	0	0	0	0	0	0	0	0	0	0	0	LIN_MODE	0	0	0
E3	C000	SCI	SCI_STAT	TDRE	TIDLE	RDRF	RIDLE	OR	NF	FE	PF	0	0	0	0	LSE	0	0	RAF
E4	0000	SCI	SCI_DATA	0	0	0	0	0	0	0	RECEIVE_TRANSMIT_DATA								
E5–FF	—	SCI	Reserved	RESERVED															
00	6141	SPI	SPI_SCTRL	SPR			DSO	ERRIE	MODFEN	SPRIE	SPMSTR	CPOL	CPHA	SPE	SPTIE	SPRF	OVRF	MODF	SPTE
01	000F	SPI	SPI_DSCTRL	WOM	0	0	BD2X	SSB_IN	SSB_DATA	SSB_ODM	SSB_AUTO	SSB_DDR	SSB_STRB	SSB_OVER	SPR3	DS			
02	0000	SPI	SPI_DRCV	R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0
03	0000	SPI	SPI_DXMIT	T15	T14	T13	T12	T11	T10	T9	T8	T7	T6	T5	T4	T3	T2	T1	T0
04–1F	—	SPI	Reserved	RESERVED															
20	0000	I2C	I2C_ADDR	0	0	0	0	0	0	0	0	AD7	AD6	AD5	AD4	AD3	AD2	AD1	0
21	0000	I2C	I2C_FREQDIV	0	0	0	0	0	0	0	0	MULT		ICR					

Table 44. Detailed Peripheral Memory Map (continued)

Offset Addr. (Hex)	Reset Value (Hex)	Periph.	Register	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Bit 0
0D	0000	GPIOE	GPIOE_ SLEW	0	0	0	0	0	0	0	0	SLEW							
0E–1F	—	GPIOE	Reserved	RESERVED															
20	00FF	GPIOF	GPIOF_ PUR	0	0	0	0	0	0	0	0	0	0	0	0	PUR			
21	0000	GPIOF	GPIOF_DR	0	0	0	0	0	0	0	0	0	0	0	0	DR			
22	0000	GPIOF	GPIOF_ DDR	0	0	0	0	0	0	0	0	0	0	0	0	DDR			
23	0080	GPIOF	GPIOF_ PER	0	0	0	0	0	0	0	0	0	0	0	0	PER			
24	—	GPIOF	Reserved	RESERVED															
25	0000	GPIOF	GPIOF_ IENR	0	0	0	0	0	0	0	0	0	0	0	0	IENR			
26	0000	GPIOF	GPIOF_ IPOLR	0	0	0	0	0	0	0	0	0	0	0	0	IPOLR			
27	0000	GPIOF	GPIOF_ IPR	0	0	0	0	0	0	0	0	0	0	0	0	IPR			
28	0000	GPIOF	GPIOF_ IESR	0	0	0	0	0	0	0	0	0	0	0	0	IESR			
29	—	GPIOF	Reserved	RESERVED															
2A	0000	GPIOF	GPIOF_ RAWDATA	0	0	0	0	0	0	0	0	0	0	0	0	RAWDATA			
2B	0000	GPIOF	GPIOF_ DRIVE	0	0	0	0	0	0	0	0	0	0	0	0	DRIVE			
2C	00FF	GPIOF	GPIOF_IFE	0	0	0	0	0	0	0	0	0	0	0	0	IFE			
2D	0000	GPIOF	GPIOF_ SLEW	0	0	0	0	0	0	0	0	0	0	0	0	SLEW			
2E–3F	—	GPIOF	Reserved	RESERVED															

Table 44. Detailed Peripheral Memory Map (continued)

Offset Addr. (Hex)	Reset Value (Hex)	Periph.	Register	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Bit 0
4E	0000	SIM	SIM_GPSC	0	0	0	0	0	0	0	0	0	0	0	0	0	0	GPS_C6	GPS_C0
4F	0000	SIM	SIM_GPSD	0	0	0	0	0	0	0	GPS_D3		GPS_D2		GPS_D1		GPS_D0		
50	0000	SIM	SIM_IPS0	0	0	0	0	IPS_FAULT3	IPS_FAULT2	IPS_FAULT1	IPS_PSRC2		IPS_PSRC1		IPS_PSRC0				
51	0000	SIM	SIM_IPS1	0	IPS_C2_WS			IPS_C1_WS			IPS_C0_WS		IPS_T1		IPS_T0				
52–5F	—	SIM	Reserved	RESERVED															
60	0208	PMC	PMC_SCR	OORF	LVDF	PPDF	PORF	OORIE	LVDIE	LVDRE	PPDE	LPR	LPRS	LPWUI	BGBE	LVDE	LVLS	PROT	
61	00--[2]	PMC	PMC_CR2	0	0	0	0	0	0	0	LPO_EN	LPO_TRIM			TRIM				
7F	—	PMC	Reserved	RESERVED															
80	0000	CMP0	CMP0_ CR0	0	0	0	0	0	0	0	0	0	FILTER_CNT			PMC		MMC	
81	0000	CMP0	CMP0_ CR1	0	0	0	0	0	0	0	0	SE	WE	0	PMODE	INV	COS	OPE	EN
82	0000	CMP0	CMP0_ FPR	0	0	0	0	0	0	0	0	FILT_PER							
83	0000	CMP0	CMP0_ SCR	0	0	0	0	0	0	0	0	0	0	0	IER	IEF	CFR	CFF	COUT
84–9F	—	CMP0	Reserved	RESERVED															
A0	0000	CMP1	CMP1_ CR0	0	0	0	0	0	0	0	0	0	FILTER_CNT			PMC		MMC	

Table 44. Detailed Peripheral Memory Map (continued)

Offset Addr. (Hex)	Reset Value (Hex)	Periph.	Register	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Bit 0
02	0000	PDB	PDB_ DELAYB	DELAYB															
03	FFFF	PDB	PDB_MOD	MOD															
04	FFFF	PDB	PDB_ COUNT	COUNT															
05–1F	—	PDB	Reserved	RESERVED															
20	0000	RTC	RTC_SC	0	0	0	0	0	0	0	0	RTIF	RTCLKS		RTIE	RTCPS			
21	0000	RTC	RTC_CNT	0	0	0	0	0	0	0	0	RTCCNT							
22	0000	RTC	RTC_MOD	0	0	0	0	0	0	0	0	RTCMOD							
23–FF	—	RTC	Reserved	RESERVED															
00	0000	HFM	FM_ CLKDIV	0	0	0	0	0	0	0	0	DIVLD	PRDIV8	DIV					
01	0000	HFM	FM_CNFG	0	0	0	0	0	LOCK	0	AEIE	CBEIE	CCIE	KEYACC	0	0	0	LBTS	BTS
03	-000[3]	HFM	FM_SECHI	KEYEN	SECSTAT	0	0	0	0	0	0	0	0	0	0	0	0	0	0
04	0000	HFM	FM_ SECLO	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SEC	
06–0F	—	HFM	Reserved	RESERVED															
10	FFFF[6]	HFM	FM_PROT	PROTECT															
11	—	HFM	Reserved	RESERVED															
13	00C0	HFM	FM_USTAT	0	0	0	0	0	0	0	0	CBEIF	CCIF	PVIOL	ACCERR	0	BLANK	0	0
14	0000	HFM	FM_CMD	0	0	0	0	0	0	0	0	0	CMD						

Table 44. Detailed Peripheral Memory Map (continued)

Offset Addr. (Hex)	Reset Value (Hex)	Periph.	Register	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Bit 0
17	—	HFM	Reserved	RESERVED															
18	0000	HFM	FM_DATA	FMDATA															
19	—	HFM	Reserved	RESERVED															
1A	FFFF[4]	HFM	FM_OPT0	IFR_OPT0															
1B	FFFF[5]	HFM	FM_OPT1	IFR_OPT1															
1D	FFFF[6]	HFM	FM_ TSTSIG	TST_AREA_SIG															
1E–3F	—	HFM	Reserved	RESERVED															

1 The binary reset value of this register is 0000 0000 0UUU UUUU, where U represents an undefined value. Spaces have been added to the value for clarity.

2 The binary reset value of this register is 0000 0000 111NC NC NC NC NC. Spaces have been added to the value for clarity.

3 The binary reset value of this register is FS00 0000 0000 0000, where F indicates that the reset state is loaded from the flash array during reset, and where S indicates that the reset state is determined by the security state of the module. Spaces have been added to the value for clarity.

4 The reset state is loaded from the flash array during reset.

5 The reset state is loaded from the flash array during reset.

6 The reset state is loaded from the flash array during reset.