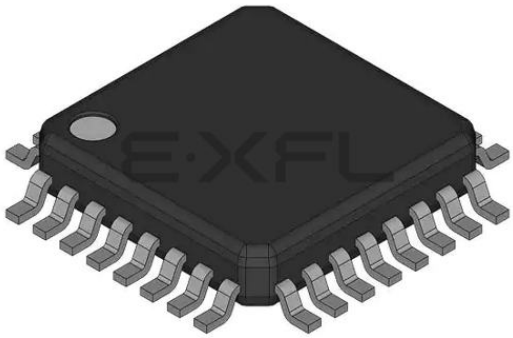

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	56800E
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	27
Program Memory Size	16KB (8K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 16
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 18x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc56f8006mlc

- Parallel instruction set with unique DSP addressing modes
- Hardware DO and REP loops
- Three internal address buses
- Four internal data buses
- Instruction set supports DSP and controller functions
- Controller-style addressing modes and instructions for compact code
- Efficient C compiler and local variable support
- Software subroutine and interrupt stack with depth limited only by memory
- JTAG/enhanced on-chip emulation (EOnCE) for unobtrusive, processor speed–independent, real-time debugging

3.1.2 Operation Range

- 1.8 V to 3.6 V operation (power supplies and I/O)
- From power-on-reset: approximately 1.9 V to 3.6 V
- Ambient temperature operating range:
  - –40 °C to 125 °C

3.1.3 Memory

- Dual Harvard architecture permits as many as three simultaneous accesses to program and data memory
- Flash security and protection that prevent unauthorized users from gaining access to the internal flash
- On-chip memory
  - 16 KB of program flash for 56F8006 and 12 KB of program flash for 56F8002
  - 2 KB of unified data/program RAM
- EEPROM emulation capability using flash

3.1.4 Interrupt Controller

- Five interrupt priority levels
  - Three user programmable priority levels for each interrupt source: Level 0, 1, 2
  - Unmaskable level 3 interrupts include: illegal instruction, hardware stack overflow, misaligned data access, SWI3 instruction. Maskable level 3 interrupts include: EOnCE step counter, EOnCE breakpoint unit, EOnCE trace buffer
  - Lowest-priority software interrupt: level LP
- Allow nested interrupt that higher priority level interrupt request can interrupt lower priority interrupt subroutine
- The masking of interrupt priority level is managed by the 56800E core
- One programmable fast interrupt that can be assigned to any interrupt source
- Notification to system integration module (SIM) to restart clock out of wait and stop states
- Ability to relocate interrupt vector table

3.1.5 Peripheral Highlights

- One multi-function, six-output pulse width modulator (PWM) module
  - Up to 96 MHz PWM operating clock
  - 15 bits of resolution
  - Center-aligned and edge-aligned PWM signal mode
  - Phase shifting PWM pulse generation

- Clock sources
  - On-chip relaxation oscillator with two user selectable frequencies: 400 kHz for low speed mode, 8 MHz for normal operation
  - On-chip low-power 1 kHz oscillator can be selected as clock source to the RTC and/or COP
  - External clock: crystal oscillator, ceramic resonator, and external clock source
- Power management controller (PMC)
  - On-chip regulator for digital and analog circuitry to lower cost and reduce noise
  - Integrated power-on reset (POR)
  - Low-voltage interrupt with a user selectable trip voltage of 1.81 V or 2.31 V
  - User selectable brown-out reset
  - Run, wait, and stop modes
  - Low-power run, wait, and stop modes
  - Partial power down mode
- Up to 40 general-purpose I/O (GPIO) pins
  - Individual control for each pin to be in peripheral or GPIO mode
  - Individual input/output direction control for each pin in GPIO mode
  - Hysteresis and configurable pullup device on all input pins
  - Configurable slew rate and drive strength and optional input low pass filters on all output pins
  - 20 mA sink/source current
- JTAG/EOnCE debug programming interface for real-time debugging
  - IEEE 1149.1 Joint Test Action Group (JTAG) interface
  - EOnCE interface for real-time debugging

3.1.6 Power Saving Features

- Three low power modes
  - Low-speed run, wait, and stop modes: 200 kHz IP bus clock provided by ROSC
  - Low-power run, wait, and stop modes: clock provided by external 32–38.4 kHz crystal
  - Partial power down mode
- Low power external oscillator can be used in any low-power mode to provide accurate clock to active peripherals
- Low power real time counter for use in run, wait, and stop modes with internal and external clock sources
- 32 µs typical wakeup time from partial power down modes
- Each peripheral can be individually disabled to save power

3.2 Award-Winning Development Environment

Processor Expert™ (PE) provides a Rapid Application Design (RAD) tool that combines easy-to-use component-based software application creation with an expert knowledge system.

The CodeWarrior Integrated Development Environment is a sophisticated tool for code navigation, compiling, and debugging. A complete set of evaluation modules (EVMs), demonstration board kit, and development system cards support concurrent engineering. Together, PE, CodeWarrior, and EVMs create a complete, scalable tools solution for easy, fast, and efficient development.

A full set of programmable peripherals — PWM, PGAs, ADCs, SCI, SPI, I^2C, PIT, timers, and analog comparators — supports various applications. Each peripheral can be independently shut down to save power. Any pin in these peripherals can also be used as general-purpose input/outputs (GPIOs).

3.3 Architecture Block Diagram

The 56F8006/56F8002's architecture is shown in Figure 2 and Figure 3. Figure 2 illustrates how the 56800E system buses communicate with internal memories and the IPBus interface and the internal connections among each unit of the 56800E core. Figure 3 shows the peripherals and control blocks connected to the IPBus bridge. Please see the system integration module (SIM) section in the *MC56F8006 Reference Manual* for information about which signals are multiplexed with those of other peripherals.

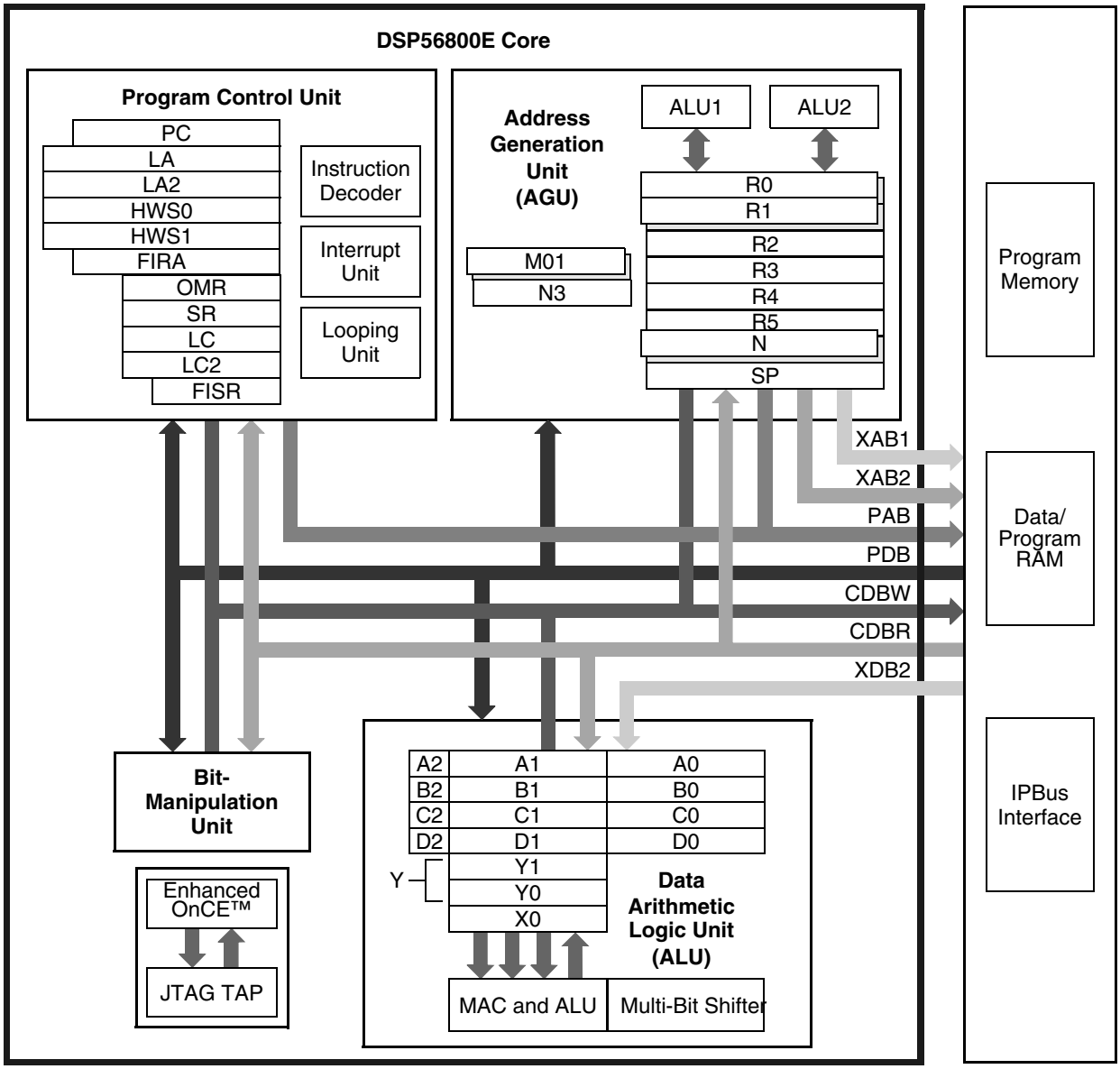


Figure 2. 56800E Core Block Diagram

3.4 Product Documentation

The documents listed in Table 2 are required for a complete description and proper design with the 56F8006/56F8002. Documentation is available from local Freescale distributors, Freescale Semiconductor sales offices, Freescale Literature Distribution Centers, or online at http://www.freescale.com.

Table 2. 56F8006/56F8002 Device Documentation

Topic	Description	Order Number
DSP56800E Reference Manual	Detailed description of the 56800E family architecture, 16-bit digital signal controller core processor, and the instruction set	DSP56800ERM
56F800x Peripheral Reference Manual	Detailed description of peripherals of the 56F8006 and 56F8002 devices	MC56F8006RM
56F80x Serial Bootloader User Guide	Detailed description of the Serial Bootloader in the 56F800x family of devices	TBD
56F8006/56F8002 Technical Data Sheet	Electrical and timing specifications, pin descriptions, and package descriptions (this document)	MC56F8006
56F8006/56F8002 Errata	Details any chip issues that might be present	MC56F8006E

4 Signal/Connection Descriptions

4.1 Introduction

The input and output signals of the 56F8006/56F8002 are organized into functional groups, as detailed in Table 3. Table 4 summarizes all device pins. In Table 4, each table row describes the signal or signals present on a pin, sorted by pin number.

Table 3. Functional Group Pin Allocations

Functional Group	Number of Pins in 28 SOIC	Number of Pins in 32 LQFP	Number of Pins in 32 PSDIP	Number of Pins in 48 LQFP
Power Inputs (V_{DD}, V_{DDA})	2	2	2	4
Ground (V_{SS}, V_{SSA})	3	3	3	4
Reset[1]	1	1	1	1
Pulse Width Modulator (PWM) Ports[1]	10	12	12	12
Serial Peripheral Interface (SPI) Ports[1]	5	7	7	7
Serial Communications Interface 0 (SCI) Ports[1]	4	5	5	5
Inter-Integrated Circuit Interface (I^2C) Ports[1]	6	7	7	7
Analog-to-Digital Converter (ADC) Inputs[1]	16	18	18	24
High Speed Analog Comparator Inputs[1]	13	15	15	25
Programmable Gain Amplifiers (PGA)[1]	4	4	4	4
Dual Timer Module (TMR) Ports[1]	8	10	10	10
Programmable Delay Block (PDB)[1]	—	—	—	1
Clock[1]	5	5	5	5
JTAG/Enhanced On-Chip Emulation (EOnCE[1])	4	4	4	4

[1] Pins may be shared with other peripherals. See Table 4.

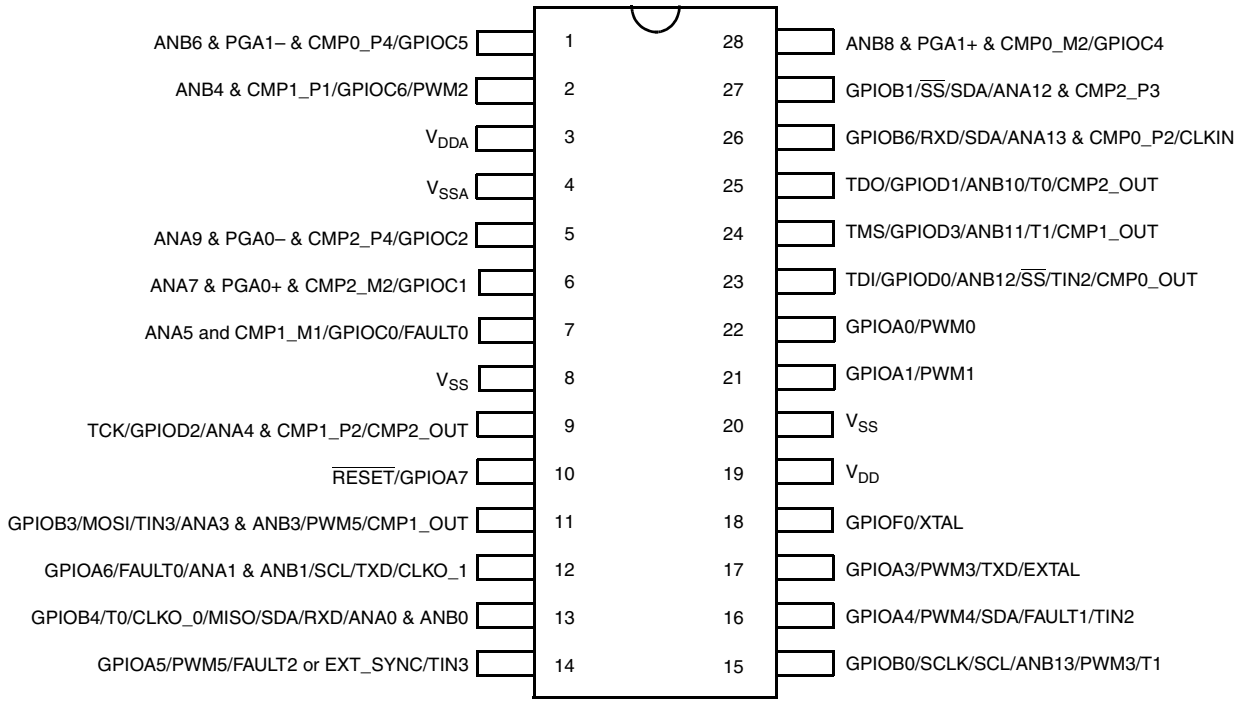


Figure 4. Top View, MC56F8006/MC56F8002 28-Pin SOIC Package

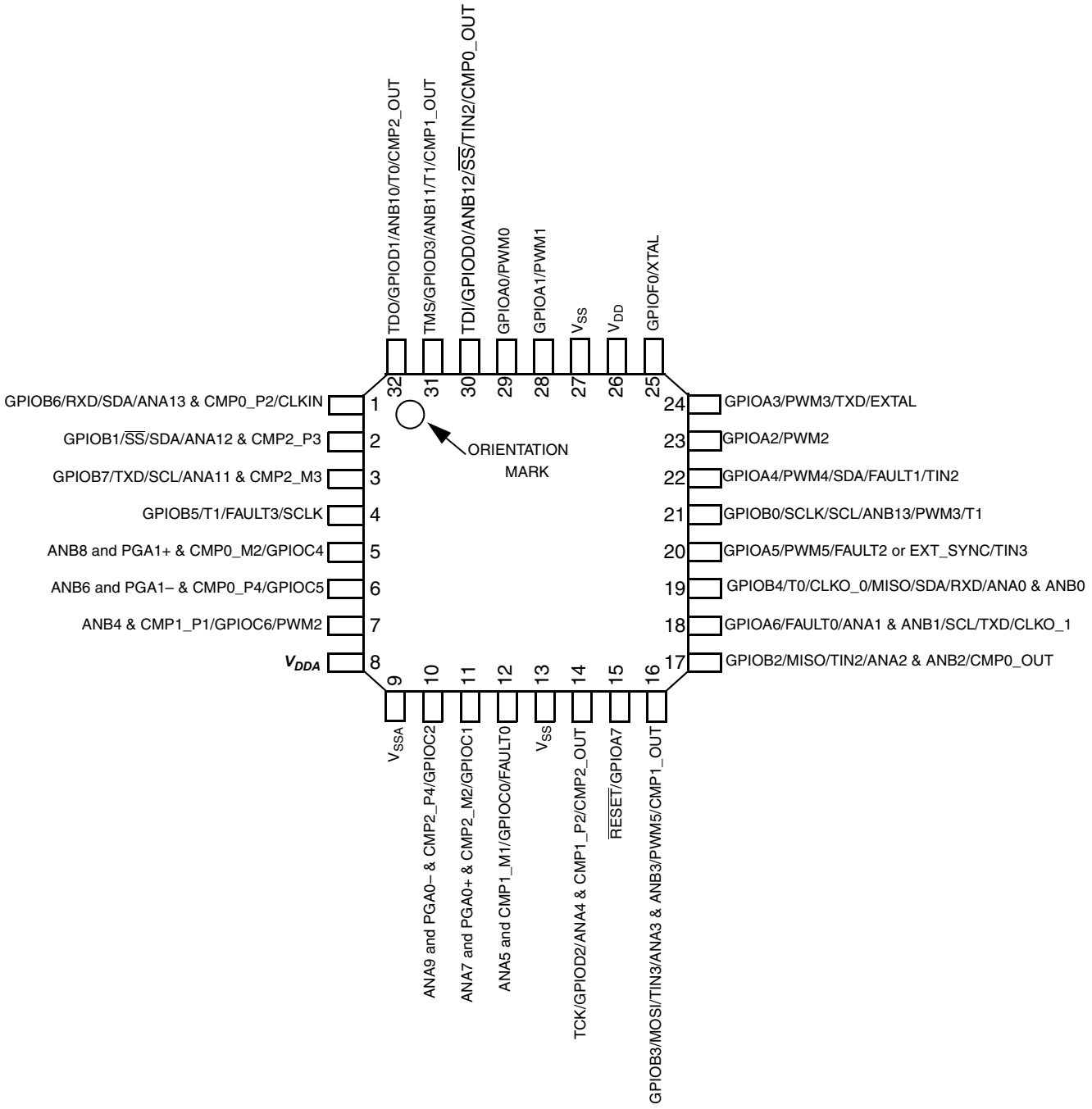


Figure 5. Top View, MC56F8006 32-Pin LQFP Package

Table 5. 56F8006/56F8002 Signal and Package Information (continued)

Signal Name	28 SOIC	32 LQFP	32 PSDIP	48 LQFP	Type	State During Reset	Signal Description
GPIOA3	17	24	20	36	Input/ Output	Input, internal pullup enabled	Port A GPIO — This GPIO pin can be individually programmed as an input or output pin.
(PWM3)					Output		PWM3 — The PWM channel 3.
(TXD)					Output		TXD — The SCI transmit data output or transmit/receive in single wire operation.
(EXTAL)					Analog Input		EXTAL — External Crystal Oscillator Input. This input can be connected to a 32.768 kHz or 1–16 MHz external crystal or ceramic resonator. When used to supply a source to the internal PLL, the crystal/resonator must be in the 4 MHz to 8 MHz range. Tie this pin low or configure as GPIO if XTAL is being driven by an external clock source. If using a 32.768 kHz crystal, place the crystal as close as possible to device pins to speed startup. After reset, the default state is GPIOA3.
GPIOA4	16	22	18	33	Input/ Output	Input, internal pullup enabled	Port A GPIO — This GPIO pin can be individually programmed as an input or output pin.
(PWM4)					Output		PWM4 — The PWM channel 4.
(SDA)					Input/Open-drain Output		SDA — The I^2C serial data line.
(FAULT1)					Input		FAULT1 — PWM fault input 1used for disabling selected PWM outputs in cases where fault conditions originate off-chip.
(TIN2)					Input		TIN2 — Dual timer module channel 2 input After reset, the default state is GPIOA4.
GPIOA5	14	20	16	29	Input/ Output	Input, internal pullup enabled	Port A GPIO — This GPIO pin can be individually programmed as an input or output pin.
(PWM5)					Output		PWM5 — The PWM channel 5.
(FAULT2/ EXT_SYNC)					Input/ Output		FAULT2 — PWM fault input 2 used for disabling selected PWM outputs in cases where fault conditions originate off-chip. EXT_SYNC — When not being used as a fault input, this pin can be used to receive a pulse to reset the PWM counter or to generate a positive pulse at the start of every PWM cycle.
(TIN3)					Input		TIN3 — Dual timer module channel 3 input After reset, the default state is GPIOA5.

Table 5. 56F8006/56F8002 Signal and Package Information (continued)

Signal Name	28 SOIC	32 LQFP	32 PSDIP	48 LQFP	Type	State During Reset	Signal Description
GPIOA6	12	18	14	26	Input/ Output	Input, internal pullup enabled	Port A GPIO — This GPIO pin can be individually programmed as an input or output pin.
(FAULT0)					Input		FAULT0 — PWM fault input 0 used for disabling selected PWM outputs in cases where fault conditions originate off-chip.
(ANA1 & ANB1)					Analog Input		ANA1 and ANB1 — Analog input to channel 1 of ADCA and ADCB.
(SCL)					Input/Open-drain Output		SCL — The I^2C serial clock
(TXD)					Output		TXD — The SCI transmit data output or transmit/receive in single wire operation.
(CLKO_1)					Output		CLKO_1 — This is a buffered clock output; the clock source is selected by clockout select (CLKOSEL) bits in the clock output select register (CLKOUT) in the SIM. When used as an analog input, the signal goes to the ANA1 and ANB1. After reset, the default state is GPIOA6.
GPIOB0	15	21	17	32	Input/ Output	Input, internal pullup enabled	Port B GPIO — This GPIO pin can be individually programmed as an input or output pin.
(SCLK)					Input/ Output		SCLK — The SPI serial clock. In master mode, this pin serves as an output, clocking slaved listeners. In slave mode, this pin serves as the data clock input.
(SCL)					Input/Open-drain Output		SCL — The I^2C serial clock.
(ANB13)					Analog Input		ANB13 — Analog input to channel 13 of ADCB
(PWM3)					Output		PWM3 — The PWM channel 3.
(T1)					Input/ Output		T1 — Dual timer module channel 1 input/output. After reset, the default state is GPIOB0.

- Provides a 3X system clock that operates at three times the system clock to PWM, timer, and SCI modules
- Safety shutdown feature is available if the PLL reference clock is lost
- Can be driven from an external clock source

The clock generation module provides the programming interface for the PLL, internal relaxation oscillator, and crystal oscillator. It also provides a postscaler to divide clock frequency down by 1, 2, 4, 8, 16, 32, 64, 128, 256 before feeding to the SIM. The SIM is responsible for further dividing these frequencies by two, which ensures a 50% duty cycle in the system clock output. For detail, see the OCCS chapter in the *MC56F8006 Peripheral Reference Manual*.

6.4.1 Internal Clock Source

An internal relaxation oscillator can supply the reference frequency when an external frequency source or crystal is not used. It is optimized for accuracy and programmability while providing several power-saving configurations that accommodate different operating conditions. The internal relaxation oscillator has little temperature and voltage variability. To optimize power, the internal relaxation oscillator supports a run state (8 MHz), standby state (400 kHz), and a power-down state.

During a boot or reset sequence, the relaxation oscillator is enabled by default (the PRECS bit in the PLLCR word is set to 0). Application code can then also switch to the external clock source and power down the internal oscillator, if desired. If a changeover between internal and external clock sources is required at power-on, ensure that the clock source is not switched until the desired external clock source is enabled and stable.

To compensate for variances in the device manufacturing process, the accuracy of the relaxation oscillator can be incrementally adjusted to within + 0.078% of 8 MHz by trimming an internal capacitor. Bits 0–9 of the OSCTL (oscillator control) register allow you to set in an additional offset (trim) to this preset value to increase or decrease capacitance. Each unit added or subtracted changes the output frequency by about 0.078% of 8 MHz, allowing incremental adjustment until the desired frequency accuracy is achieved.

The center frequency of the internal oscillator is calibrated at the factory to 8 MHz and the TRIM value is stored in the flash information block and loaded to the FMOPT1 register at reset. When using the relaxation oscillator, the boot code should read the FMOPT1 register and set this value as OSCTL TRIM. For further information, see the *MC56F8006 Peripheral Reference Manual*.

6.4.2 Crystal Oscillator/Ceramic Resonator

The internal crystal oscillator circuit is designed to interface with a parallel-resonant crystal resonator in the frequency range, specified for the external crystal, of 32.768 kHz (Typ) or 1–16 MHz. A ceramic resonator can be substituted for the 1–16 MHz range. When used to supply a source to the internal PLL, the recommended crystal/resonator is in the 4 MHz to 8 MHz (recommend 8 MHz) range to achieve optimized PLL performance. Oscillator circuits are shown in Figure 10, Figure 11, and Figure 12. Follow the crystal supplier's recommendations when selecting a crystal, because crystal parameters determine the component values required to provide maximum stability and reliable start-up. The load capacitance values used in the oscillator circuit design should include all stray layout capacitances. The crystal and associated components should be mounted as near as possible to the EXTAL and XTAL pins to minimize output distortion and start-up stabilization time. When using low-frequency, low-power mode, the only external component is the crystal itself. In the other oscillator modes, load capacitors (C_x, C_y) and feedback resistor (R_F) are required. In addition, a series resistor (R_S) may be used in high-gain modes. Recommended component values are listed in Table 28.

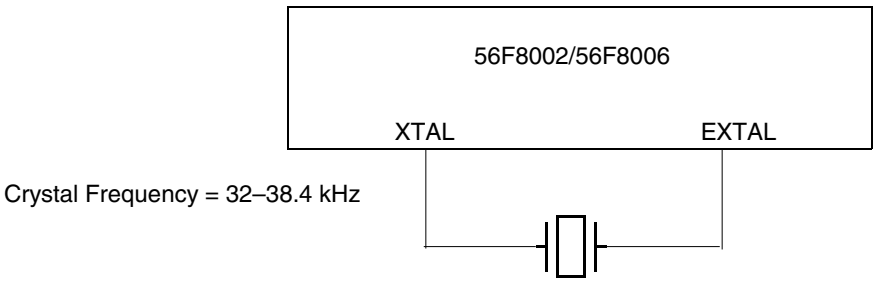


Figure 10. Typical Crystal Oscillator Circuit: Low-Range, Low-Power Mode

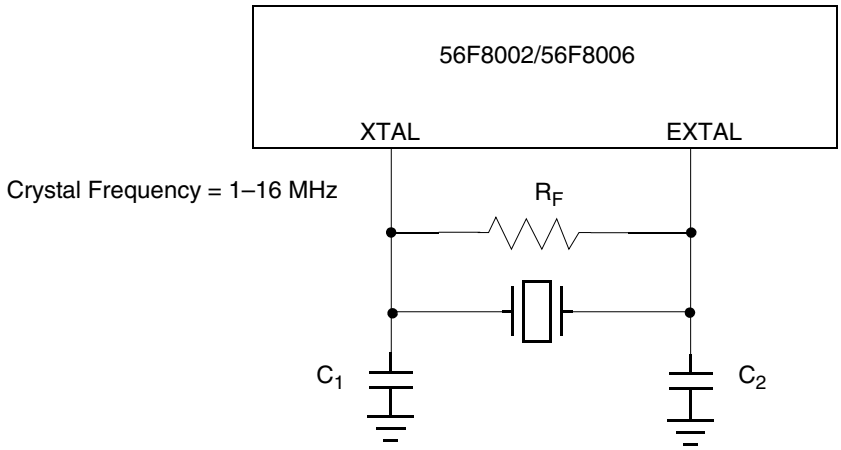


Figure 11. Typical Crystal or Ceramic Resonator Circuit: High-Range, Low-Power Mode

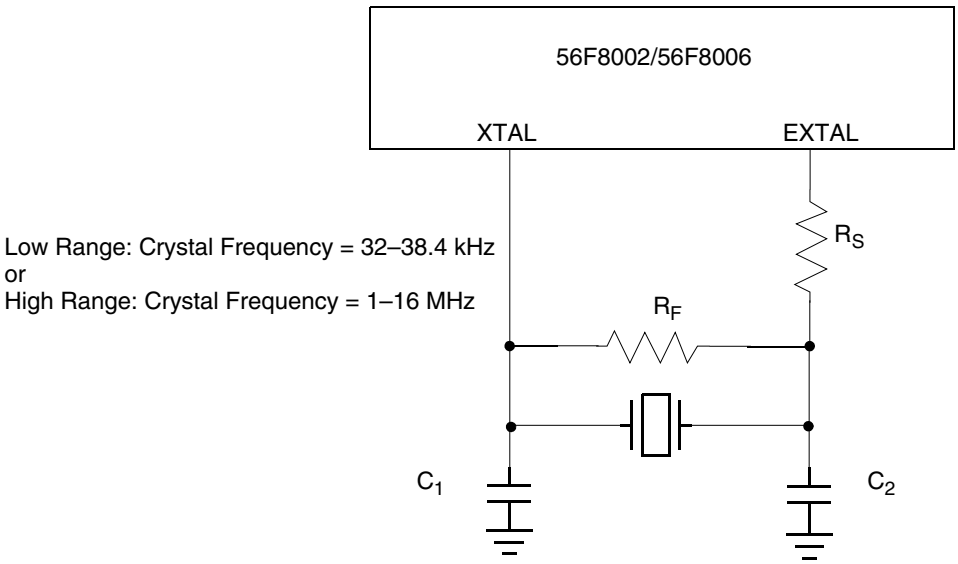


Figure 12. Typical Crystal or Ceramic Resonator Circuit: Low Range and High Range, High-Gain Mode

6.4.3 External Clock Input — Crystal Oscillator Option

The recommended method of connecting an external clock is illustrated in Figure 13. The external clock source is connected to XTAL and the EXTAL pin is grounded or configured as GPIO while CLK_MOD bit in OSCTL register is set. The external clock input must be generated using a relatively low impedance driver with maximum frequency less than 8 MHz.

- Registers containing the JTAG ID of the chip
- Controls for programmable peripheral and GPIO connections
- Peripheral clocks for TMR and PWM and SCI with a high-speed (3X) option
- Power-saving clock gating for peripherals
- Controls the enable/disable functions of large regulator standby mode with write protection capability
- Permits selected peripherals to run in stop mode to generate stop recovery interrupts
- Controls for programmable peripheral and GPIO connections
- Software chip reset
- I/O short address base location control
- Peripheral protection control to provide runaway code protection for safety-critical applications
- Controls output of internal clock sources to CLKO pin
- Four general-purpose software control registers are reset only at power-on
- Peripherals stop mode clocking control

6.7 PWM, PDB, PGA, and ADC Connections

The comparators, timers, and PWM_reload_sync output can be connected to the programmable delay block (PDB) trigger input. The PDB pre-trigger A and trigger A outputs are connected to the ADCA and PGA0 hardware trigger inputs. The PDB pre-trigger B and trigger B outputs are connected to the ADCB and PGA1 hardware trigger inputs. When the input trigger of PDB is asserted, PDB trigger and pre-trigger outputs are asserted after a delay of a pre-programmed period. See the *MC56F8006 Peripheral Reference Manual* for additional information.

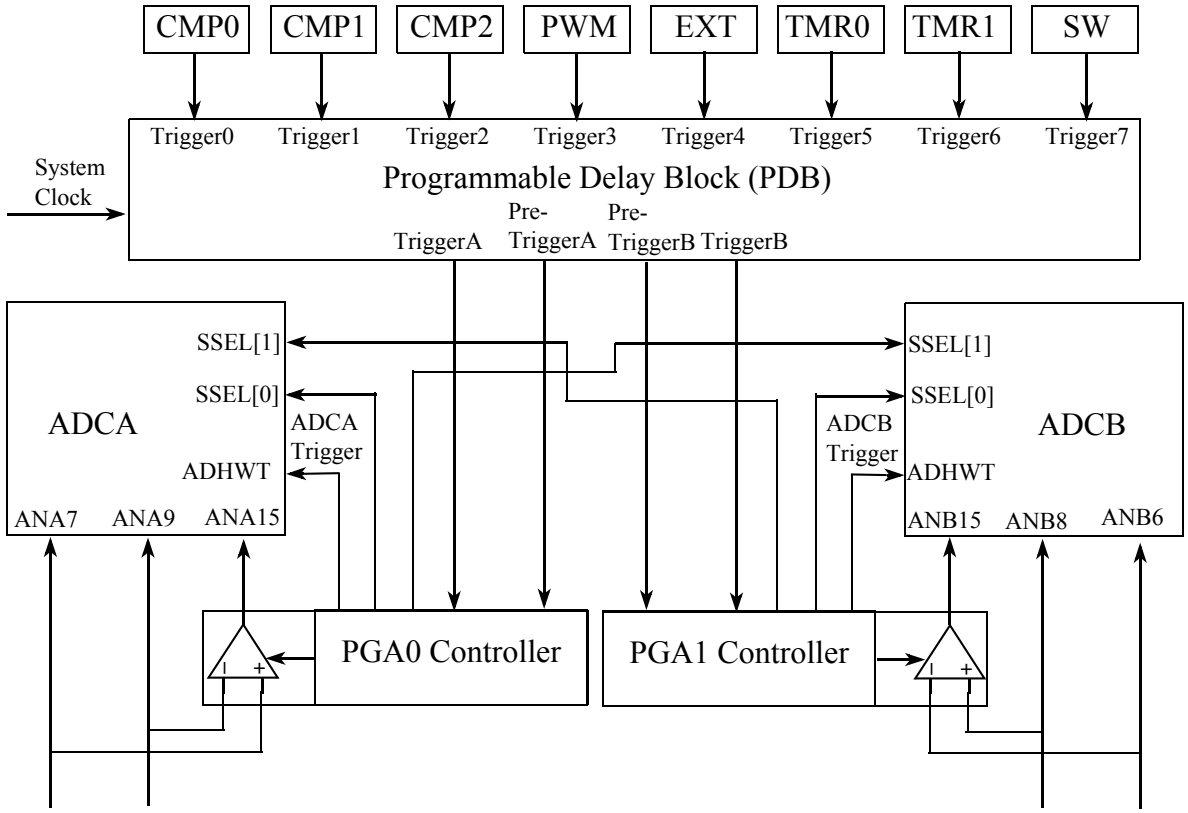


Figure 15. Synchronization of ADC, PDB

Table 15. 28SOIC Package Thermal Characteristics (continued)

Characteristic	Comments	Symbol	Value (LQFP)	Unit
Junction to ambient (@200 ft/min)	Four layer board (2s2p)	$R_{\theta JMA}$	42	°C/W
Junction to board		$R_{\theta JB}$	23	°C/W
Junction to case		$R_{\theta JC}$	26	°C/W
Junction to package top	Natural Convection	Ψ_{JT}	9	°C/W

Table 16. 32LQFP Package Thermal Characteristics

Characteristic	Comments	Symbol	Value (LQFP)	Unit
Junction to ambient Natural convection	Single layer board (1s)	$R_{\theta JA}$	84	°C/W
Junction to ambient Natural convection	Four layer board (2s2p)	$R_{\theta JMA}$	56	°C/W
Junction to ambient (@200 ft/min)	Single layer board (1s)	$R_{\theta JMA}$	70	°C/W
Junction to ambient (@200 ft/min)	Four layer board (2s2p)	$R_{\theta JMA}$	49	°C/W
Junction to board		$R_{\theta JB}$	33	°C/W
Junction to case		$R_{\theta JC}$	20	°C/W
Junction to package top	Natural convection	Ψ_{JT}	4	°C/W

Table 17. 32PSDIP Package Thermal Characteristics

Characteristic	Comments	Symbol	Value (LQFP)	Unit
Junction to ambient Natural convection	Single layer board (1s)	$R_{\theta JA}$	56	°C/W
Junction to ambient Natural convection	Four layer board (2s2p)	$R_{\theta JMA}$	41	°C/W
Junction to ambient (@200 ft/min)	Single layer board (1s)	$R_{\theta JMA}$	45	°C/W
Junction to ambient (@200 ft/min)	Four layer board (2s2p)	$R_{\theta JMA}$	36	°C/W
Junction to board		$R_{\theta JB}$	18	°C/W
Junction to case		$R_{\theta JC}$	24	°C/W
Junction to package top	Natural convection	Ψ_{JT}	10	°C/W

Table 28. Crystal Oscillator Characteristics

Characteristic	Symbol	Min	Typ[1]	Max	Unit
Oscillator crystal or resonator (PRECS = 1, CLK_MOD = 0) Low range (RANGE = 0) High range (RANGE = 1), high gain (COHL =0) High range (RANGE = 1), low power (COHL =1)	 f_{lo} f_{hi} f_{hi}	 32 1 1	 — — —	 38.4 16 8	 kHz MHz MHz
Load capacitors Low range (RANGE=0), low power (COHL =1) Other oscillator settings	C_1, C_2	See Note[2] See Note[3]			
Feedback resistor Low range, low power (RANGE=0, COHL =1)[2] Low range, high gain (RANGE=0, COHL =0) High range (RANGE=1, COHL=X)	R_F	 — — —	 — 10 1	 — — —	MΩ
Series resistor Low range, low power (RANGE = 0, COHL =1)[2] Low range, high gain (RANGE = 0, COHL =0) High range, low power (RANGE = 1, COHL =1) High range, high gain (RANGE = 1,COHL =0) ≥ 8 MHz 4 MHz 1 MHz	R_S	 — — — — — —	 0 100 0 0 0 0	 — — — 0 10 20	kΩ
Crystal start-up time [4] Low range, low power Low range, high gain High range, low power High range, high gain	 t_{CSTL} t_{CSTH}	 — — — —	 TBD TBD TBD TBD	 — — — —	ms
Square wave input clock frequency (PRECS = 1, CLK_MOD = 1)	f_{xtal}	—	—	50.0	MHz

1 Data in Typical column was characterized at 3.0 V, 25°C or is typical recommended value.

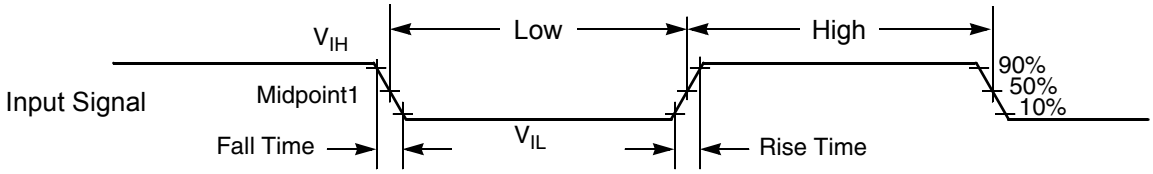
2 Load capacitors (C_1,C_2), feedback resistor (R_F) and series resistor (R_S) are incorporated internally when RANGE=HGO=0.

3 See crystal or resonator manufacturer's recommendation.

4 Proper PC board layout procedures must be followed to achieve specifications.

8.13 AC Electrical Characteristics

Tests are conducted using the input levels specified in Table 22. Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured between the 10% and 90% points, as shown in Figure 25.



The midpoint is $V_{IL} + (V_{IH} - V_{IL})/2$.

Figure 25. Input Signal Measurement References

Figure 26 shows the definitions of the following signal states:

- Active state, when a bus or signal is driven, and enters a low impedance state

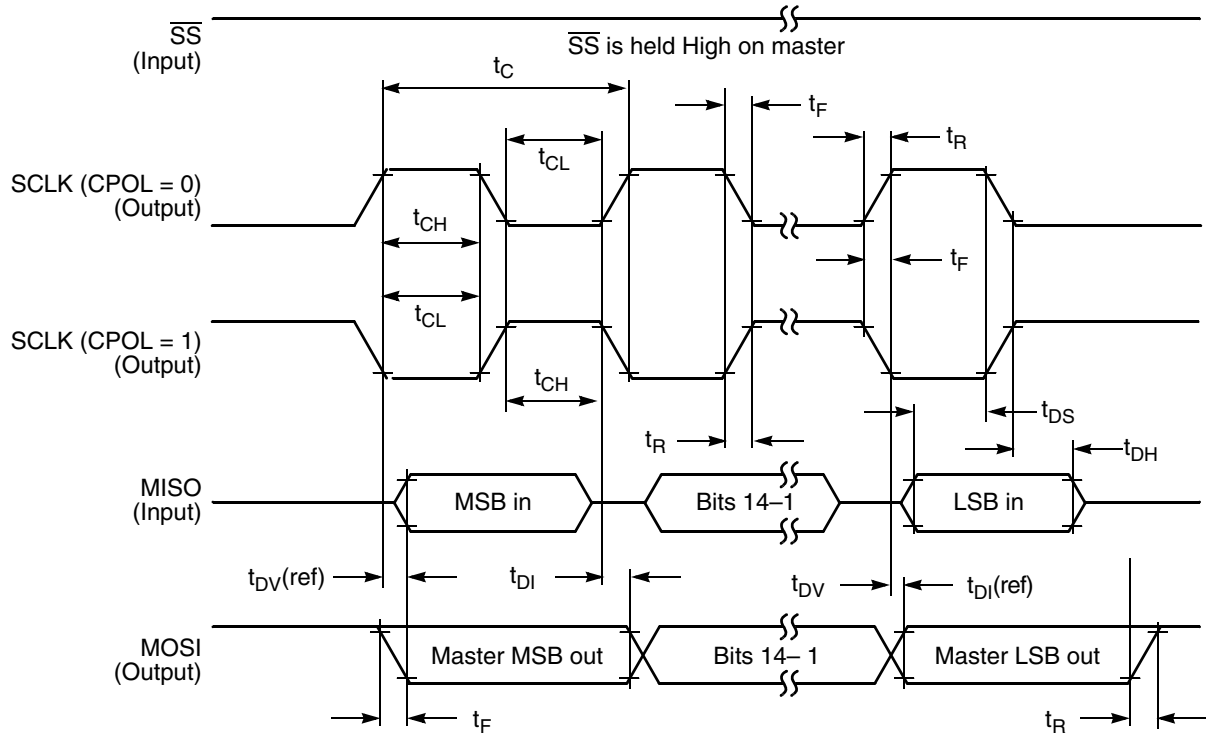


Figure 28. SPI Master Timing (CPHA = 1)

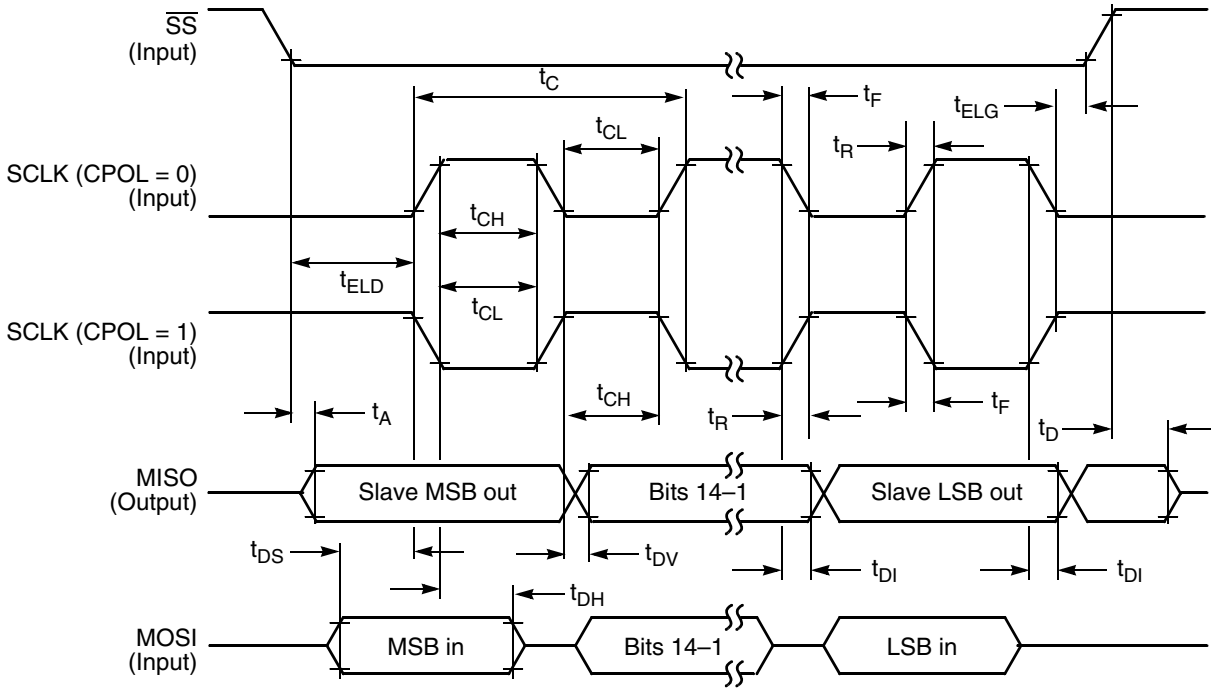


Figure 29. SPI Slave Timing (CPHA = 0)

9.3 Ordering Information

Table 40 lists the pertinent information needed to place an order. Consult a Freescale Semiconductor sales office or authorized distributor to determine availability and to order devices.

Table 40. 56F8006/56F8002 Ordering Information

Device	Supply Voltage	Package Type	Pin Count	Frequency (MHz)	Ambient Temperature Range	Order Number
MC56F8002	1.8–3.6 V	Small Outline IC (SOIC)	28	32	–40° to + 105° C –40° to + 125° C	MC56F8002VWL MC56F8002MWL[1]
MC56F8006	1.8–3.6 V	Small Outline IC (SOIC)	28	32	–40° to + 105° C –40° to + 125° C	MC56F8006VWL MC56F8006MWL[1]
MC56F8006	1.8–3.6 V	Low-Profile Quad Flat Pack (LQFP)	32	32	–40° to + 105° C –40° to + 125° C	MC56F8006VLC MC56F8006MLC[1]
MC56F8006	1.8–3.6 V	Low-Profile Quad Flat Pack (LQFP)	48	32	–40° to + 105° C –40° to + 125° C	MC56F8006VLF MC56F8006MLF[1]
MC56F8006	1.8–3.6 V	Plastic Shrink Dual In-line Package (PSDIP)	32	32	–40° to + 105° C	MC56F8006VBM

[1] This package is RoHS compliant.

Table 43. Interrupt Vector Table Contents[1]

Peripheral	Vector Number	User Encoding	Priority Level	Vector Base Address +	Interrupt Function
Core				P:0x00	Reserved for Reset Overlay[2]
Core				P:0x02	Reserved for COP Reset Overlay
Core	2	N/A	3	P:0x04	Illegal Instruction
Core	3	N/A	3	P:0x06	HW Stack Overflow
Core	4	N/A	3	P:0x08	Misaligned Long Word Access
Core	5	N/A	3	P:0x0A	EOnCE Step Counter
Core	6	N/A	3	P:0x0C	EOnCE Breakpoint Unit
Core	7	N/A	3	P:0x0E	EOnCE Trace Buffer
Core	9	N/A	3	P:0x10	EOnCE Transmit Register Empty
Core	9	N/A	3	P:0x12	EOnCE Receive Register Full
PMC	10	0x0A	0	P:0x14	Low-Voltage Detector
PLL	11	0x0B	0	P:0x16	Phase-Locked Loop Loss of Locks and Loss of Clock
ADCA	12	0x0C	0	P:0x18	ADCA Conversion Complete
ADCB	13	0x0D	0	P:0x1A	ADCB Conversion Complete
PWM	14	0x0E	0	P:0x1C	Reload PWM and/or PWM Faults
CMP0	15	0x0F	0	P:0x1E	Comparator 0 Rising/Falling Flag
CMP1	16	0x10	0	P:0x20	Comparator 1 Rising/Falling Flag
CMP2	17	0x11	0	P:0x22	Comparator 2 Rising/Falling Flag
FM	18	0x12	0	P:0x24	Flash Memory Access Status
SPI	19	0x13	0	P:0x26	SPI Receiver Full
SPI	20	0x14	0	P:0x28	SPI Transmitter Empty
SCI	21	0x15	0	P:0x2A	SCI Transmitter Empty/Idle
SCI	22	0x16	0	P:0x2C	SCI Receiver Full/Overrun/Errors
I^2C	23	0x17	0	P:0x2E	I^2C Interrupt
PIT	24	0x18	0	P:0x30	Interval Timer Interrupt
TMR0	25	0x19	0	P:0x32	Dual Timer, Channel 0 Interrupt
TMR1	26	0x1A	0	P:0x34	Dual Timer, Channel 1 Interrupt
GPIOA	27	0x1B	0	P:0x36	GPIOA Interrupt
GPIOB	28	0x1C	0	P:0x38	GPIOB Interrupt
GPIOC	29	0x1D	0	P:0x3A	GPIOC Interrupt
GPIOD	30	0x1E	0	P:0x3C	GPIOD Interrupt
GPIOE	29	0x1F	0	P:0x3E	GPIOE Interrupt
GPIOF	30	0x20	0	P:0x40	GPIOF Interrupt
RTC	33	0x21	0	P:0x42	Real Time Clock

Table 44. Detailed Peripheral Memory Map (continued)

Offset Addr. (Hex)	Reset Value (Hex)	Periph.	Register	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Bit 0
29	0000	PWM	PWM_VAL3	PMVAL															
2A	0000	PWM	PWM_VAL4	PMVAL															
2B	0000	PWM	PWM_VAL5	PMVAL															
2C	0FFF	PWM	PWM_DTIM0	0	0	0	0	PWMDT0											
2D	0FFF	PWM	PWM_DTIM1	0	0	0	0	PWMDT1											
2E	FFFF	PWM	PWM_DMAP1	DISMAP_15_0															
2F	00FF	PWM	PWM_DMAP2	0	0	0	0	0	0	0	0	DISMAP_23_16							
30	0000	PWM	PWM_CNFG	0	DBG_EN	WAIT_EN	EDG	0	TOPNEG45	TOPNEG23	TOPNEG01	0	BOTNEG45	BOTNEG23	BOTNEG01	INDEP45	INDEP23	INDEP01	WP
31	0000	PWM	PWM_CCTRL	ENHA	nBX	MSK5	MSK4	MSK3	MSK2	MSK1	MSK0	0	0	VLMODE		0	SWP45	SWP23	SWP01
32	00-U[1]	PWM	PWM_PORT	0	0	0	0	0	0	0	0	0	PORT						
33	0000	PWM	PWM_ICCTRL	0	0	0	0	0	0	0	0	0	0	PEC2	PEC1	PEC0	ICC2	ICC1	ICC0
34	0000	PWM	PWM_SCTRL	0	0	CINV5	CINV4	CINV3	CINV2	CINV1	CINV0	0	SRC2		0	SRC1		0	SRC0

Table 44. Detailed Peripheral Memory Map (continued)

Offset Addr. (Hex)	Reset Value (Hex)	Periph.	Register	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Bit 0
C3	0000	PGA1	PGA1_STS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	RUNNING	STCOMP
C4–DF	—	PGA1	Reserved	RESERVED															
E0	0200	SCI	SCI_RATE	SBR													FRAC_SBR		
E1	0000	SCI	SCI_CTRL1	LOOP	SWAI	RSRC	M	WAKE	POL	PE	PT	TEIE	TIIE	RFIE	REIE	TE	RE	RWU	SBK
E2	0000	SCI	SCI_CTRL2	0	0	0	0	0	0	0	0	0	0	0	0	LIN_MODE	0	0	0
E3	C000	SCI	SCI_STAT	TDRE	TIDLE	RDRF	RIDLE	OR	NF	FE	PF	0	0	0	0	LSE	0	0	RAF
E4	0000	SCI	SCI_DATA	0	0	0	0	0	0	0	RECEIVE_TRANSMIT_DATA								
E5–FF	—	SCI	Reserved	RESERVED															
00	6141	SPI	SPI_SCTRL	SPR			DSO	ERRIE	MODFEN	SPRIE	SPMSTR	CPOL	CPHA	SPE	SPTIE	SPRF	OVRF	MODF	SPTE
01	000F	SPI	SPI_DSCTRL	WOM	0	0	BD2X	SSB_IN	SSB_DATA	SSB_ODM	SSB_AUTO	SSB_DDR	SSB_STRB	SSB_OVER	SPR3	DS			
02	0000	SPI	SPI_DRCV	R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0
03	0000	SPI	SPI_DXMIT	T15	T14	T13	T12	T11	T10	T9	T8	T7	T6	T5	T4	T3	T2	T1	T0
04–1F	—	SPI	Reserved	RESERVED															
20	0000	I2C	I2C_ADDR	0	0	0	0	0	0	0	0	AD7	AD6	AD5	AD4	AD3	AD2	AD1	0
21	0000	I2C	I2C_FREQDIV	0	0	0	0	0	0	0	0	MULT		ICR					

Table 44. Detailed Peripheral Memory Map (continued)

Offset Addr. (Hex)	Reset Value (Hex)	Periph.	Register	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Bit 0
22	0000	I2C	I2C_CR1	0	0	0	0	0	0	0	0	IICEN	IICIE	MST	TX	TXAK	RSTA	0	0
23	0080	I2C	I2C_SR	0	0	0	0	0	0	0	0	TCF	IAAS	BUSY	ARBL	0	SRW	IICIF	RXAK
24	0000	I2C	I2C_DATA	0	0	0	0	0	0	0	0	DATA							
25	0000	I2C	I2C_CR2	0	0	0	0	0	0	0	0	GCAEN	ADEXT	0	0	0	AD10	AD9	AD8
26	0000	I2C	I2C_SMB_CSR	0	0	0	0	0	0	0	0	RESERVED	RESERVED	SIICAEN	TCKSEL	SLTF	SHTF	0	0
27	0000	I2C	I2C_ADDR2	0	0	0	0	0	0	0	0	SAD7	SAD6	SAD5	SAD4	SAD3	SAD2	SAD1	0
28	0000	I2C	I2C_SLT1	0	0	0	0	0	0	0	0	SSLT15	SSLT14	SSLT13	SSLT12	SSLT11	SSLT10	SSLT9	SSLT8
29	0000	I2C	I2C_SLT2	0	0	0	0	0	0	0	0	SSLT7	SSLT6	SSLT5	SSLT4	SSLT3	SSLT2	SSLT1	SSLT0
30–3F	—	I2C	Reserved	RESERVED															
40	0302	COP	COP_CTRL	0	0	0	0	0	0	PSS		0	CLKSEL		CLOREN	CSEN	CWEN	CEN	CWP
41	FFFF	COP	COP_TOUT	TIMEOUT															
42	FFFF	COP	COP_CNTR	COUNT_SERVICE															
43–5F	—	COP	Reserved	RESERVED															

Table 44. Detailed Peripheral Memory Map (continued)

Offset Addr. (Hex)	Reset Value (Hex)	Periph.	Register	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Bit 0
0D	0000	GPIOE	GPIOE_ SLEW	0	0	0	0	0	0	0	0	SLEW							
0E–1F	—	GPIOE	Reserved	RESERVED															
20	00FF	GPIOF	GPIOF_ PUR	0	0	0	0	0	0	0	0	0	0	0	0	PUR			
21	0000	GPIOF	GPIOF_DR	0	0	0	0	0	0	0	0	0	0	0	0	DR			
22	0000	GPIOF	GPIOF_ DDR	0	0	0	0	0	0	0	0	0	0	0	0	DDR			
23	0080	GPIOF	GPIOF_ PER	0	0	0	0	0	0	0	0	0	0	0	0	PER			
24	—	GPIOF	Reserved	RESERVED															
25	0000	GPIOF	GPIOF_ IENR	0	0	0	0	0	0	0	0	0	0	0	0	IENR			
26	0000	GPIOF	GPIOF_ IPOLR	0	0	0	0	0	0	0	0	0	0	0	0	IPOLR			
27	0000	GPIOF	GPIOF_ IPR	0	0	0	0	0	0	0	0	0	0	0	0	IPR			
28	0000	GPIOF	GPIOF_ IESR	0	0	0	0	0	0	0	0	0	0	0	0	IESR			
29	—	GPIOF	Reserved	RESERVED															
2A	0000	GPIOF	GPIOF_ RAWDATA	0	0	0	0	0	0	0	0	0	0	0	0	RAWDATA			
2B	0000	GPIOF	GPIOF_ DRIVE	0	0	0	0	0	0	0	0	0	0	0	0	DRIVE			
2C	00FF	GPIOF	GPIOF_IFE	0	0	0	0	0	0	0	0	0	0	0	0	IFE			
2D	0000	GPIOF	GPIOF_ SLEW	0	0	0	0	0	0	0	0	0	0	0	0	SLEW			
2E–3F	—	GPIOF	Reserved	RESERVED															