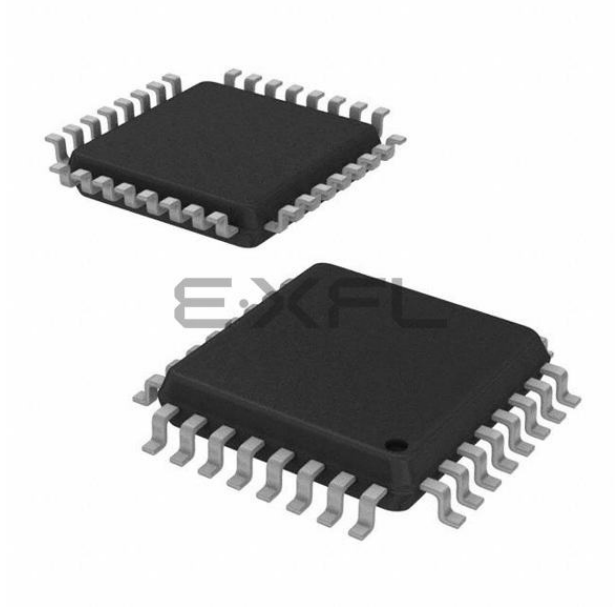

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	56800E
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	27
Program Memory Size	16KB (8K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 16
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 18x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc56f8006vlc

Table of Contents

Table 5. 56F8006/56F8002 Signal and Package Information (continued)

Signal Name	28 SOIC	32 LQFP	32 PSDIP	48 LQFP	Type	State During Reset	Signal Description
GPIOB3	11	16	12	24	Input/ Output	Input, internal pullup enabled	Port B GPIO — This GPIO pin can be individually programmed as an input or output pin.
(MOSI)					Input/ Output		MOSI — Master out/slave in. In master mode, this pin serves as the data output. In slave mode, this pin serves as the data input.
(TIN3)					Input/ Output		TIN3 — Dual timer module channel 3 input.
(ANA3 and ANB3)					Input		ANA3 and ANB3 — Analog input to channel 3 of ADCA and ADCB.
(PWM5)					Output		PWM5 — The PWM channel 5.
(CMP1_ OUT					Output		CMP1_OUT— Analog comparator 1 output. When used as an analog input, the signal goes to the ANA3 and ANB3. After reset, the default state is GPIOB3.
GPIOB4	13	19	15	27	Input/ Output	Input, internal pullup enabled	Port B GPIO — This GPIO pin can be individually programmed as an input or output pin.
(T0)					Input/ Output		T0 — Dual timer module channel 0 input/output.
(CLKO_0)					Output		CLKO_0 — This is a buffered clock output; the clock source is selected by clockout select (CLKOSEL) bits in the clock output select register (CLKOUT) of the SIM.
(MISO)					Input/ Output		MISO — Master in/slave out. In master mode, this pin serves as the data input. In slave mode, this pin serves as the data output. The MISO line of a slave device is placed in the high-impedance state if the slave device is not selected.
(SDA)					Input/Open-drain Output		SDA — The I^2C serial data line.
(RXD)					Input		RXD — The SCI receive data input.
(ANA0 and ANB0)					Analog Input		ANA0 and ANB0 — Analog input to channel 0 of ADCA and ADCB. When used as an analog input, the signal goes to the ANA0 and ANB0. After reset, the default state is GPIOB4.

Table 5. 56F8006/56F8002 Signal and Package Information (continued)

Signal Name	28 SOIC	32 LQFP	32 PSDIP	48 LQFP	Type	State During Reset	Signal Description
TMS (GPIOD3) (ANB11) (T1) (CMP1_OUT)	24	31	27	47	Input Input/ Output Analog Input Input/ Output Output	Input, internal pullup enabled	Test Mode Select Input — This input pin is used to sequence the JTAG TAP controller's state machine. It is sampled on the rising edge of TCK and has an on-chip pullup resistor. Port D GPIO — This GPIO pin can be individually programmed as an input or output pin. ANB11 — Analog input to channel 11 of ADCB. T1 — Dual timer module channel 1 input/output. CMP1_OUT — Analog comparator 2 output. After reset, the default state is TMS. Always tie the TMS pin to VDD through a 2.2 kΩ resistor.
GPIOE0				5	Input/ Output	Input, internal pullup enabled	Port E GPIO — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is GPIOE0.
GPIOE1 (ANB9 and CMP0_P1)				6	Input/ Output Analog Input	Input, internal pullup enabled	Port E GPIO — This GPIO pin can be individually programmed as an input or output pin. ANB9 and CMP0_P1 — Analog input to channel 9 of ADCB and positive input 1 of analog comparator 0. After reset, the default state is GPIOE1.
GPIOE2 (ANB7 and CMP0_M1)				8	Input/ Output Analog Input	Input, internal pullup enabled	Port E GPIO — This GPIO pin can be individually programmed as an input or output pin. ANB7 and CMP0_M1 — Analog input to channel 7 of ADCB and negative input 1 of analog comparator 0. After reset, the default state is GPIOE2.
GPIOE3 (ANA10 and CMP2_M1)				14	Input/ Output Analog Input	Input, internal pullup enabled	Port E GPIO — This GPIO pin can be individually programmed as an input or output pin. ANA10 and CMP2_M1 — Analog input to channel 10 of ADCA and negative input 1 of analog comparator 2. After reset, the default state is GPIOE3.
GPIOE4 (ANA6 and CMP2_P2)				18	Input/ Output Analog Input	Input, internal pullup enabled	Port E GPIO — This GPIO pin can be individually programmed as an input or output pin. ANA6 and CMP2_P2 — Analog input to channel 6 of ADCA and positive input 2 of analog comparator 2. After reset, the default state is GPIOE4.

Table 8. Program Memory Map[1] for 56F8002 at Reset (continued)

Begin/End Address	Memory Allocation
P: 0x1F FFFF P: 0x00 8800	RESERVED
P: 0x00 83FF P: 0x00 8000	On-Chip RAM[2]: 2 KB
P: 0x00 7FFF P: 0x00 2000	RESERVED
P: 0x00 1FFF P: 0x00 0800	• Internal program flash: 12 KB • Interrupt vector table locates from 0x00 0800 to 0x00 0865 • COP reset address = 0x00 0802 • Boot location = 0x00 0800
P: 0x00 07FF P: 0x00 0000	RESERVED

1 All addresses are 16-bit word addresses.

2 This RAM is shared with data space starting at address X: 0x00 0000; see Figure 9.

5.3 Data Map

The 56F8006/56F8002 series contain a dual access memory. It can be accessed from core primary data buses (XAB1; CDBW; CDBR) and secondary data buses (XAB2; XDB2). Addresses in data memory are selected on the XAB1 and XAB2 buses. Byte, word, and long data transfers occur on the 32-bit CDBR and CDBW buses. A second 16-bit read operation can be performed in parallel on the XDB2 bus.

Peripheral registers and on-chip JTAG/EOnCE controller registers are memory-mapped into data memory access. A special direct address mode is supported for accessing a first 64-location in data memory by using a single word instruction.

The data memory map is shown in Table 9.

Table 9. Data Memory Map[1]

Begin/End Address	Memory Allocation
X:0xFF FFFF X:0xFF FF00	EOnCE 256 locations allocated
X:0xFF FEFF X:0x01 0000	RESERVED
X:0x00 FFFF X:0x00 F000	On-Chip Peripherals 4096 locations allocated
X:0x00 EFFF X:0x00 8800	RESERVED
X:0x00 87FF X:0x00 8000	RESERVED
X:0x00 7FFF X:0x00 0400	RESERVED
X:0x00 03FF X:0x00 0000	On-Chip Data RAM 2 KB[2]

1 All addresses are 16-bit word addresses.

2 This RAM is shared with Program space starting at P: 0x00 8000. See Figure 8 and Figure 9.

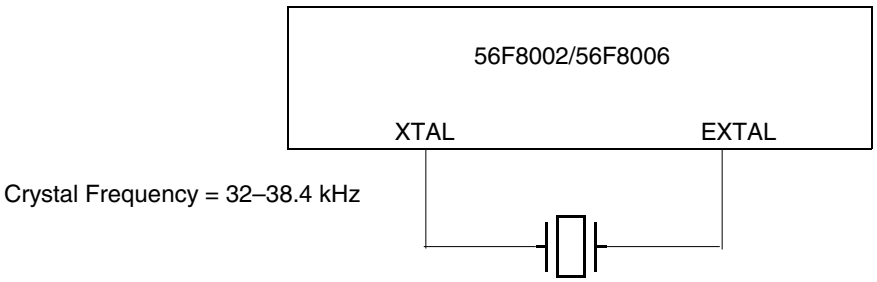

Figure 10. Typical Crystal Oscillator Circuit: Low-Range, Low-Power Mode

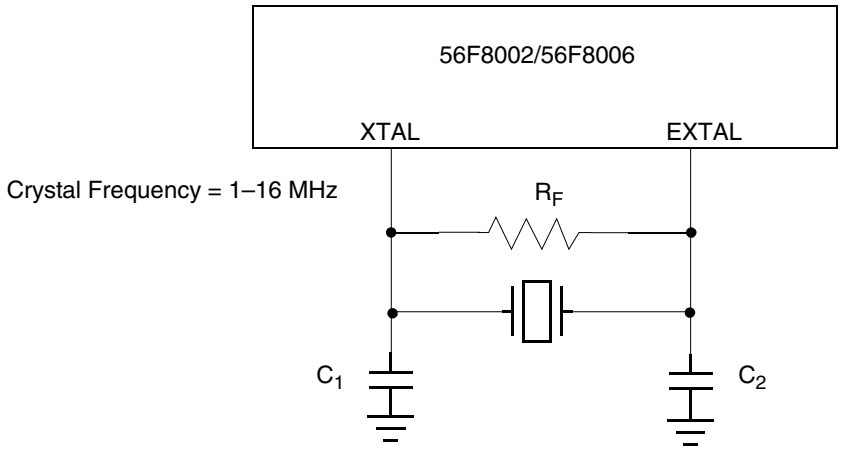

Figure 11. Typical Crystal or Ceramic Resonator Circuit: High-Range, Low-Power Mode

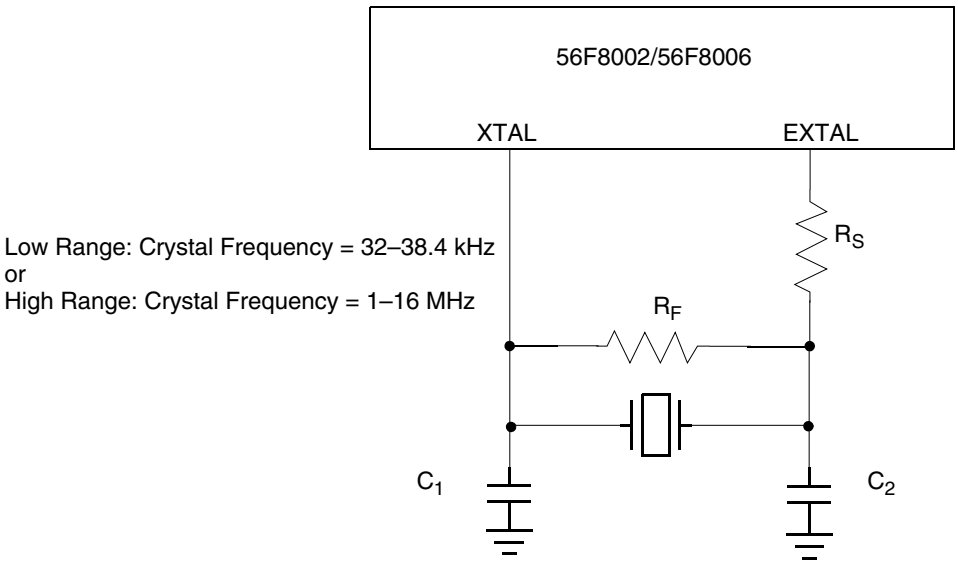

Figure 12. Typical Crystal or Ceramic Resonator Circuit: Low Range and High Range, High-Gain Mode

6.4.3 External Clock Input — Crystal Oscillator Option

The recommended method of connecting an external clock is illustrated in Figure 13. The external clock source is connected to XTAL and the EXTAL pin is grounded or configured as GPIO while CLK_MOD bit in OSCTL register is set. The external clock input must be generated using a relatively low impedance driver with maximum frequency less than 8 MHz.

Each ADC contains a temperature sensor. Outputs of temperature sensors, PGAs, on-chip regulators and VDDA are internally routed to ADC inputs.

- Internal PGA0 output available on ANA15
- Internal PGA0 positive input calibration voltage available on ANA16
- Internal PGA0 negative input calibration voltage available on ANA17
- Internal PGA1 output available on ANB15
- Internal PGA1 positive input calibration voltage available on ANB16
- Internal PGA1 negative input calibration voltage available on ANB17
- ADCA temperature sensor available on ANA26
- ADCB temperature sensor available on ANB26
- Output of on-chip digital voltage regulator is routed to ANA24
- Output of on-chip analog voltage regulator is routed to ANA25
- Output of on-chip small voltage regulator for ROSC is routed to ANB24
- Output of on-chip small voltage regulator for PLL is routed to ANB25
- VDDA is routed to ANA27 and ANB27

6.8 Joint Test Action Group (JTAG)/Enhanced On-Chip Emulator (EOnCE)

The DSP56800E Family includes extensive integrated support for application software development and real-time debugging. Two modules, the Enhanced On-Chip Emulation module (EOnCE) and the core test access port (TAP, commonly called the JTAG port), work together to provide these capabilities. Both are accessed through a common 4-pin JTAG/EOnCE interface. These modules allow you to insert the 56F8006/56F8002 into a target system while retaining debug control. This capability is especially important for devices without an external bus, because it eliminates the need for a costly cable to bring out the footprint of the chip, as is required by a traditional emulator system.

The DSP56800E EOnCE module is a Freescale-designed module used to develop and debug application software used with the chip. This module allows non-intrusive interaction with the CPU and is accessible through the pins of the JTAG interface or by software program control of the DSP56800E core. Among the many features of the EOnCE module is the support for data communication between the controller and the host software development and debug systems in real-time program execution. Other features allow for hardware breakpoints, the monitoring and tracking of program execution, and the ability to examine and modify the contents of registers, memory, and on-chip peripherals, all in a special debug environment. No user-accessible resources need to be sacrificed to perform debugging operations.

The DSP56800E JTAG port is used to provide an interface for the EOnCE module to the DSP JTAG pins. Joint Test Action Group (JTAG) boundary scan is an IEEE 1149.1 standard methodology enabling access to test features using a test access port (TAP). A JTAG boundary scan consists of a TAP controller and boundary scan registers. Please contact your Freescale sales representative or authorized distributor for device-specific BSDL information.

NOTE

In normal operation, an external pullup on the TMS pin is highly recommend to place the JTAG state machine in reset state if this pin is not configured as GPIO.

7 Security Features

The 56F8006/56F8002 offers security features intended to prevent unauthorized users from reading the contents of the flash memory (FM) array. The 56F8006/56F8002's flash security consists of several hardware interlocks that prevent unauthorized users from gaining access to the flash array.

After flash security is set, an authorized user can be enabled to access on-chip memory if a user-defined software subroutine, which reads and transfers the contents of internal memory via peripherals, is included in the application software. This

application software could communicate over a serial port, for example, to validate the authenticity of the requested access, then grant it until the next device reset. The inclusion of such a back door technique is at the discretion of the system designer.

7.1 Operation with Security Enabled

After you have programmed flash with the application code, or as part of the programming of the flash with the application code, the 56F8006/56F8002 can be secured by programming the security word, 0x0002, into program memory location 0x00 1FF7. This can also be effected by use of the CodeWarrior IDE menu flash lock command. This nonvolatile word keeps the device secured after reset, caused, for example, by a power-down of the device. Refer to the flash memory chapter in the *MC56F8006 Peripheral Reference Manual* for detail. When flash security mode is enabled, the 56F8006/56F8002 disables the core EOnCE debug capabilities. Normal program execution is otherwise unaffected.

7.2 Flash Access Lock and Unlock Mechanisms

There are several methods that effectively lock or unlock the on-chip flash.

7.2.1 Disabling EOnCE Access

On-chip flash can be read by issuing commands across the EOnCE port, which is the debug interface for the 56800E CPU. The TCK, TMS, TDO, and TDI pins comprise a JTAG interface onto which the EOnCE port functionality is mapped. When the device boots, the chip-level JTAG TAP (test access port) is active and provides the chip's boundary scan capability and access to the ID register, but proper implementation of flash security blocks any attempt to access the internal flash memory via the EOnCE port when security is enabled. This protection is effective when the device comes out of reset, even prior to the execution of any code at startup.

7.2.2 Flash Lockout Recovery Using JTAG

If the device is secured, one lockout recovery mechanism is the complete erasure of the internal flash contents, including the configuration field, thus disabling security (the protection register is cleared). This does not compromise security, as the entire contents of your secured code stored in flash are erased before security is disabled on the device on the next reset or power-up sequence.

To start the lockout recovery sequence via JTAG, the JTAG public instruction (LOCKOUT_RECOVERY) must first be shifted into the chip-level TAP controller's instruction register. After the LOCKOUT_RECOVERY instruction has been shifted into the instruction register, the clock divider value must be shifted into the corresponding 7-bit data register. After the data register has been updated, you must transition the TAP controller into the RUN-TEST/IDLE state for the lockout sequence to commence. The controller must remain in this state until the erase sequence is complete. Refer to the *MC56F8006 Peripheral Reference Manual* for detail, or contact Freescale.

NOTE

After the lockout recovery sequence has completed, you must reset the JTAG-TAP controller and device to return to normal unsecured operation. Power-on reset resets both too.

7.2.3 Flash Lockout Recovery Using CodeWarrior

CodeWarrior can unlock a device by selecting the *Debug* menu, then selecting *DSP56800E*, followed by *Unlock Flash*. Another mechanism is also built into CodeWarrior using the device's memory configuration file. The command "*Unlock_Flash_on_Connect 1*" in the *.cfg* file accomplishes the same task as using the *Debug* menu.

This lockout recovery mechanism is the complete erasure of the internal flash contents, including the configuration field, thus disabling security (the protection register is cleared).

Table 15. 28SOIC Package Thermal Characteristics (continued)

Characteristic	Comments	Symbol	Value (LQFP)	Unit
Junction to ambient (@200 ft/min)	Four layer board (2s2p)	$R_{\theta JMA}$	42	°C/W
Junction to board		$R_{\theta JB}$	23	°C/W
Junction to case		$R_{\theta JC}$	26	°C/W
Junction to package top	Natural Convection	Ψ_{JT}	9	°C/W

Table 16. 32LQFP Package Thermal Characteristics

Characteristic	Comments	Symbol	Value (LQFP)	Unit
Junction to ambient Natural convection	Single layer board (1s)	$R_{\theta JA}$	84	°C/W
Junction to ambient Natural convection	Four layer board (2s2p)	$R_{\theta JMA}$	56	°C/W
Junction to ambient (@200 ft/min)	Single layer board (1s)	$R_{\theta JMA}$	70	°C/W
Junction to ambient (@200 ft/min)	Four layer board (2s2p)	$R_{\theta JMA}$	49	°C/W
Junction to board		$R_{\theta JB}$	33	°C/W
Junction to case		$R_{\theta JC}$	20	°C/W
Junction to package top	Natural convection	Ψ_{JT}	4	°C/W

Table 17. 32PSDIP Package Thermal Characteristics

Characteristic	Comments	Symbol	Value (LQFP)	Unit
Junction to ambient Natural convection	Single layer board (1s)	$R_{\theta JA}$	56	°C/W
Junction to ambient Natural convection	Four layer board (2s2p)	$R_{\theta JMA}$	41	°C/W
Junction to ambient (@200 ft/min)	Single layer board (1s)	$R_{\theta JMA}$	45	°C/W
Junction to ambient (@200 ft/min)	Four layer board (2s2p)	$R_{\theta JMA}$	36	°C/W
Junction to board		$R_{\theta JB}$	18	°C/W
Junction to case		$R_{\theta JC}$	24	°C/W
Junction to package top	Natural convection	Ψ_{JT}	10	°C/W

Table 19. Recommended Operating Conditions
($V_{REFL\ x}$= 0 V, V_{SSA} = 0 V, V_{SS} = 0 V)

Characteristic	Symbol	Notes	Min	Typ	Max	Unit
Supply voltage	V_{DD}, V_{DDA}		3	3.3	3.6	V
Voltage difference V_{DD} to V_{DDA}	ΔV_{DD}		–0.1	0	0.1	V
Voltage difference V_{SS} to V_{SSA}	ΔV_{SS}		–0.1	0	0.1	V
Device Clock Frequency Using relaxation oscillator Using external clock source	FSYSCLK		 1 0		 32 32	MHz
Input Voltage High (digital inputs)	V_{IH}	Pin Groups 1, 2	2.0		V_{DD}	V
Input Voltage Low (digital inputs)	V_{IL}	Pin Groups 1, 2	–0.3		0.8	V
Oscillator Input Voltage High XTAL driven by an external clock source	V_{IHOSC}	Pin Group 4	2.0		V_{DDA} + 0.3	V
Oscillator Input Voltage Low	V_{ILOSC}	Pin Group 4	–0.3		0.8	V
Output Source Current High at V_{OH} min.)[1] When programmed for low drive strength When programmed for high drive strength	I_{OH}	 Pin Group 1 Pin Group 1	 — —		 –4 –8	mA
Output Source Current Low (at V_{OL} max.)[1] When programmed for low drive strength When programmed for high drive strength	I_{OL}	 Pin Groups 1, 2 Pin Groups 1, 2	 — —		 4 8	mA
Ambient Operating Temperature (Extended Industrial)	T_A		–40		105	°C
Flash Endurance (Program Erase Cycles)	N_F	T_A = –40°C to 125°C	10,000		—	cycles
Flash Data Retention	t_R	$T_J \leq$ 85°C avg	15		—	years
Flash Data Retention with <100 Program/Erase Cycles	t_{FLRET}	$T_J \leq$ 85°C avg	20	—	—	years

1 Total chip source or sink current cannot exceed 75 mA.

Table 20. Default Mode

Pin Group 1	GPIO, TDI, TDO, TMS, TCK
Pin Group 2	SCL, SDA
Pin Group 3	ADC and Comparator Analog Inputs and PGA Inputs
Pin Group 4	XTAL, EXTAL

8.5 DC Electrical Characteristics

This section includes information about power supply requirements and I/O pin characteristics.

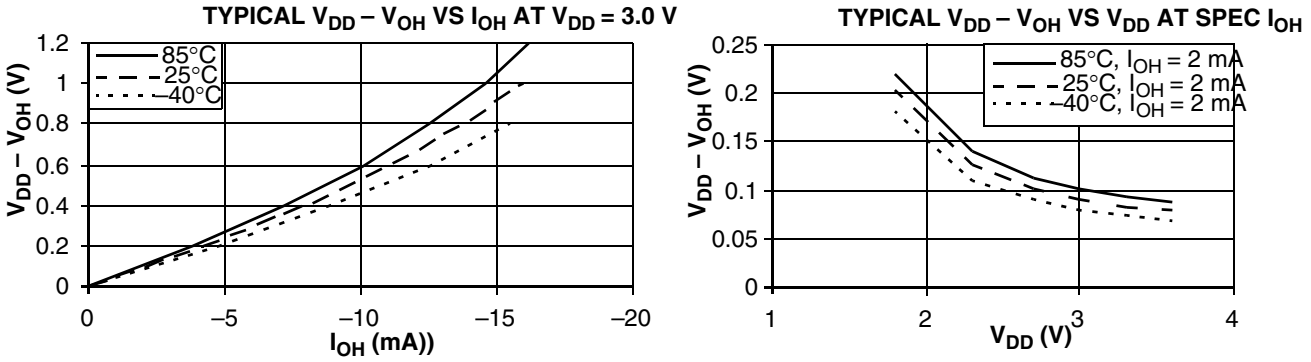

Figure 19. Typical High-Side (Source) Characteristics — Low Drive (GPIO_x_DRIVEn = 0)

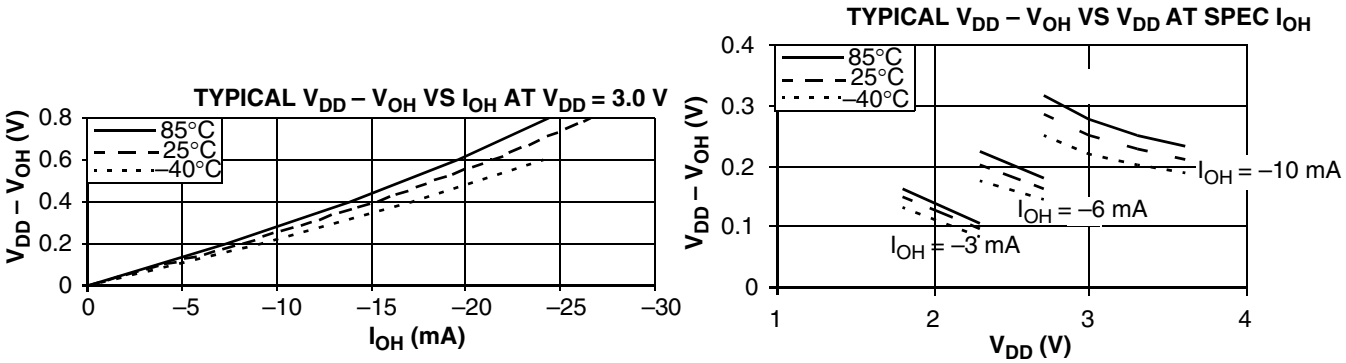

Figure 20. Typical High-Side (Source) Characteristics — High Drive (GPIO_x_DRIVEn = 1)

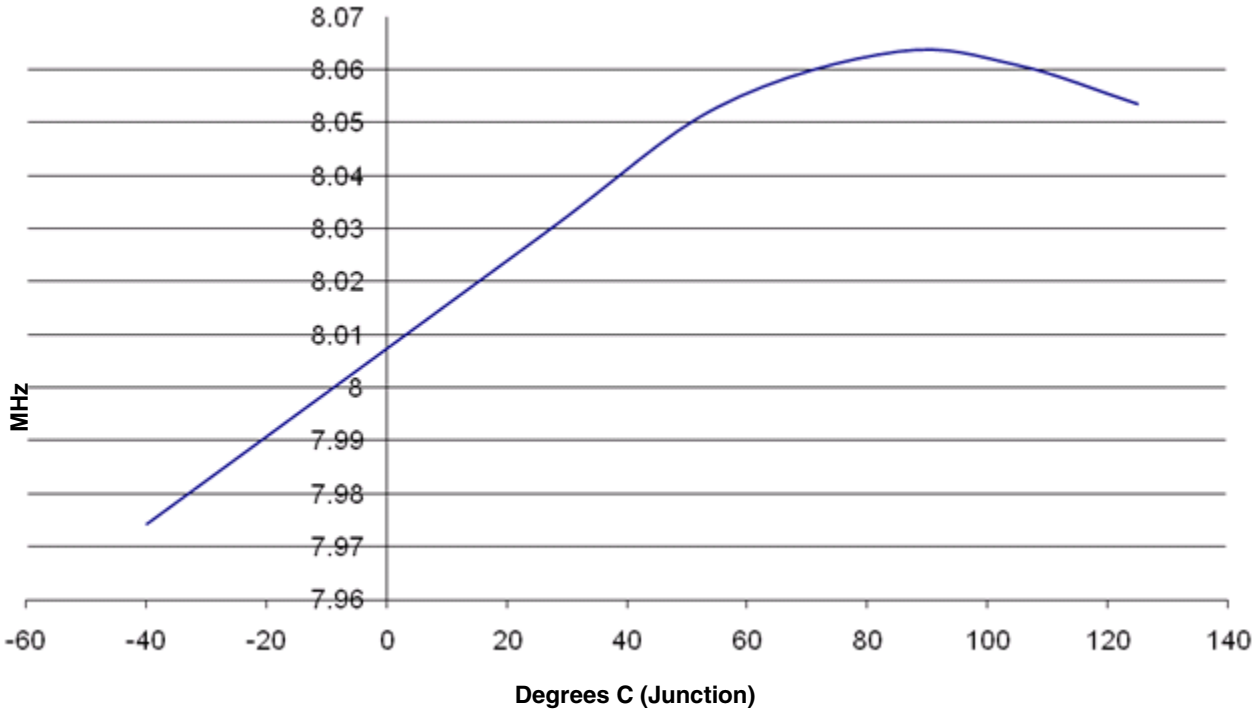

Figure 22. Relaxation Oscillator Temperature Variation (Typical) After Trim for devices with temperature operating range from –40 °C to 105 °C

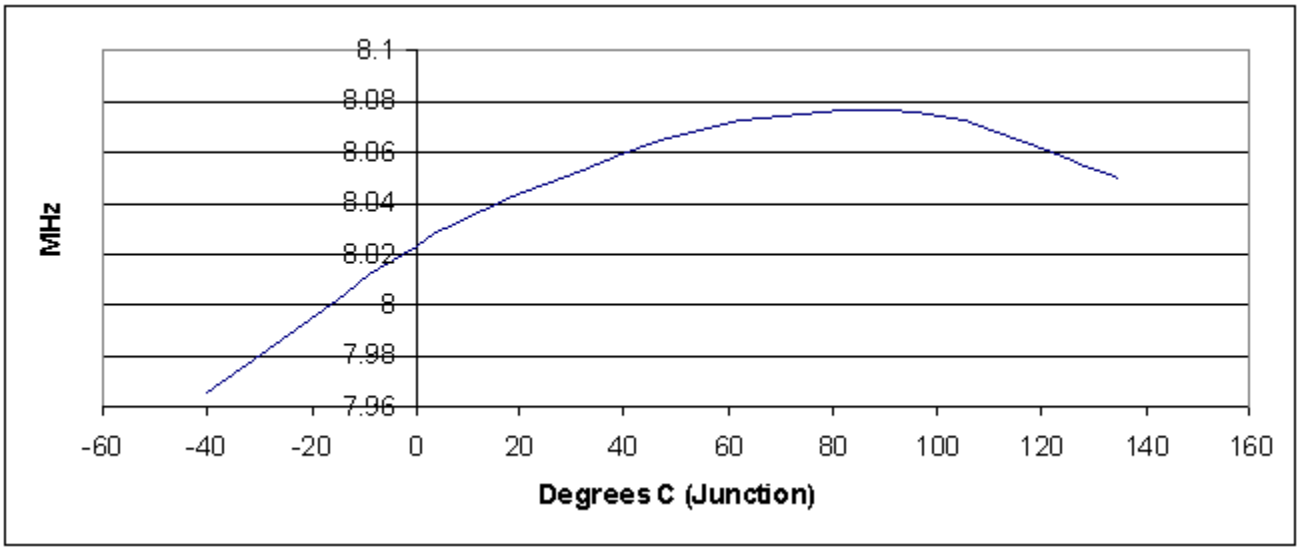

Figure 23. Relaxation Oscillator Temperature Variation (Typical) After Trim for devices with temperature operating range from –40 °C to 125 °C

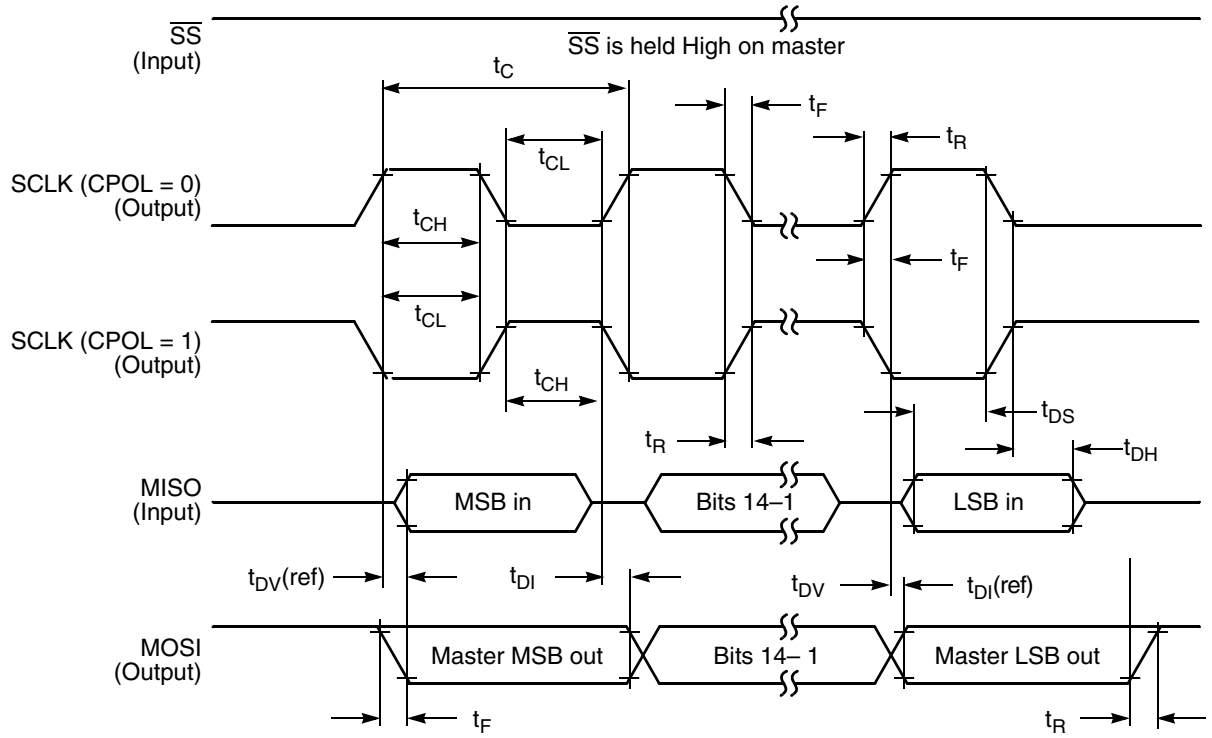

Figure 28. SPI Master Timing (CPHA = 1)

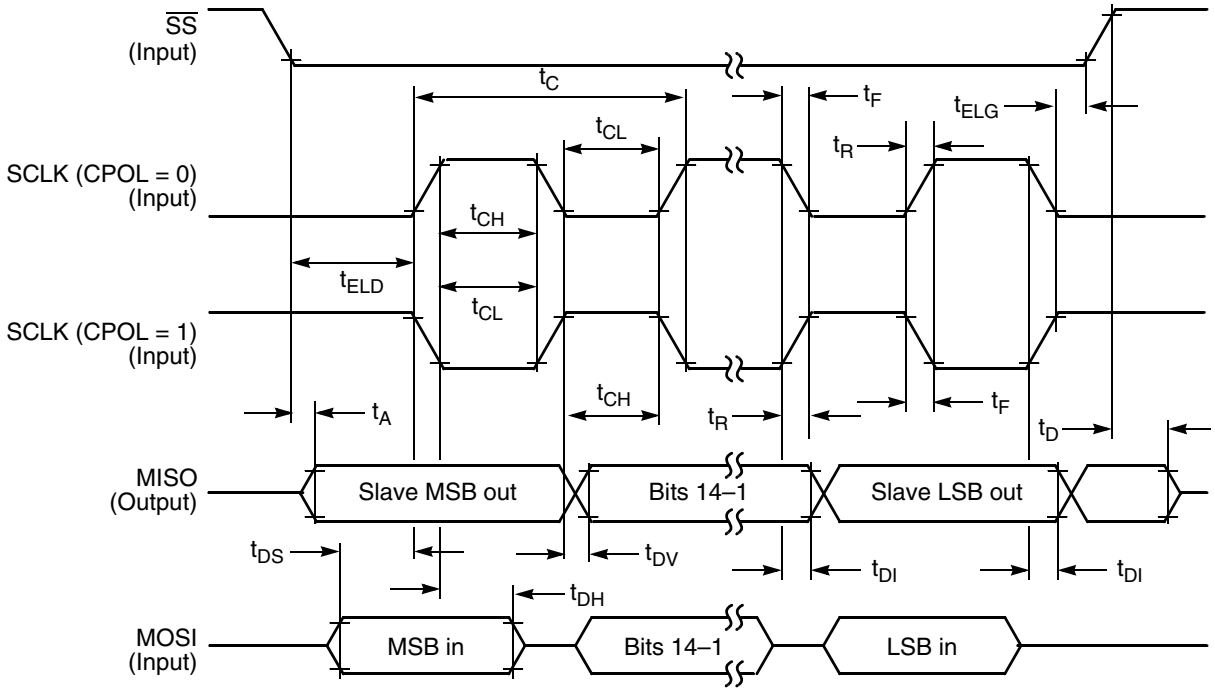

Figure 29. SPI Slave Timing (CPHA = 0)

1 Typical values assume V_{DDA} = 3.0 V, Temp = 25°C, f_{ADCK}=1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
2 1 LSB = $(V_{REFH} - V_{REFL})/2^N$
3 Monotonicity and no-missing-codes guaranteed in 10-bit and 8-bit modes
4 Based on input pad leakage current. Refer to pad electricals.

8.17 HSCMP Specifications

Table 38. HSCMP Specifications

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{PWR}	1.8		3.6	V
Supply current, high speed mode (EN=1, PMODE=1, $V_{DDA} \geq V_{LVI\_trip}$)	I_{DDAHS}		150		μA
Supply current, low speed mode (EN=1, PMODE=0)	I_{DDALS}		10		μA
Supply current, off mode (EN=0,)	I_{DDAOFF}			100	nA
Analog input voltage	V_{AIN}	V_{SSA} – 0.01		V_{DDA} + 0.01	V
Analog input offset voltage	V_{AIO}			40	mV
Analog comparator hysteresis	V_H	3.0		20.0	mV
Propagation Delay, high speed mode (EN=1, PMODE=1), 2.4 V < V_{DDA} < 3.6 V	t_{DHSN}[1]		70	140	ns
Propagation Delay, High Speed Mode (EN=1, PMODE=1), 1.8 V < V_{DDA} < 2.4 V	t_{DHSB}[2]		70	249	ns
Propagation Delay, Low Speed Mode (EN=1, PMODE=0), 2.4 V < V_{DDA} < 3.6 V	t_{AINIT}[3]		400	600	ns
Propagation Delay, Low Speed Mode (EN=1, PMODE=0), 1.8 V < V_{DDA} < 2.4 V	t_{AINIT}[4]		400	600	ns

1 Measured with an input waveform that switches 30 mV above and below the reference, to the CMPO output pin. V_{DDA} > $V_{LVI\_WARNING}$ => LVI_WARNING NOT ASSERTED.
2 Measured with an input waveform that switches 30mV above and below the reference, to the CMPO output pin. V_{DDA} < $V_{LVI\_WARNING}$ => LVI_WARNING ASSERTED.
3 Measured with an input waveform that switches 30mV above and below the reference, to the CMPO output pin. V_{DDA} > $V_{LVI\_WARNING}$ => LVI_WARNING NOT ASSERTED.
4 Measured with an input waveform that switches 30mV above and below the reference, to the CMPO output pin. V_{DDA} < $V_{LVI\_WARNING}$ => LVI_WARNING ASSERTED.

8.18 Optimize Power Consumption

See Section 8.6, "Supply Current Characteristics," for a list of I_{DD} requirements for the 56F8006/56F8002. This section provides additional detail that can be used to optimize power consumption for a given application.

Power consumption is given by the following equation:

Eqn. 1

$$\begin{aligned}\text{Total power} = \quad & \text{A: internal [static component]} \\ & +\text{B: internal [state-dependent component]} \\ & +\text{C: internal [dynamic component]} \\ & +\text{D: external [dynamic component]} \\ & +\text{E: external [static component]}\end{aligned}$$

A, the internal [static] component, is comprised of the DC bias currents for the oscillator, leakage currents, PLL, and voltage references. These sources operate independently of processor state or operating frequency.

B, the internal [state-dependent] component, reflects the supply current required by certain on-chip resources only when those resources are in use. These include RAM, flash memory, and the ADCs.

C, the internal [dynamic] component, is classic $C*V^2*F$ CMOS power dissipation corresponding to the 56800E core and standard cell logic.

D, the external [dynamic] component, reflects power dissipated on-chip as a result of capacitive loading on the external pins of the chip. This is also commonly described as $C*V^2*F$, although simulations on two of the I/O cell types used on the 56800E reveal that the power-versus-load curve does have a non-zero Y-intercept.

Table 39. I/O Loading Coefficients at 10 MHz

	Intercept	Slope
8 mA drive	1.3	0.11 mW/pF
4 mA drive	1.15 mW	0.11 mW/pF

Power due to capacitive loading on output pins is (first order) a function of the capacitive load and frequency at which the outputs change. Table 39 provides coefficients for calculating power dissipated in the I/O cells as a function of capacitive load. In these cases:

$$\textit{TotalPower} = \Sigma((\text{Intercept} + \text{Slope}*\text{Cload})*\text{frequency}/10\ \text{MHz}) \qquad \textit{Eqn. 2}$$

where:

- Summation is performed over all output pins with capacitive loads
- Total power is expressed in mW
- C_{load} is expressed in pF

Because of the low duty cycle on most device pins, power dissipation due to capacitive loads was found to be fairly low when averaged over a period of time.

E, the external [static component], reflects the effects of placing resistive loads on the outputs of the device. Sum the total of all V^2/R or IV to arrive at the resistive load contribution to power. Assume V = 0.5 for the purposes of these rough calculations. For instance, if there is a total of eight PWM outputs driving 10 mA into LEDs, then P = 8*0.5*0.01 = 40 mW.

In previous discussions, power consumption due to parasitics associated with pure input pins is ignored, as it is assumed to be negligible.

10 Package Mechanical Outline Drawings

10.1 28-pin SOIC Package

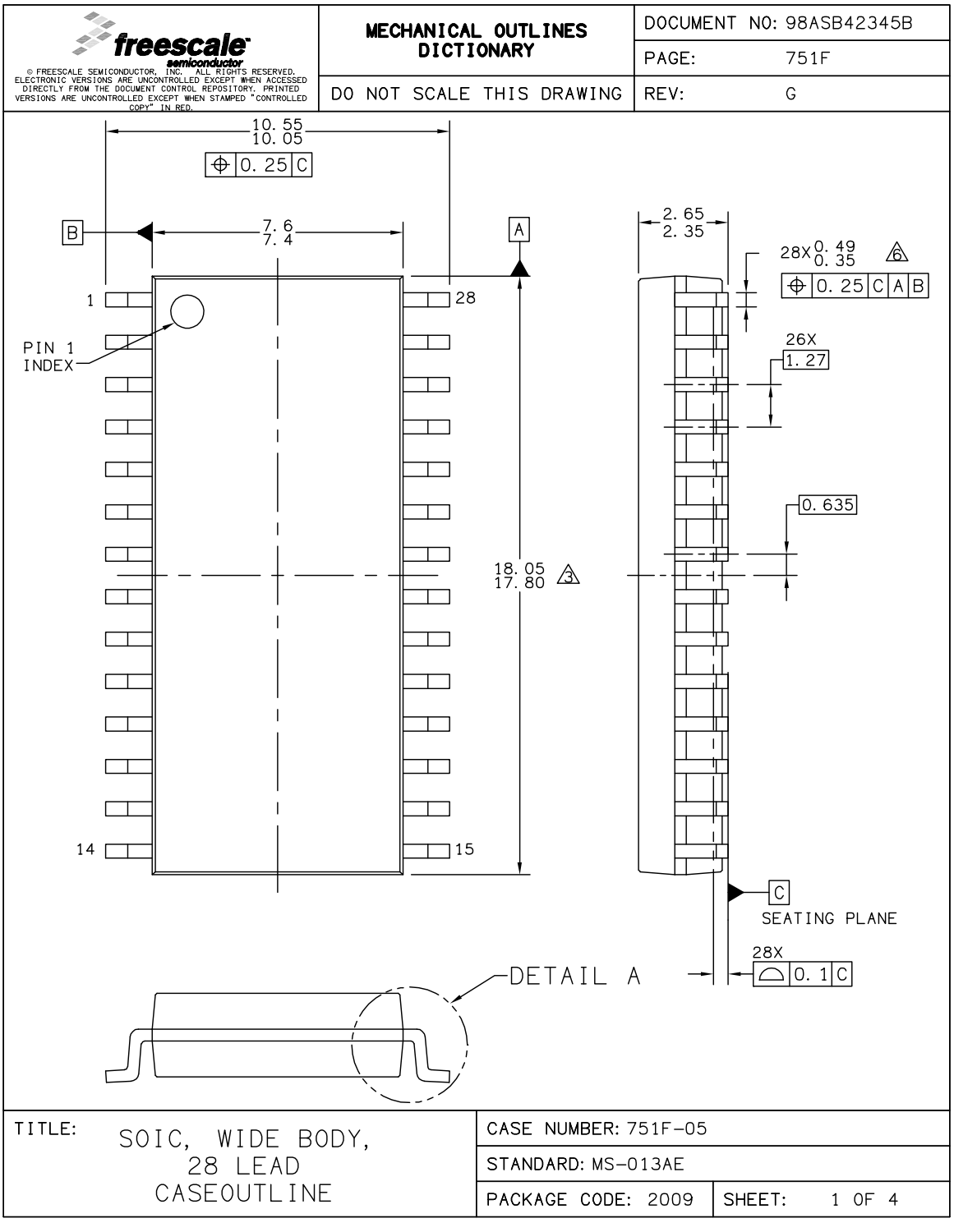

Table 44. Detailed Peripheral Memory Map (continued)

Offset Addr. (Hex)	Reset Value (Hex)	Periph.	Register	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Bit 0
0A	0000	TMR0	TMR0_ CSCTRL	DBG_EN		FAULT	ALT_LOAD	0	0	0	0	TCF2EN	TCF1EN	TCF2	TCF1	CL2		CL1	
0B	0000	TMR0	TMR0_ FILT	0	0	0	0	0	FILT_CNT			FILT_PER							
0C–0E	—	TMR0	Reserved	RESERVED															
0F	000F	TMR0	TMR_ ENBL	0	0	0	0	0	0	0	0	0	0	0	0	ENBL			
10	0000	TMR1	TMR1_ COMP1	COMPARISON_1															
11	0000	TMR1	TMR1_ COMP2	COMPARISON_2															
12	0000	TMR1	TMR1_ CAPT	CAPTURE															
13	0000	TMR1	TMR1_ LOAD	LOAD															
14	0000	TMR1	TMR1_ HOLD	HOLD															
15	0000	TMR1	TMR1_ CNTR	COUNTER															
16	0000	TMR1	TMR1_ CTRL	CM			PCS				SCS		ONCE	LENGTH	DIR	COINIT	OM		
17	0000	TMR1	TMR1_ SCTRL	TCF	TCFIE	TOF	TOFIE	IEF	IEFIE	IPS	INPUT	CAPTURE_ MODE		MSTR	EEOF	VAL	FORCE	OPS	OEN
18	0000	TMR1	TMR1_ CMPLD1	COMPARATOR_LOAD_1															
19	0000	TMR1	TMR1_ CMPLD2	COMPARATOR_LOAD_2															

Table 44. Detailed Peripheral Memory Map (continued)

Offset Addr. (Hex)	Reset Value (Hex)	Periph.	Register	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Bit 0
C3	0000	PGA1	PGA1_STS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	RUNNING	STCOMP
C4–DF	—	PGA1	Reserved	RESERVED															
E0	0200	SCI	SCI_RATE	SBR													FRAC_SBR		
E1	0000	SCI	SCI_CTRL1	LOOP	SWAI	RSRC	M	WAKE	POL	PE	PT	TEIE	TIIE	RFIE	REIE	TE	RE	RWU	SBK
E2	0000	SCI	SCI_CTRL2	0	0	0	0	0	0	0	0	0	0	0	0	LIN_MODE	0	0	0
E3	C000	SCI	SCI_STAT	TDRE	TIDLE	RDRF	RIDLE	OR	NF	FE	PF	0	0	0	0	LSE	0	0	RAF
E4	0000	SCI	SCI_DATA	0	0	0	0	0	0	0	RECEIVE_TRANSMIT_DATA								
E5–FF	—	SCI	Reserved	RESERVED															
00	6141	SPI	SPI_SCTRL	SPR			DSO	ERRIE	MODFEN	SPRIE	SPMSTR	CPOL	CPHA	SPE	SPTIE	SPRF	OVRF	MODF	SPTE
01	000F	SPI	SPI_DSCTRL	WOM	0	0	BD2X	SSB_IN	SSB_DATA	SSB_ODM	SSB_AUTO	SSB_DDR	SSB_STRB	SSB_OVER	SPR3	DS			
02	0000	SPI	SPI_DRCV	R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0
03	0000	SPI	SPI_DXMIT	T15	T14	T13	T12	T11	T10	T9	T8	T7	T6	T5	T4	T3	T2	T1	T0
04–1F	—	SPI	Reserved	RESERVED															
20	0000	I2C	I2C_ADDR	0	0	0	0	0	0	0	0	AD7	AD6	AD5	AD4	AD3	AD2	AD1	0
21	0000	I2C	I2C_FREQDIV	0	0	0	0	0	0	0	0	MULT		ICR					

Table 44. Detailed Peripheral Memory Map (continued)

Offset Addr. (Hex)	Reset Value (Hex)	Periph.	Register	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Bit 0
85	0000	GPIOA	GPIOA_ IENR	0	0	0	0	0	0	0	0	IEN							
86	0000	GPIOA	GPIOA_ IPOLR	0	0	0	0	0	0	0	0	IPOL							
87	0000	GPIOA	GPIOA_ IPR	0	0	0	0	0	0	0	0	IP							
88	0000	GPIOA	GPIOA_ IESR	0	0	0	0	0	0	0	0	IES							
89	—	GPIOA	Reserved	RESERVED															
8A	0000	GPIOA	GPIOA_ RAWDATA	0	0	0	0	0	0	0	0	RAWDATA							
8B	0000	GPIOA	GPIOA_ DRIVE	0	0	0	0	0	0	0	0	DRIVE							
8C	00FF	GPIOA	GPIOA_IFE	0	0	0	0	0	0	0	0	IFE							
8D	0000	GPIOA	GPIOA_ SLEW	0	0	0	0	0	0	0	0	SLEW							
8E–9F	—	GPIOA	Reserved	RESERVED															
A0	00FF	GPIOB	GPIOB_ PUR	0	0	0	0	0	0	0	0	PUR							
A1	0000	GPIOB	GPIOB_DR	0	0	0	0	0	0	0	0	DR							
A2	0000	GPIOB	GPIOB_ DDR	0	0	0	0	0	0	0	0	DDR							
A3	0080	GPIOB	GPIOB_ PER	0	0	0	0	0	0	0	0	PER							
A4	—	GPIOB	Reserved	RESERVED															
A5	0000	GPIOB	GPIOB_ IENR	0	0	0	0	0	0	0	0	IENR							
A6	0000	GPIOB	GPIOB_ IPOLR	0	0	0	0	0	0	0	0	IPOLR							

Table 44. Detailed Peripheral Memory Map (continued)

Offset Addr. (Hex)	Reset Value (Hex)	Periph.	Register	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Bit 0
40	0000	SIM	SIM_CTRL	0	0	0	0	0	0	0	0	0	0	ONCEEBL	SW RST	STOP_ DISABLE		WAIT_ DISABLE	
41	0001	SIM	SIM_ RSTAT	0	0	0	0	0	0	0	0	0	SWR	COP_CPU	COP_LOR	EXTR	LVDR	PPD	POR
42	01F2	SIM	SIM_ MSHID	SIM_MSH_ID															
43	601D	SIM	SIM_ LSHID	SIM_LSH_ID															
45	2020	SIM	SIM_ CLKOUT	0	0	CLKDIS1	0	0	CLKOSEL1			0	0	CLKDIS0	CLKOSEL0				
46	0000	SIM	SIM_PCR	TMR_CR	0	PWM_CR	SCI_CR	0	0	0	0	0	0	0	0	0	0	0	0
47	0000	SIM	SIM_PCE	CMP2	CMP1	CMP0	ADC1	ADC0	PGA1	PGA0	I2C	SCI	SPI	PWM	COP	PDB	PIT	TA1	TA0
48	0000	SIM	SIM_SDR	CMP2	CMP1	CMP0	ADC1	ADC0	PGA1	PGA0	I2C	SCI	SPI	PWM	COP	PDB	PIT	TA1	TA0
49	F000	SIM	SIM_ISAL	ADDR_15_6										0	0	0	0	0	0
4A	0000	SIM	SIM_PROT	0	0	0	0	0	0	0	0	0	0	0	0	PCEP		GIPSP	
4B	0000	SIM	SIM_GPSA	0	0	0	0	0	0	0	GPS_A6			GPS_A5		GPS_A4		GPS_A3	
4C	0000	SIM	SIM_ GPSB0	GPS_B5		GPS_B4			GPS_B3			GPS_B2		0	GPS_B1		GPS_B0		
4D	0000	SIM	SIM_ GPSB1	0	0	0	0	0	0	0	0	0	0	0	0	GPS_B7		GPS_B6	

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