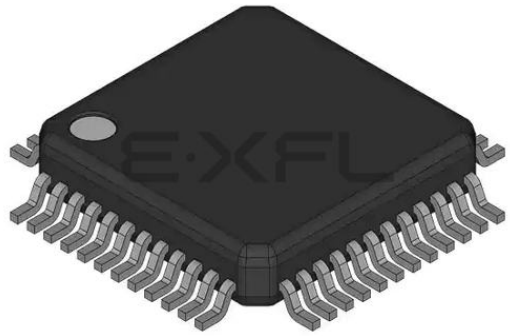

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RAM Size	-
Voltage - Supply (Vcc/Vdd)	-
Data Converters	-
Oscillator Type	-
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Mounting Type	-
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Supplier Device Package	-
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1 MC56F8006/MC56F8002 Family Configuration

MC56F8006/MC56F8002 device comparison in Table 1.

Table 1. MC56F8006 Series Device Comparison

Feature	MC56F8006			MC56F8002
	28-pin	32-pin	48-pin	28-pin
Flash memory size (Kbytes)	16			12
RAM size (Kbytes)	2			
Analog comparators (ACMP)	3			
Analog-to-digital converters (ADC)	2			
Unshielded ADC inputs	6	7	7	6
Shielded ADC inputs	9	11	17	9
Total number of ADC input pins[1]	15	18	24	15
Programmable gain amplifiers (PGA)	2			
Pulse-width modulator (PWM) outputs	6			
PWM fault inputs	3	4	4	3
Inter-integrated circuit (IIC)	1			
Serial peripheral interface (SPI)	1			
High speed serial communications interface (SCI)	1			
Programmable interrupt timer (PIT)	1			
Programmable delay block (PDB)	1			
16-bit multi-purpose timers (TMR)	2			
Real-time counter (RTC)	1			
Computer operating properly (COP) timer	Yes			
Phase-locked loop (PLL)	Yes			
1 kHz on-chip oscillator	Yes			
8 MHz (400 kHz at standby mode) on-chip ROSC	Yes			
Crystal oscillator	Yes			
Power management controller (PMC)	Yes			
IEEE 1149.1 Joint Test Action Group (JTAG) interface	Yes			
Enhanced on-chip emulator (EOnCE) IEEE 1149.1 Joint Test Action Group (JTAG) interface	Yes			

[1] Some ADC inputs share the same pin. See Table 4.

2 Block Diagram

Figure 1 shows a top-level block diagram of the MC56F8006/MC56F8002 digital signal controller. Package options for this family are described later in this document. Italics indicate a 56F8002 device parameter.

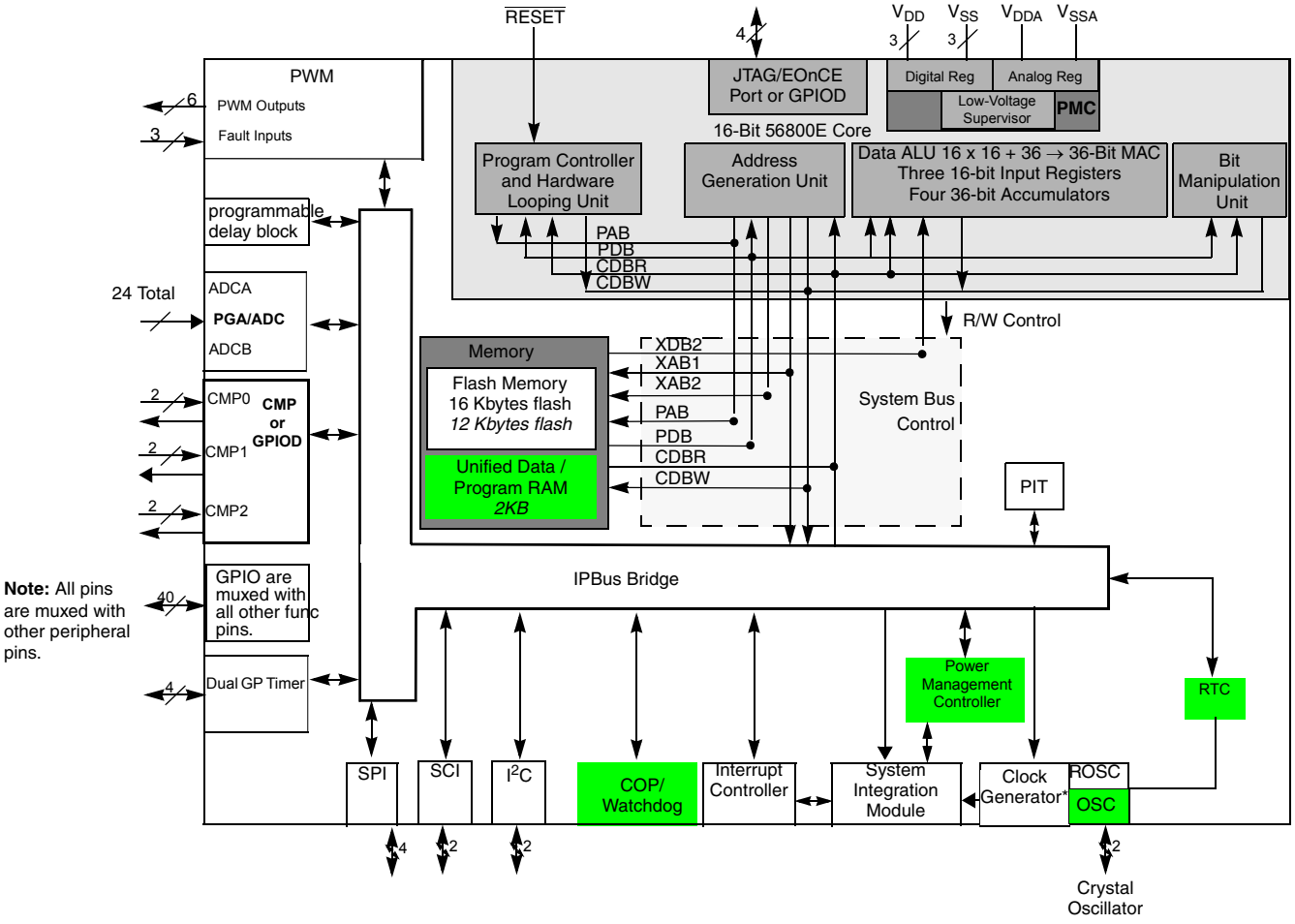


Figure 1. MC56F8006/MC56F8002 Block Diagram

3 Overview

3.1 56F8006/56F8002 Features

3.1.1 Core

- Efficient 16-bit 56800E family digital signal controller (DSC) engine with dual Harvard architecture
- As many as 32 million instructions per second (MIPS) at 32 MHz core frequency
- 155 basic instructions in conjunction with up to 20 address modes
- Single-cycle 16 × 16-bit parallel multiplier-accumulator (MAC)
- Four 36-bit accumulators, including extension bits
- 32-bit arithmetic and logic multi-bit shifter

3.3 Architecture Block Diagram

The 56F8006/56F8002's architecture is shown in Figure 2 and Figure 3. Figure 2 illustrates how the 56800E system buses communicate with internal memories and the IPBus interface and the internal connections among each unit of the 56800E core. Figure 3 shows the peripherals and control blocks connected to the IPBus bridge. Please see the system integration module (SIM) section in the *MC56F8006 Reference Manual* for information about which signals are multiplexed with those of other peripherals.

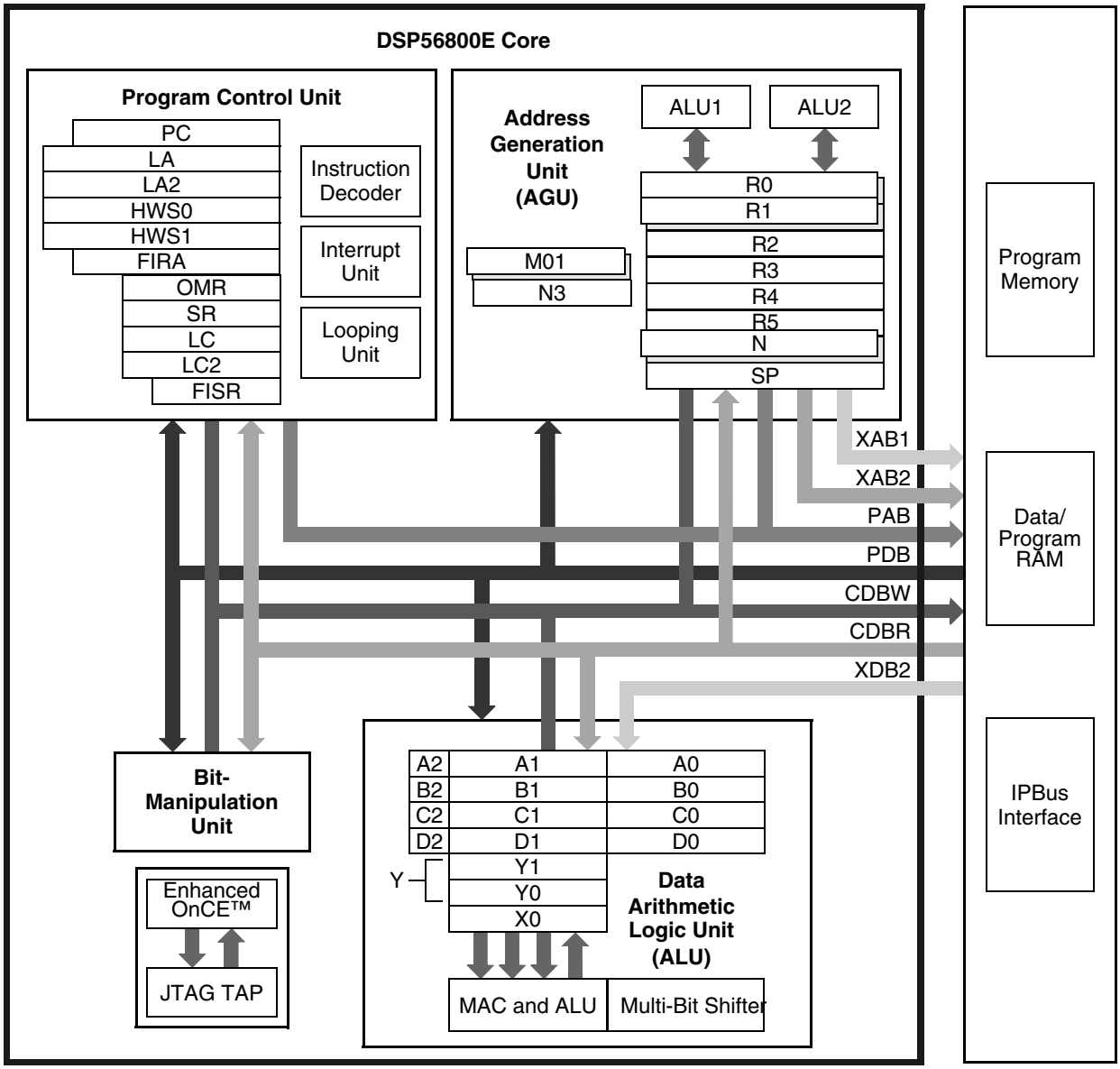


Figure 2. 56800E Core Block Diagram

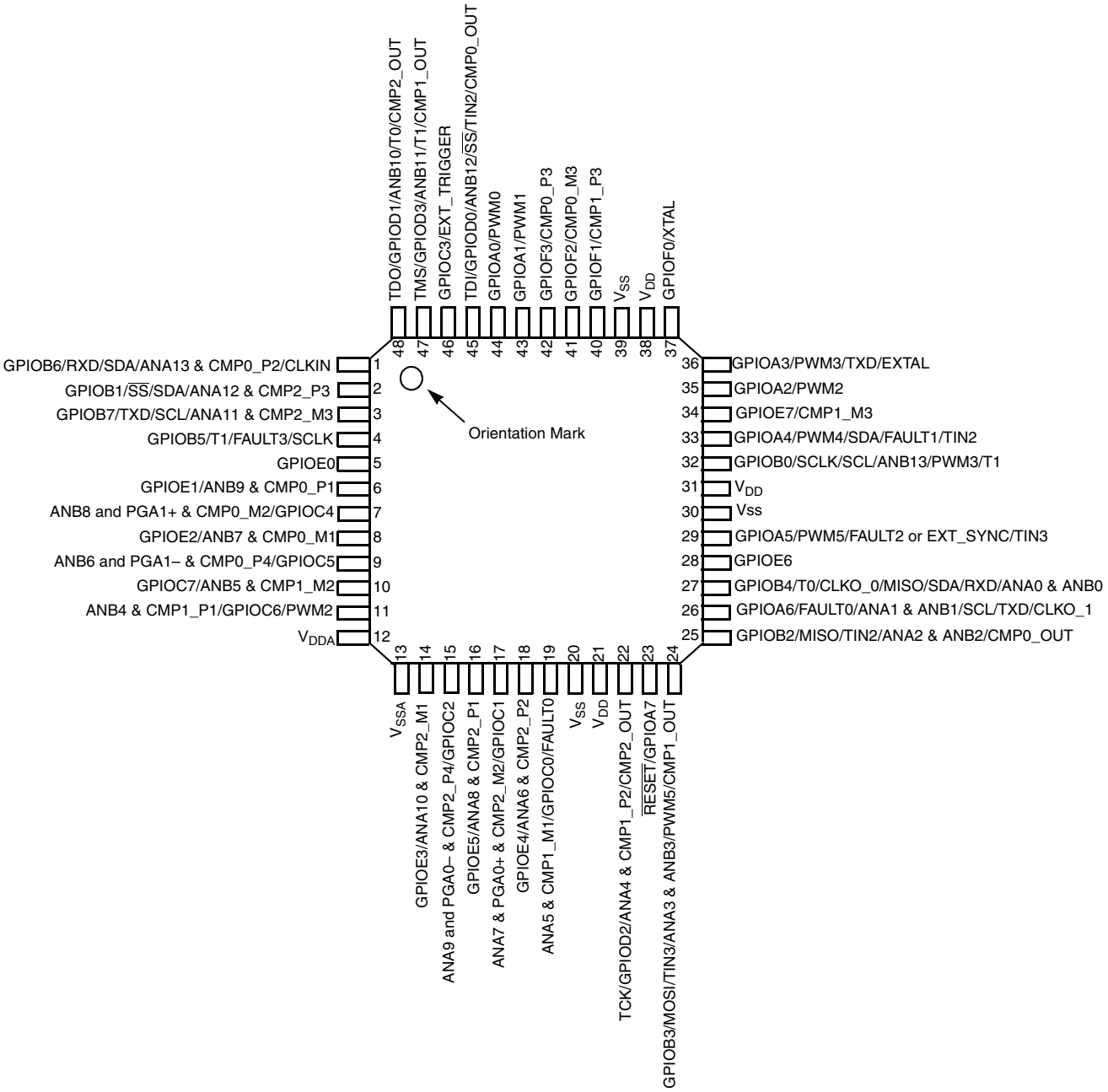


Figure 7. Top View, MC56F8006 48-Pin LQFP Package

4.3 56F8006/56F8002 Signal Pins

After reset, each pin is configured for its primary function (listed first). Any alternate functionality must be programmed via the GPIO module's peripheral enable registers (GPIO_x_PER) and SIM module's (GPS_xn) GPIO peripheral select registers. If CLKIN or XTAL is selected as device external clock input, the CLK_MOD bit in the OCCS oscillator control register (OSCTL) needs to be set too. EXT_SEL bit in OSCTL selects CLKIN or XTAL.

Table 5. 56F8006/56F8002 Signal and Package Information (continued)

Signal Name	28 SOIC	32 LQFP	32 PSDIP	48 LQFP	Type	State During Reset	Signal Description
GPIOA3	17	24	20	36	Input/ Output	Input, internal pullup enabled	Port A GPIO — This GPIO pin can be individually programmed as an input or output pin.
(PWM3)					Output		PWM3 — The PWM channel 3.
(TXD)					Output		TXD — The SCI transmit data output or transmit/receive in single wire operation.
(EXTAL)					Analog Input		EXTAL — External Crystal Oscillator Input. This input can be connected to a 32.768 kHz or 1–16 MHz external crystal or ceramic resonator. When used to supply a source to the internal PLL, the crystal/resonator must be in the 4 MHz to 8 MHz range. Tie this pin low or configure as GPIO if XTAL is being driven by an external clock source. If using a 32.768 kHz crystal, place the crystal as close as possible to device pins to speed startup. After reset, the default state is GPIOA3.
GPIOA4	16	22	18	33	Input/ Output	Input, internal pullup enabled	Port A GPIO — This GPIO pin can be individually programmed as an input or output pin.
(PWM4)					Output		PWM4 — The PWM channel 4.
(SDA)					Input/Open-drain Output		SDA — The I^2C serial data line.
(FAULT1)					Input		FAULT1 — PWM fault input 1used for disabling selected PWM outputs in cases where fault conditions originate off-chip.
(TIN2)					Input		TIN2 — Dual timer module channel 2 input After reset, the default state is GPIOA4.
GPIOA5	14	20	16	29	Input/ Output	Input, internal pullup enabled	Port A GPIO — This GPIO pin can be individually programmed as an input or output pin.
(PWM5)					Output		PWM5 — The PWM channel 5.
(FAULT2/ EXT_SYNC)					Input/ Output		FAULT2 — PWM fault input 2 used for disabling selected PWM outputs in cases where fault conditions originate off-chip. EXT_SYNC — When not being used as a fault input, this pin can be used to receive a pulse to reset the PWM counter or to generate a positive pulse at the start of every PWM cycle.
(TIN3)					Input		TIN3 — Dual timer module channel 3 input After reset, the default state is GPIOA5.

Table 5. 56F8006/56F8002 Signal and Package Information (continued)

Signal Name	28 SOIC	32 LQFP	32 PSDIP	48 LQFP	Type	State During Reset	Signal Description
GPIOE5 (ANA8 and CMP2_P1)				16	Input/ Output Analog Input	Input, internal pullup enabled	Port E GPIO — This GPIO pin can be individually programmed as an input or output pin. ANA8 and CMP2_P1— Analog input to channel 8 of ADCA and positive input 1 of analog comparator 2. After reset, the default state is GPIOE5.
GPIOE6				28	Input/ Output	Input, internal pullup enable	Port E GPIO — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is GPIOE6.
GPIOE7 (CMP1_M3)				34	Input/ Output Analog Input	Input, internal pullup enabled	Port E GPIO — This GPIO pin can be individually programmed as an input or output pin CMP1_M3 — Analog input to both negative input 3 of analog comparator 1. After reset, the default state is GPIOE7.
GPIOF0 (XTAL)	18	25	21	37	Input/ Output Analog Input/ Output	Input, internal pullup enabled	Port F GPIO — This GPIO pin can be individually programmed as an input or output pin. XTAL — External Crystal Oscillator Output. This output connects the internal crystal oscillator output to an external crystal or ceramic resonator. After reset, the default state is GPIOF0.
GPIOF1 (CMP1_P3)				40	Input/ Output Analog Input	Input, internal pullup enabled	Port F GPIO — This GPIO pin can be individually programmed as an input or output pin CMP1_P3 — Analog input to both positive input 3 of analog comparator 1. After reset, the default state is GPIOF1
GPIOF2 (CMP0_M3)				41	Input/ Output Analog Input	Input, internal pullup enabled	Port F GPIO — This GPIO pin can be individually programmed as an input or output pin. CMP0_M3 — Analog input to both negative input 3 of analog comparator 0. After reset, the default state is GPIOF2.
GPIOF3 (CMP0_P3)				42	Input/ Output Analog Input	Input, internal pullup enabled	Port F GPIO — This GPIO pin can be individually programmed as an input or output pin. CMP0_P3 — Analog input to both positive input 3 of analog comparator 0. After reset, the default state is GPIOF3.

On-chip RAM is also mapped into program space starting at P: 0x00 8000. This makes for easier online reprogramming of on-chip flash.

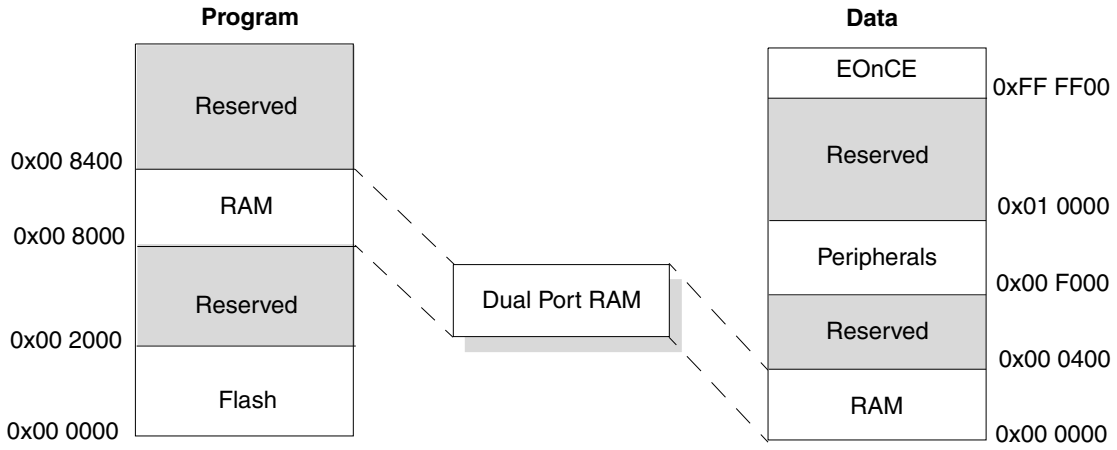


Figure 8. 56F8006 Dual Port RAM Map

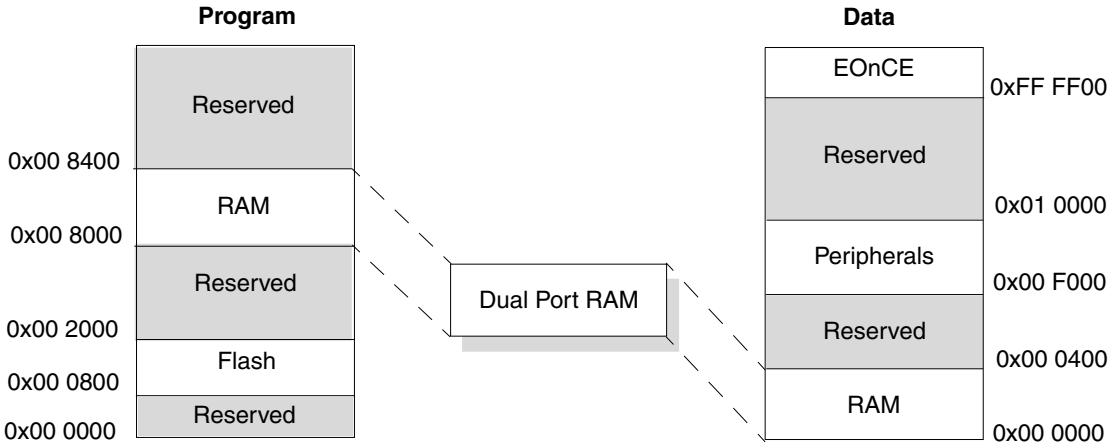


Figure 9. 56F8002 Dual Port RAM Map

5.4 Interrupt Vector Table and Reset Vector

The location of the vector table is determined by the vector base address register (VBA). The value in this register is used as the upper 14 bits of the interrupt vector VAB[20:0]. The lower seven bits are determined based on the highest priority interrupt and are then appended onto VBA before presenting the full VAB to the core. Please see the *MC56F8006 Peripheral Reference Manual* for detail. The reset startup addresses of 56F8002 and 56F8006 are different.

- 56F8006 startup address is located at 0x00 0000. The reset value of VBA is reset to a value of 0x0000 that corresponds to address 0x00 0000
- 56F8002 startup address is located at 0x00 0800. The reset value of VBA is reset to a value of 0x0010 that corresponds to address 0x00 0800

By default, the chip reset address and COP reset address correspond to vector 0 and 1 of the interrupt vector table. In these instances, the first two locations in the vector table must contain branch or JMP instructions. All other entries must contain JSR instructions.

The highest number vector, a user assignable vector USER6 (vector 50), can be defined as a fast interrupt if the instruction located in this vector location is not a JSR or BSR instruction. Please see section 9.3.3.3 of *DSP56800E 16-Bit Core Reference Manual* for detail.

7.2.4 Flash Lockout Recovery without Mass Erase

7.2.4.1 Without Presenting Back Door Access Keys to the Flash Unit

A user can un-secure a secured device by programming the word 0x0000 into program flash location 0x00 1FF7. After completing the programming, the JTAG TAP controller and the device must be reset to return to normal unsecured operation.

You are responsible for directing the device to invoke the flash programming subroutine to reprogram the word 0x0000 into program flash location 0x00 1FF7. This is done by, for example, toggling a specific pin or downloading a user-defined key through serial interfaces.

NOTE

Flash contents can be programmed only from 1s to 0s.

7.2.4.2 Presenting Back Door Access Key to the Flash Unit

It is possible to temporarily bypass the security through a back door access scheme, using a 4-word key, to temporarily unlock of the flash. A back door access requires support from the embedded software. This software would typically permit an external user to enter a four word code through one of the communications interfaces and then use it to attempt the unlock sequence. If your input matches the four word code stored at location 0x00 1FFC–0x00 1FFF in the flash memory, the part immediately becomes unsecured (at runtime) and you can access internal memory via JTAG/EOnCE port. Refer to the *MC56F8006 Peripheral Reference Manual* for detail. The key must be entered in four consecutive accesses to the flash, so this routine should be designed to run in RAM.

7.3 Product Analysis

The recommended method of unsecuring a secured device for product analysis of field failures is via the method described in Section 7.2.4.2, “Presenting Back Door Access Key to the Flash Unit.” The customer would need to supply technical support with the details of the protocol to access the subroutines in flash memory. An alternative method for performing analysis on a secured device would be to mass-erase and reprogram the flash with the original code, but modify the security word or not program the security word.

8 Specifications

8.1 General Characteristics

The 56F8006/56F8002 is fabricated in high-density low power and low leakage CMOS with a maximum voltage of 3.6 V digital inputs during normal operation without causing damage.

Absolute maximum ratings in Table 12 are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond these ratings may affect device reliability or cause permanent damage to the device.

Unless otherwise stated, all specifications within this chapter apply over the temperature range of –40ºC to 105ºC ambient temperature over the following supply ranges: $V_{SS} = V_{SSA} = 0V$, $V_{DD} = V_{DDA} = 3.0–3.6$ V, CL $\leq$ 50 pF, $f_{OP} = 32$ MHz

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.

8.2 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified Table 12 may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, take normal precautions to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}) or the programmable pullup resistor associated with the pin is enabled.

Table 12. Absolute Maximum Ratings

(V_{SS} = 0 V, V_{SSA} = 0 V)

Characteristic	Symbol	Notes	Min	Max	Unit
Supply Voltage Range	V_{DD}		–0.3	3.8	V
Analog Supply Voltage Range	V_{DDA}		–0.3	3.6	V
Voltage difference V_{DD} to V_{DDA}	ΔV_{DD}		–0.3	0.3	V
Voltage difference V_{SS} to V_{SSA}	ΔV_{SS}		–0.3	0.3	V
Digital Input Voltage Range	V_{IN}	Pin Groups 1, 2	–0.3	V_{DD}+0.3	V
Oscillator Voltage Range	V_{OSC}	Pin Group 4	TBD	TBD	V
Analog Input Voltage Range	V_{INA}	Pin Group 3	–0.3	3.6	V
Input clamp current, per pin (V_{IN} < 0)[1 2 3]	V_{IC}		—	–25.0	mA
Output clamp current, per pin (V_O < 0)[1 2 3]	V_{OC}		—	–20.0	mA
Output Voltage Range (Normal Push-Pull mode)	V_{OUT}	Pin Group 1	–0.3	V_{DD}	V
Ambient Temperature Industrial	T_A		–40	105	°C
Storage Temperature Range (Extended Industrial)	T_{STG}		–55	150	°C

1 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages, then use the larger of the two resistance values.

2 All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.

3 Power supply must maintain regulation within operating VDD range during instantaneous and operating maximum current conditions. If positive injection current (V_{In} > V_{DD}) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} loads shunt current greater than maximum injection current. This is the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present or if the clock rate is low (which would reduce overall power consumption).

8.2.1 ESD Protection and Latch-Up Immunity

Although damage from electrostatic discharge (ESD) is much less common on these devices than on early CMOS circuits, use normal handling precautions to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits. During the device qualification ESD stresses were performed for the human body model (HBM), the machine model (MM), and the charge device model (CDM).

Table 18. 48LQFP Package Thermal Characteristics

Characteristic	Comments	Symbol	Value (LQFP)	Unit
Junction to ambient Natural convection	Single layer board (1s)	$R_{\theta JA}$	79	°C/W
Junction to ambient Natural convection	Four layer board (2s2p)	$R_{\theta JMA}$	55	°C/W
Junction to ambient (@200 ft/min)	Single layer board (1s)	$R_{\theta JMA}$	66	°C/W
Junction to ambient (@200 ft/min)	Four layer board (2s2p)	$R_{\theta JMA}$	48	°C/W
Junction to board		$R_{\theta JB}$	34	°C/W
Junction to case		$R_{\theta JC}$	20	°C/W
Junction to package top	Natural Convection	Ψ_{JT}	4	°C/W

NOTE

Junction-to-ambient thermal resistance determined per JEDEC JESD51–3 and JESD51–6. Thermal test board meets JEDEC specification for this package.

Junction-to-board thermal resistance determined per JEDEC JESD51–8. Thermal test board meets JEDEC specification for the specified package.

Junction-to-case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51–2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT

Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

See Section 9.1, “Thermal Design Considerations,” for more detail on thermal design considerations.

8.4 Recommended Operating Conditions

This section includes information about recommended operating conditions.

Table 22. Supply Current Consumption (continued)

Mode	Conditions	Typical @ 3.3 V, 25 °C		Maximum @ 3.6 V, 105 °C		Maximum @ 3.6 V, 125 °C	
		I_{DD} [1]	I_{DDA}	I_{DD} [1]	I_{DDA}	I_{DD} [1]	I_{DDA}
LPwait [3]	32.768 kHz device clock; Clocked by a 32.768 kHz external crystal oscillator in power down; PLL disabled; All peripheral modules disabled and clock gated off; processor core in wait state	157.55 µA	1.57 mA	380 µA	3.4 mA	398 µA	3.6 mA
Stop	32 MHz device clock relaxation oscillator (ROSC) in high speed mode; PLL engaged; all peripheral module and core clocks are off; ADC/DAC/comparator powered off; processor core in stop state	8.21 mA	65.51 µA	9.8 mA	130 µA	10.3 mA	132 µA
LSstop [2]	200 kHz device clock; relaxation oscillator (ROSC) in standby mode; PLL disabled; all peripheral modules disabled and clock gated off; processor core in stop state.	194.69 µA	65.51 µA	340 µA	120 µA	357 µA	123 µA
LPstop [2]	32.768 kHz device clock; Clocked by a 32.768 kHz external crystal relaxation oscillator (ROSC) in power down; PLL disabled; all peripheral modules disabled and clock gated off; processor core in stop state.	2.77 µA	13.99 nA	45 µA	3.0 µA	58 µA	3.6 µA
PPD [4] with XOSC	32.768 kHz clock fed on XTAL RTC or COP monitoring XOSC (but no wakeup) processor core in stop state	879.72 nA	11.56 nA	18 µA	2.4 µA	22 µA	3.0 µA
PPD with LP oscillator (1 kHz) enabled	RTC or COP monitoring LP oscillator (but no wakeup); processor core in stop state.	499.15 nA	13.9 nA	14 µA	2.4 µA	17 µA	2.8 mA
PPD with no clock monitoring	RTC and LP oscillator are disabled; processor core in stop state.	494.04 nA	12.88 nA	14 µA	2.4 µA	17 µA	2.8 µA

1 No output switching; all ports configured as inputs; all inputs low; no DC loads.

2 Low speed mode: LPR (lower voltage regulator control bit) = 0 and voltage regulator is in full regulation. Characterization only.

3 Low power mode: LPR (lower voltage regulator control bit) = 1; the voltage regulator is put into standby.

4 Partial power down mode: PPDE (partial power down enable bit) = 1; power management controller (PMC) enters partial power down mode the next time that the STOP command is executed.

8.7 Flash Memory Characteristics

Table 23. Flash Timing Parameters

Characteristic	Symbol	Min	Typ	Max	Unit
Program time[1]	tprog	20	—	40	μs
Erase time [2]	terase	20	—	—	ms
Mass erase time	tme	100	—	—	ms

1 There is additional overhead that is part of the programming sequence. See the *MC56F8006 Peripheral Reference Manual* for detail.

2 Specifies page erase time. There are 512 bytes per page in the program flash memory.

8.8 External Clock Operation Timing

Table 24. External Clock Operation Timing Requirements[1]

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency of operation (external clock driver)[2]	f_{osc}	—	—	64	MHz
Clock pulse width[3]	t_{PW}	6.25	—	—	ns
External clock input rise time[4]	t_{rise}	—	—	3	ns
External clock input fall time[5]	t_{fall}	—	—	3	ns
Input high voltage overdrive by an external clock	V_{ih}	$0.85V_{DD}$	—	—	V
Input high voltage overdrive by an external clock	V_{il}	—	—	$0.3V_{DD}$	V

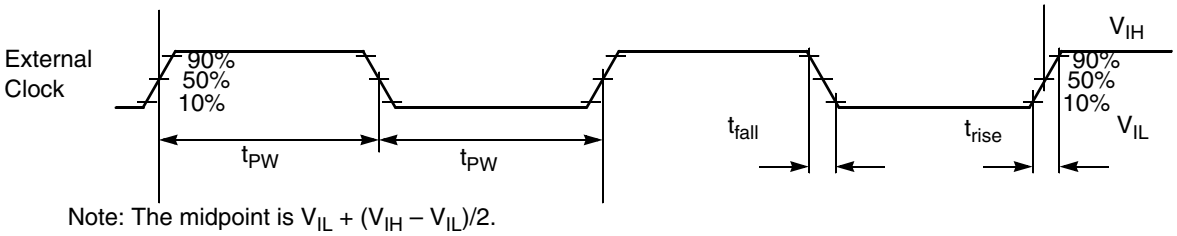
1 Parameters listed are guaranteed by design.

2 See Figure 21 for detail on using the recommended connection of an external clock driver.

3 The chip may not function if the high or low pulse width is smaller than 6.25 ns.

4 External clock input rise time is measured from 10% to 90%.

5 External clock input fall time is measured from 90% to 10%.



Note: The midpoint is $V_{IL} + (V_{IH} - V_{IL})/2$.

Figure 21. External Clock Timing

8.9 Phase Locked Loop Timing

Table 25. Phase Locked Loop Timing

Characteristic	Symbol	Min	Typ	Max	Unit
PLL input reference frequency[1]	f_{ref}	4	8	—	MHz
PLL output frequency[2]	f_{op}	120	192	—	MHz
PLL lock time[3] [4]	t_{plls}	—	40	100	µs
Accumulated jitter using an 8 MHz external crystal as the PLL source[5]	J_A	—	—	0.37	%
Cycle-to-cycle jitter	$t_{jitterpll}$	—	350	—	ps

1 An externally supplied reference clock should be as free as possible from any phase jitter for the PLL to work correctly. The PLL is optimized for 8 MHz input.

2 The core system clock operates at 1/6 of the PLL output frequency.

3 This is the time required after the PLL is enabled to ensure reliable operation.

4 From powerdown to powerup state at 32 MHz system clock state.

5 This is measured on the CLKO signal (programmed as system clock) over 264 system clocks at 32 MHz system clock frequency and using an 8 MHz oscillator frequency.

8.10 Relaxation Oscillator Timing

Table 26. Relaxation Oscillator Timing

Characteristic	Symbol	Minimum	Typical	Maximum	Unit
Relaxation oscillator output frequency[1] Normal Mode Standby Mode	f_{op}	—	 8.05 400	—	 MHz kHz
Relaxation oscillator stabilization time[2]	t_{roscs}	—	1	3	ms
Cycle-to-cycle jitter. This is measured on the CLKO signal (programmed prescaler_clock) over 264 clocks[3]	$t_{jitterrosc}$	—	400	—	ps
Variation over temperature –40 °C to 105 °C[4]		—	—	–3.0 to +2.0	%
Variation over temperature 0 °C to 105 °C[5]		—	—	–2.0 to +2.0	%
Variation over temperature –40 °C to 125 °C[4]		—	—	–3.5 to +3.0	%

1 Output frequency after factory trim.

2 This is the time required from standby to normal mode transition.

3 J_A is required to meet QSCI requirements.

4 See Figure 22. The power supply VDD must be greater than or equal to 2.6 V. Below 2.6 V, the maximum variation over the whole temperature and whole voltage range from 1.8 V to 2.6 V will be +/-16%.

5 This data is only applied to devices with temperature range from –40 °C to 105 °C.

8.11 Reset, Stop, Wait, Mode Select, and Interrupt Timing

NOTE

All address and data buses described here are internal.

Table 27. Reset, Stop, Wait, Mode Select, and Interrupt Timing[1,2]

Characteristic	Symbol	Typical Min	Typical Max	Unit	See Figure
Minimum $\overline{\text{RESET}}$ Assertion Duration	t_{RA}	4T	—	ns	—
Minimum GPIO pin Assertion for Interrupt	t_{IW}	2T	—	ns	Figure 24
$\overline{\text{RESET}}$ deassertion to First Address Fetch	t_{RDA}	$96T_{OSC}$ + 64T	$97T_{OSC}$ + 65T	ns	—
Delay from Interrupt Assertion to Fetch of first instruction (exiting Stop)	t_{IF}	—	6T	ns	—

1 In the formulas, T = system clock cycle and T_{osc} = oscillator clock cycle. For an operating frequency of 32 MHz, T = 31.25 ns. At 4 MHz (used coming out of reset and stop modes), T = 250 ns.

2 Parameters listed are guaranteed by design.

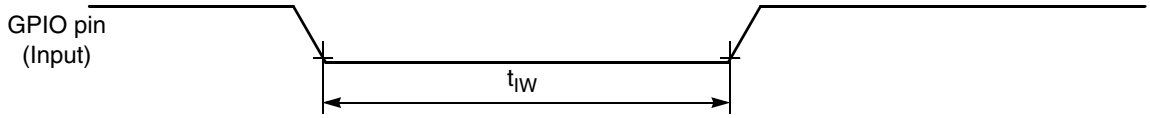


Figure 24. GPIO Interrupt Timing (Negative Edge-Sensitive)

8.12 External Oscillator (XOSC) Characteristics

Reference Figure 10, and Figure 11, and Figure 12 for crystal or resonator circuits.

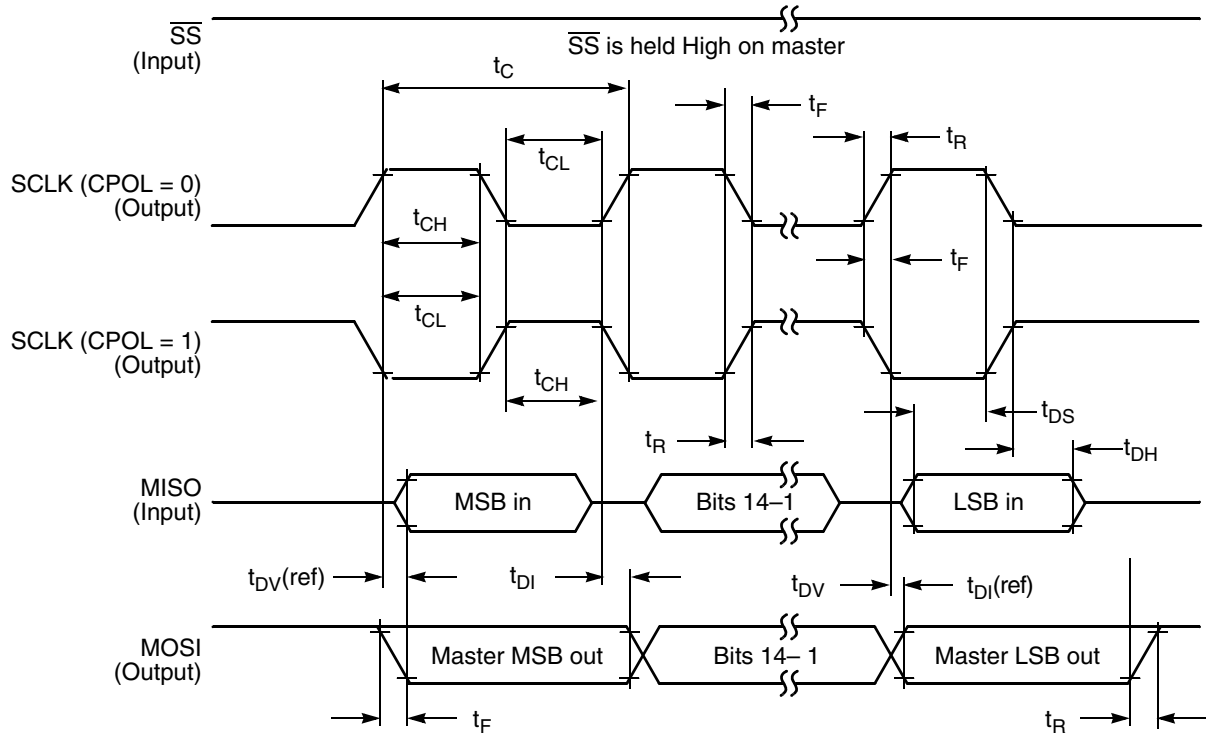


Figure 28. SPI Master Timing (CPHA = 1)

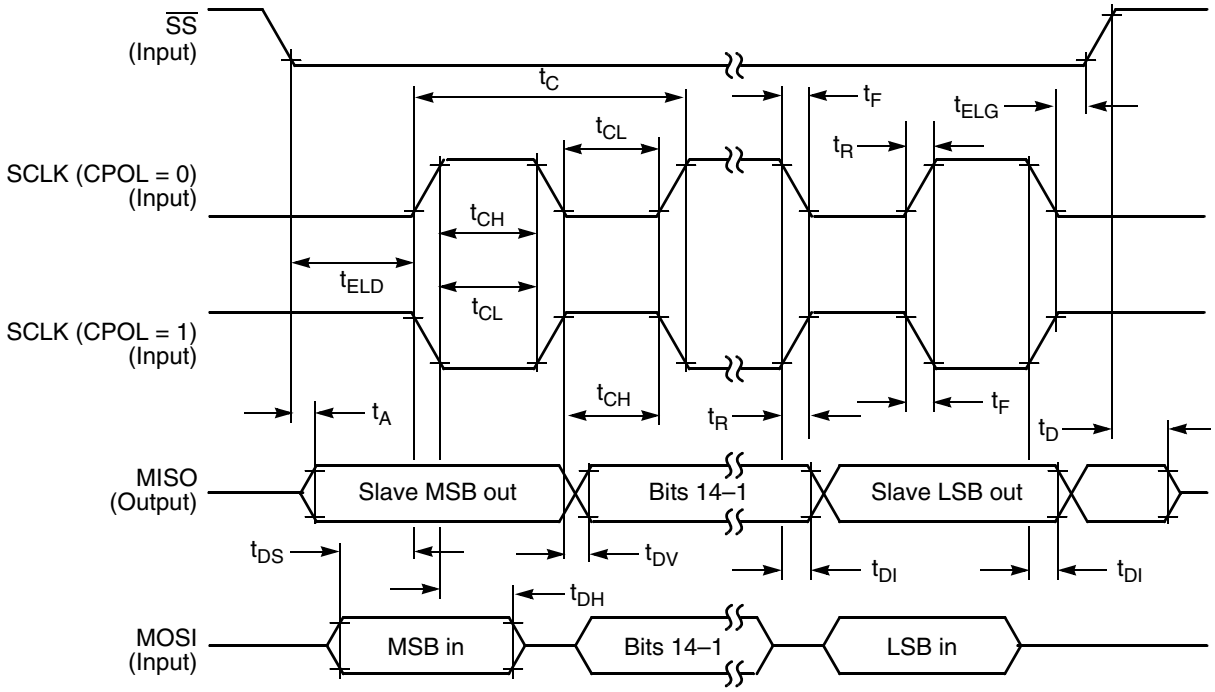


Figure 29. SPI Slave Timing (CPHA = 0)

Table 37. ADC Characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA})

Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
Supply current ADLPC=1 ADLSMP=1 ADCO=1		I_{DDAD}	—	120	—	μA	
Supply current ADLPC=1 ADLSMP=0 ADCO=1		I_{DDAD}	—	202	—	μA	
Supply current ADLPC=0 ADLSMP=1 ADCO=1		I_{DDAD}	—	288	—	μA	
Supply current ADLPC=0 ADLSMP=0 ADCO=1		I_{DDAD}	—	0.532	1	mA	
ADC asynchronous clock source	High speed (ADLPC=0)	f_{ADACK}	2	3.3	5	MHz	t_{ADACK} = $1/f_{ADACK}$
	Low power (ADLPC=1)		1.25	2	3.3		
Conversion time (including sample time)	Short sample (ADLSMP=0)	t_{ADC}	—	20	—	ADCK cycles	
	Long sample (ADLSMP=1)		—	40	—		
Sample time	Short sample (ADLSMP=0)	t_{ADS}	—	3.5	—	ADCK cycles	
	Long sample (ADLSMP=1)		—	23.5	—		
Differential Non-linearity	12-bit mode	DNL	—	±1.75	—	LSB[2]	
	10-bit mode[3]		—	±0.5	±1.0		
	8-bit mode[3]		—	±0.3	±0.5		
Integral non-linearity	12-bit mode	INL	—	±1.5	—	LSB[2]	
	10-bit mode		—	±0.5	±1.0		
	8-bit mode		—	±0.3	±0.5		
Quantization error	12-bit mode	E_Q	—	–1 to 0	—	LSB[2]	
	10-bit mode		—	—	±0.5		
	8-bit mode		—	—	±0.5		
Input leakage error	12-bit mode	E_{IL}	—	±2	—	LSB[2]	Pad leakage[4] * R_{AS}
	10-bit mode		—	±0.2	±4		
	8-bit mode		—	±0.1	±1.2		
Temp sensor slope	–40°C–25°C	m	—	1.646	—	mV/°C	
	25°C–125°C		—	1.769	—		
Temp sensor voltage	25°C	V_{TEMP25}	—	701.2	—	mV	

Power consumption is given by the following equation:

Eqn. 1

$$\begin{aligned}\text{Total power} = \quad & \text{A: internal [static component]} \\ & +\text{B: internal [state-dependent component]} \\ & +\text{C: internal [dynamic component]} \\ & +\text{D: external [dynamic component]} \\ & +\text{E: external [static component]}\end{aligned}$$

A, the internal [static] component, is comprised of the DC bias currents for the oscillator, leakage currents, PLL, and voltage references. These sources operate independently of processor state or operating frequency.

B, the internal [state-dependent] component, reflects the supply current required by certain on-chip resources only when those resources are in use. These include RAM, flash memory, and the ADCs.

C, the internal [dynamic] component, is classic $C*V^2*F$ CMOS power dissipation corresponding to the 56800E core and standard cell logic.

D, the external [dynamic] component, reflects power dissipated on-chip as a result of capacitive loading on the external pins of the chip. This is also commonly described as $C*V^2*F$, although simulations on two of the I/O cell types used on the 56800E reveal that the power-versus-load curve does have a non-zero Y-intercept.

Table 39. I/O Loading Coefficients at 10 MHz

	Intercept	Slope
8 mA drive	1.3	0.11 mW/pF
4 mA drive	1.15 mW	0.11 mW/pF

Power due to capacitive loading on output pins is (first order) a function of the capacitive load and frequency at which the outputs change. Table 39 provides coefficients for calculating power dissipated in the I/O cells as a function of capacitive load. In these cases:

$$\textit{TotalPower} = \Sigma((\text{Intercept} + \text{Slope}*\text{Cload})*\text{frequency}/10\ \text{MHz}) \qquad \textit{Eqn. 2}$$

where:

- Summation is performed over all output pins with capacitive loads
- Total power is expressed in mW
- C_{load} is expressed in pF

Because of the low duty cycle on most device pins, power dissipation due to capacitive loads was found to be fairly low when averaged over a period of time.

E, the external [static component], reflects the effects of placing resistive loads on the outputs of the device. Sum the total of all V^2/R or IV to arrive at the resistive load contribution to power. Assume V = 0.5 for the purposes of these rough calculations. For instance, if there is a total of eight PWM outputs driving 10 mA into LEDs, then P = 8*0.5*0.01 = 40 mW.

In previous discussions, power consumption due to parasitics associated with pure input pins is ignored, as it is assumed to be negligible.

10 Package Mechanical Outline Drawings

10.1 28-pin SOIC Package

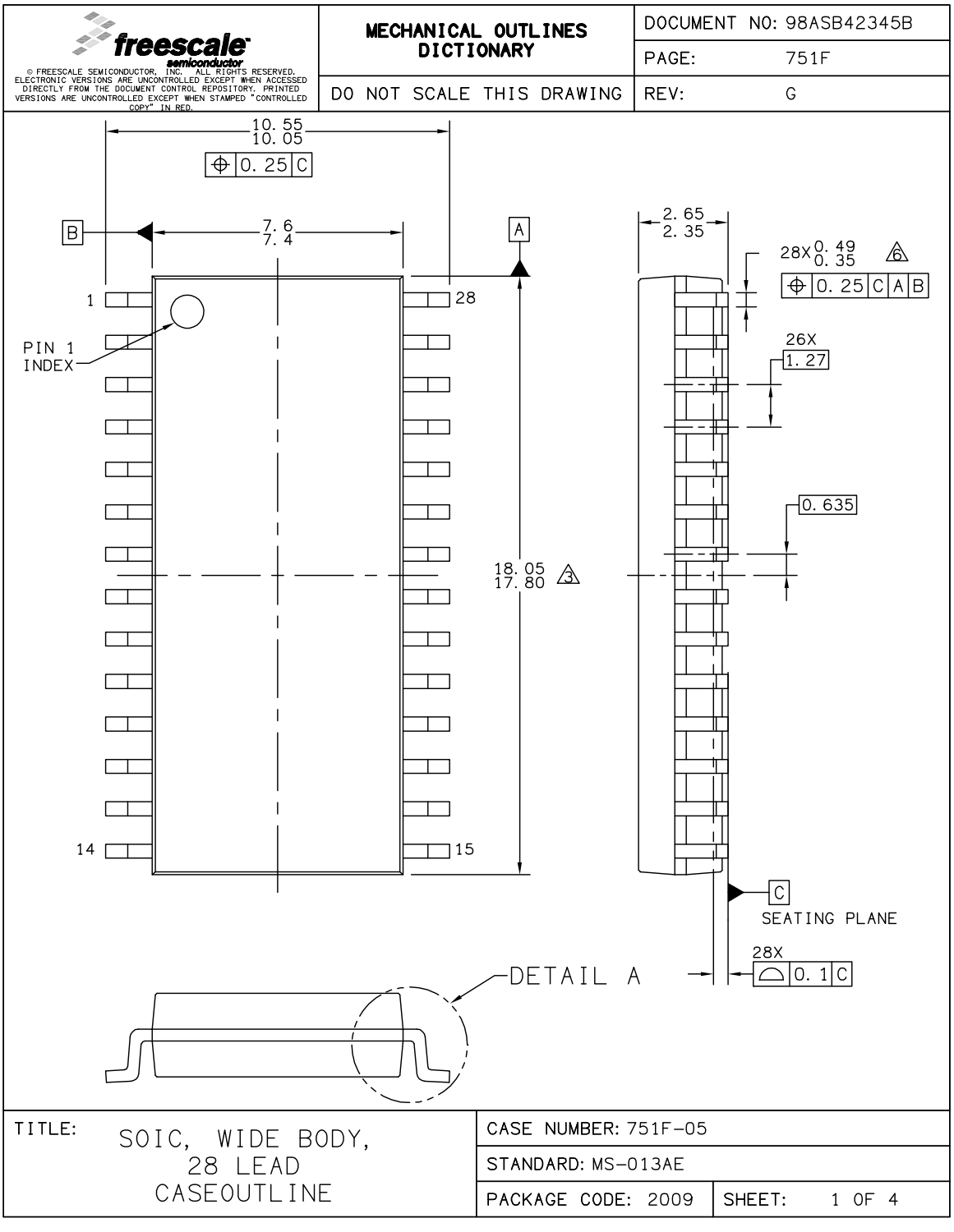


Table 43. Interrupt Vector Table Contents[1] (continued)

Peripheral	Vector Number	User Encoding	Priority Level	Vector Base Address +	Interrupt Function
Reserved	34- 39	0x22-0x27	0	P:0x44 - P:0x4E	Reserved
core	40	N/A	0	P:0x50	SW Interrupt 0
core	41	N/A	1	P:0x52	SW Interrupt 1
core	42	N/A	2	P:0x54	SW Interrupt 2
core	43	N/A	3	P:0x56	SW Interrupt 3
SWILP	44	N/A	-1	P:0x58	SW Interrupt Low Priority
USER1	45	N/A	1	P:0x5A	User Programmable Priority Level 1 Interrupt
USER2	46	N/A	1	P:0x5C	User Programmable Priority Level 1 Interrupt
USER3	47	N/A	1	P:0x5E	User Programmable Priority Level 1 Interrupt
USER4	48	N/A	2	P:0x60	User Programmable Priority Level 2 Interrupt
USER5	49	N/A	2	P:0x62	User Programmable Priority Level 2 Interrupt
USER6[3]	50	N/A	2	P:0x64	User Programmable Priority Level 2 Interrupt

1 Two words are allocated for each entry in the vector table. This does not allow the full address range to be referenced from the vector table, providing only 19 bits of address.

2 If the VBA is set to the reset value, the first two locations of the vector table overlay the chip reset addresses because the reset address would match the base of this vector table.

3 USER6 vector can be defined as a fast interrupt if the instruction located in this vector location is not a JSR or BSR instruction. Please see section 9.3.3.3 of *DSP56800E 16-Bit Core Reference Manual* for detail.

Appendix B
Peripheral Register Memory Map and Reset Value

NOTE

In Table 44, ADC0 stands for ADCA, ADC1 stands for ADCB, and GPIOn is the same as GPIO_n (for example, GPIOA_PUR is the same as GPIO_A_PUR).

Table 44. Detailed Peripheral Memory Map

Offset Addr. (Hex)	Reset Value (Hex)	Periph.	Register	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Bit 0
00	0000	TMR0	TMR0_ COMP1	COMPARISON_1															
01	0000	TMR0	TMR0_ COMP2	COMPARISON_2															
02	0000	TMR0	TMR0_ CAPT	CAPTURE															
03	0000	TMR0	TMR0_ LOAD	LOAD															
04	0000	TMR0	TMR0_ HOLD	HOLD															
05	0000	TMR0	TMR0_ CNTR	COUNTER															
06	0000	TMR0	TMR0_ CTRL	CM			PCS				SCS		ONCE	LENGTH	DIR	Co_INIT	OM		
07	0000	TMR0	TMR0_ SCTRL	TCF	TCFIE	TOF	TOFIE	IEF	IEFIE	IPS	INPUT	CAPTURE_ MODE		MSTR	EEOF	VAL	FORCE	OPS	OEN
08	0000	TMR0	TMR0_ CMPLD1	COMPARATOR_LOAD_1															
09	0000	TMR0	TMR0_ CMPLD2	COMPARATOR_LOAD_2															